Passive memristor synaptic circuits with multiple timing dependent plasticity mechanisms

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Abstract

Adaptation of synaptic strength is central to memory and learning in biological systems, enabling important high-level processes such as the ability of animals to respond to a changing environment. Memristor devices are a promising new, nanoscale technology that emulates the function of synapses and can therefore be used to represent synaptic elements in analog artificial neural networks. The main mechanism to carry out unsupervised adaptation of weights in memristive synapses currently involves artificial spiking neural network designs relying on spike-timing dependent plasticity (STDP). We present and analyze a new memristive circuit that in addition to STDP learning rules also implements competitive adjustment based on relative timing of presynaptic inputs. The cooperative effect of multiple learning rules in the new circuit may ameliorate the problem of erasure of synaptic weights

Keywords: memristor, synapse, input-driven plasticity, STDP, artificial spiking neural network, catastrophic forgetting

1. Introduction

Artificial neural networks aim to provide a new computational platform for solving a multitude of cognitive problems from visual and auditory perception to meaningful interaction of biomimetic robots with their environment. There is a wide variety of approaches to the implementation of artificial neural networks, ranging from emulation on a classical digital computer to specialized analog hardware implementations. However, most of the approaches incorporate memory-like elements that correspond to synapses found in biological structures in the brain, where they serve to connect individual neurons and regulate transmission of neuron signals by being in either a potentiated or a depressed state; a potentiated synapse provides for easier signal transmission, whereas a depressed synapse reduces the efficacy of signal transmission.

In an artificial neural network implemented in a digital system the state of an artificial synapse is typically represented by a multi-bit memory element whereas in analog systems, the synaptic state is non-discrete and varies in an analog manner. Memristors, first proposed by Leon Chua in the 1970's [1] and connected with experiments in key work of HP Lab [2], have recently been showed to emulate synapses and represent a very promising alternative to traditional analog circuit elements [3,4]. There are multiple reasons why memristors are especially promising for the development of an artificial brain-

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like system. Firstly, they are easily scalable down to nanoscale dimensions, which fits well with the expectation that these elements will greatly outnumber integrate and fire neurons. An average biological soma may have several thousand synaptic connections from other neurons. Secondly, storage of a memristor's state does not require any energy, and thus memristor can be used as a non-volatile memory. Memristors also exhibit significant nonlinearity in their current-voltage (IV) characteristics that allow for two distinct operation regimes – low voltage operation that does not disturb synaptic state and higher voltage operation that changes the state.

In biology, the change in synaptic states is well-documented and is presumed to underlie various brain behaviours e.g. Hebbian learning, brain plasticity, or adaptation to specific stimuli. Some artificial intelligence systems may do without a mechanism for changing the synaptic state, e.g. a deep neural network may be trained off-line and its synaptic weights hardwired into a system and deployed in practice afterwards. However, such an approach is inherently limited since a given system will not be able to adjust to new stimuli, be it a change in its environment, new visual shapes, and so on. Therefore it would be desirable for have mechanisms for on-line changes of synaptic state.

Of course, replication of every mechanism of biological adaptation is hardly possible, since biological synapses can grow, disappear and reappear, which are feats outside the realm of traditional solid-state electronics. The majority of research has concentrated on the replication of spike-timing dependent plasticity (STDP) that is observed in biological synapses. The focus has been to mostly design systems that exhibit the same synaptic changes found in biological counterparts [3,4,5,6,7]. However, biological neurons exhibit much larger variety of adaptation and computation than their neuromorphic counterparts due to their complex dendritic trees [8,9]. For instance, while STDP can be observed in proximal synapses in vivo, it is absent at distal synapses [10]. Therefore it is not clear that STDP-based learning is sufficient for training complex artificial neural networks. An alternative to STDP may be provided by plasticity based on relative timing of competing pre-synaptic signals.

In this paper we propose a new passive memristive circuit design that represents new type of learning in artificial synapses. We will show that it is able to implement competitive input-driven weight adjustment and explain how the adjustment mechanism interacts with the classical STDP mechanism.

2. Double-legged synaptic circuit as part of a spiking neural network

The proposed new circuit exhibiting novel synaptic behaviour consists only of memristive elements as shown in the dotted rectangle in Figure 1. Central to the functioning of this circuit is the double-legged memristor synapse(M-M') that consists of two memristors connected in series that connect a presynaptic neuron (N) with a postsynaptic neuron (N'). The double-legged terminology relates to the two connected legs between the M and M' synapse.

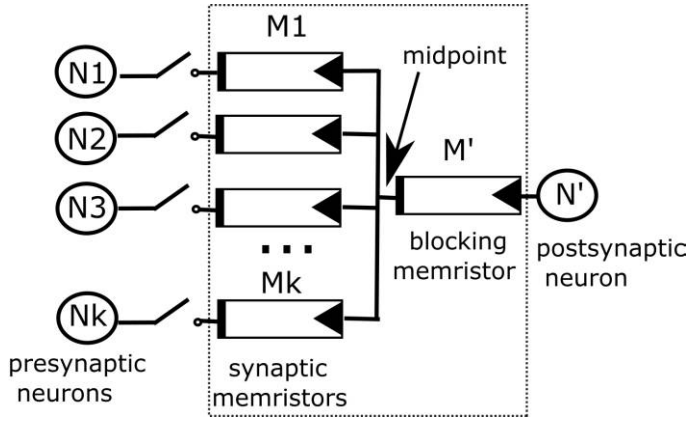


Figure 1. A single stage dendritic architecture based on a series of k double-legged connecting synapses (M-M') that connect the presynaptic neurons (N) with a postsynaptic neuron (N')

The neurons are assumed to be integrate-and-fire neurons, meaning that charge flows from presynaptic neurons to the postsynaptic neuron, where it dissipates. If however, enough charge is accumulated the neuron will fire. When a presynaptic neuron fires a spike, the switch between it and the following memristor would close and a charge will flow from the neuron to the postsynaptic neuron *N'*. The amount of charge transferred is controlled by the resistance state of intermediate memristors. Thus, the largest amount of charge would be transferred if both intermediate memristors would be in the low-resistance state. We assume that during firing of postsynaptic neuron, a backpropagating pulse is sent towards presynaptic neurons.

In order to maximize the interaction of spikes (and simplify our analysis) we will adopt a design akin to half-voltage programming scheme proposed for the memristor cross-bar arrays [11]. We assume that spikes from the presynaptic neurons as well as the backpropagation spike from the postsynaptic neuron oscillate as shown in Figure 2a. This shape of spikes allows to generate relative voltages up to $2V_P$ between synaptic circuit terminals depending on their temporal offset (Figure 2c).

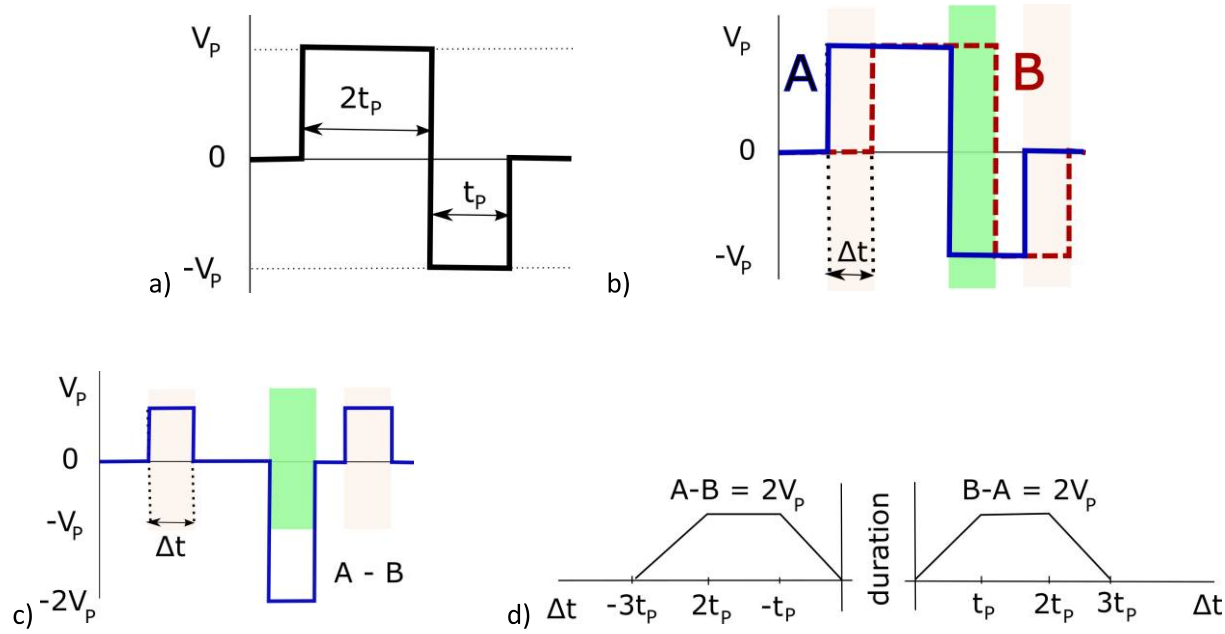


Figure 2. Graphs denoting the shape of a spike used by the spiking neurons (a), two pulses differing in time by offset Δt, with background color indicating the magnitude of voltage difference (b), the voltage difference between two pulses (c), and the duration of time when the absolute voltage difference between A and B is double that of V_P depending on Δt (d).

Finally, it is assumed that all neurons connected to the synapse fire only sporadically, and coincidences are rare. The most common occurrence would be a single presynaptic neuron spiking alone. Less often cases would be when:

- two presynaptic neurons fire simultaneously, or
- a presynaptic pulse overlaps with the backpropagation pulse from the postsynaptic neuron.

We further assume the cases of three neurons firing simultaneously are exceedingly rare and do not analyze their impact in this study.

3. Methods

This section summarizes our modelling methods including the model of memristor and the parameters of the spikes. We used SPICE OPUS [12] for our simulations. The term memristor was originally meant to describe a circuit modelling element complementing a resistor, capacitor and inductor, but in recent years it has been applied to several classes of physical devices governed by more general models [13], even those exhibiting volatile effects [14]. Two major classes of memristors exists. Valence change memory (VCM) is based on the diffusion of oxygen vacancies across a metal-oxide material, whereas in electrochemical metallization cells (ECM), switching is dependent on the migrations of cations from electrodes based on active materials. For the purpose of our modelling we have chosen physically based model for ECM memristors [15], used in work of S. Ferch et al [16]. In the model the memristor has a single state variable representing the length of the gap between the conductive filament and an electrode. SET happens when positive voltage is applied, whereas RESET when negative voltage is applied for sufficiently long time (Figure 3a). Figure 3c) indicates measured current under triangular pulse (Figure 3b). The evolution of underlying state variable, the gap, is shown in Figure 3d). Finally, Figure 3e) shows a quasi-static IV-characteristic of a single memristor exhibiting indicative pinch-hysteresis loop [17,18].

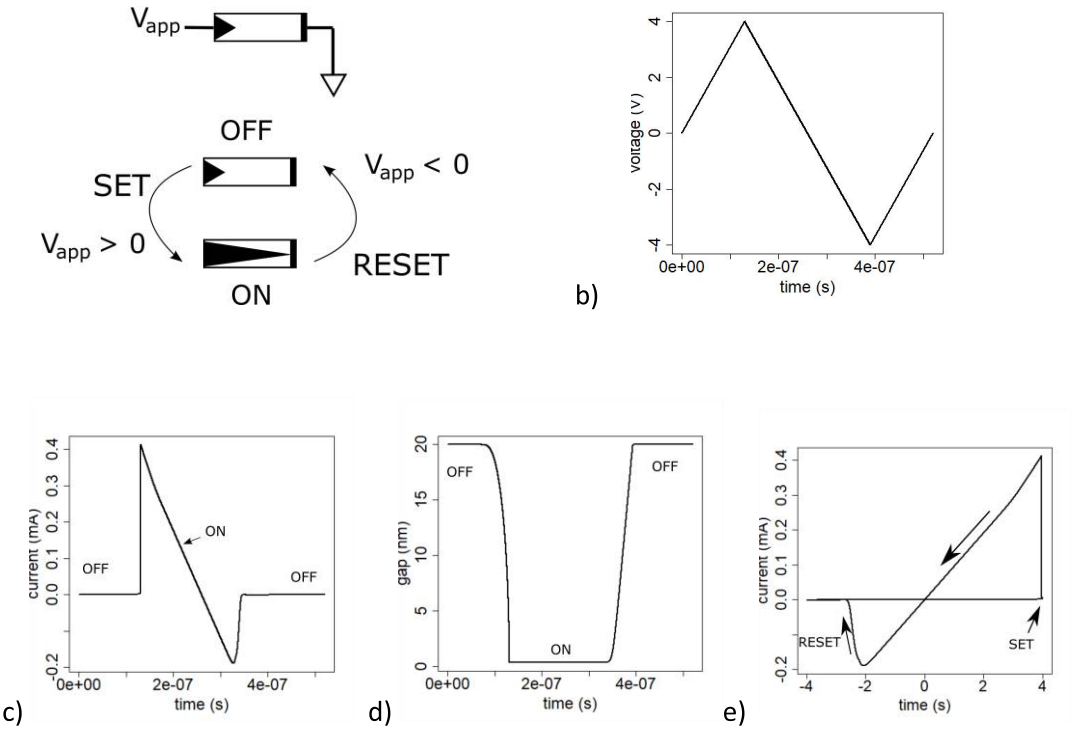


Figure 3. Schematic Characteristics of the ECM based system used in the modelling when driven by a triangular pulse with frequency 2 MHz. Simulation schema (a), applied voltage (b), current vs. time (c), gap vs. time (d) and its quasi-static IV characteristics.

Based on the properties of the model we chose values V_P = 2.5V and t_P = 1e-8 s for neural spikes (see Figure 2).

4. Simulations and results

The state space of a double-legged synaptic circuit consisting of two input memristors and a single output memristor can be represented by a cube as shown in Figure 4. Although a memristor device is an analogue device it is possible to examine the maximum current and minimum current states of the devices representing the ON and OFF states respectively. In this scenario each memristor can be in either of these states, thus the three memristor double-legged synapse gives eight possible combinations. The goal of this study is to examine the transitions between vertices of the cube, since these represent the extreme states of the circuit. The complexity of analysis of state transitions in the circuit is further compounded by possible relative timing of pulses. We have therefore selected three key simulation scenarios that demonstrate the key principles behind the state transitions occuring in the circuit and these are presented in the following section.

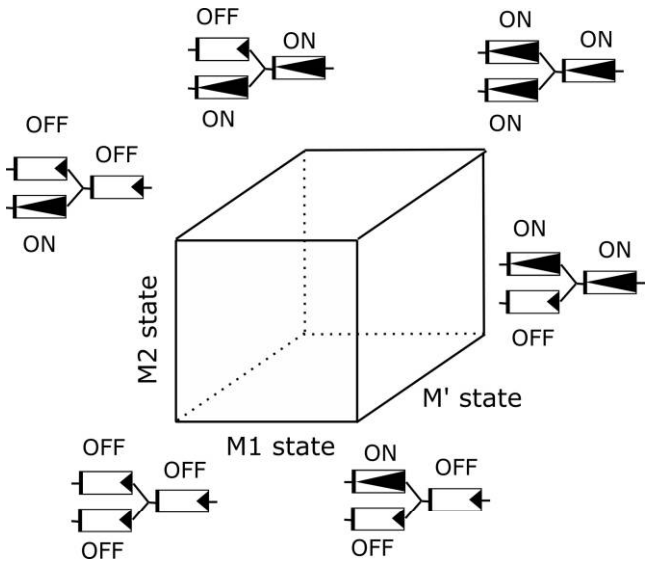


Figure 4. The state space of double-legged synaptic circuit for the case of two presynaptic neurons when the synapses are either in the ON or OFF state.

4. 1. Transmission of a pulse

The first key operating principle the double-legged synaptic circuit demonstrates, relates to the transmision of pulses between neurons. Consider the situation shown by the diagram in Figure 5a where the double-legged synaptic circuit from Figure 1 reduces to two memristors in series. Voltage source P1 represents the presynaptic neuron. When one of the memristors is OFF, no current flows, so this case is not particularly interesting. However, when both memristors are ON, a single pulse fired from the presynaptic neuron to the postsynaptic neuron, does not significantly change the state of the synapse. This can be seen by the transient simulations shown in Figure 5b and 5c. The simulation demonstrates several points. Firstly, the current does not decrease appreciably with subsequent pulses, indicating that voltage V_P is too small to alter significantly the ON state of the memristors for pulses of duration t_P. More precisely, the simulation indicates growth of the gap to less than 10 fm, which is less than a two millionth part of the maximum modelling gap. Secondly, each pulse transfers charge to the postsynaptic neuron, in fact integration of the current shows that the transferred charge is slightly below 1 pC for each pulse. It should be noted that by using oscillating pulses, the efficiency of charge transfer is reduced threefold compared to using constant voltages [3]. However, as we shall see below, the special shape of pulses allows the circuit to implement additional plasticity mechanisms.

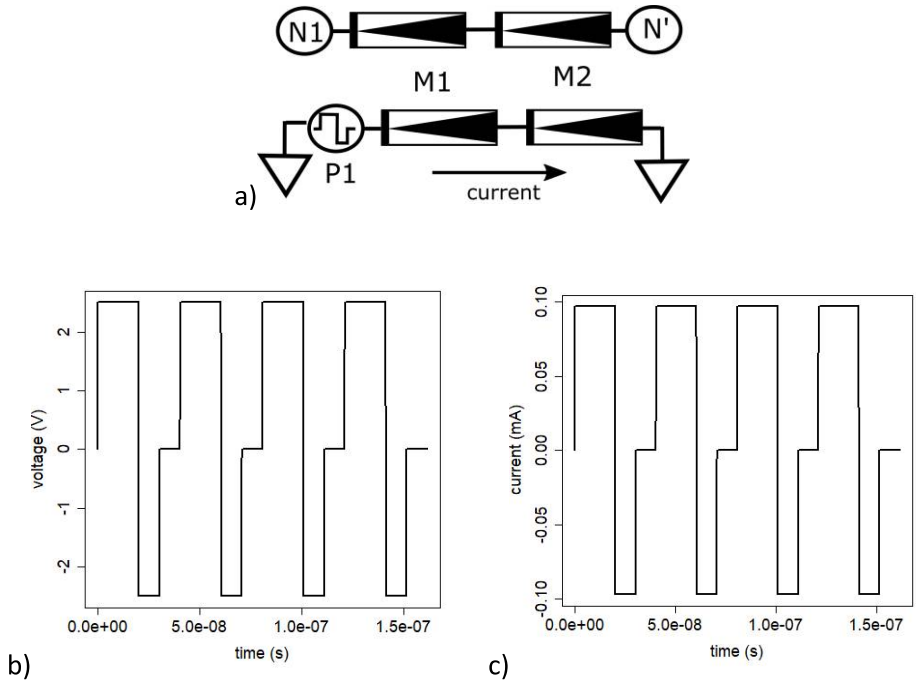


Figure 5. a) Conceptual (top) and electrical (bottom) schema for modelling transmission of a presynaptic pulse, b) voltage vs time, c) current vs. time

4.2. Input-driven plasticity

The second key operating principle this circuit demonstrates is input-driven control of the plasticity with the adaptation being modulated by the state of the blocking memristor M'. The schematic in Figure 6a, with both memristors M1 and M2 in operation, illustrate this effect. Transient simulations performed on this circuit, as shown in Figure 6b and 6c, show the situation when 4 pulses are fired from neuron P1, and 4 pulses are fired from neuron P2. From Figure 6c it can be seen that the pulses modify the gap length between the conductive filament and the electrode. This is akin to changing the synaptic plasticity of the circuit since the gap length relates directly to the strength of the connection or synaptic plasticity. Interestingly, Figure 6c shows that complete reversal of the state of the memristor can be achieved by the application of pulses, which in this case occurs after only three pulses are applied. We remark that the state of the blocking memristor stays essentially OFF, with the gap decreasing by less than 1% during the simulation and oscillating back to its maximum possible value.

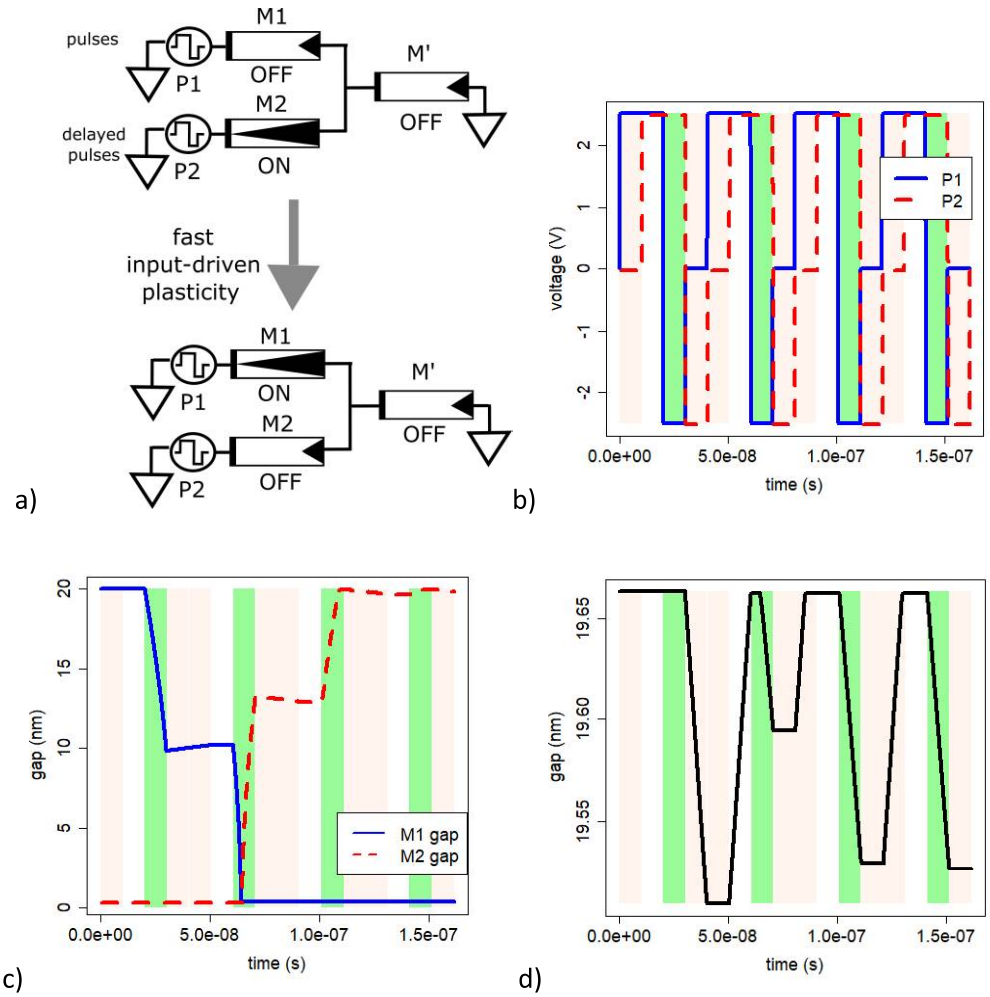
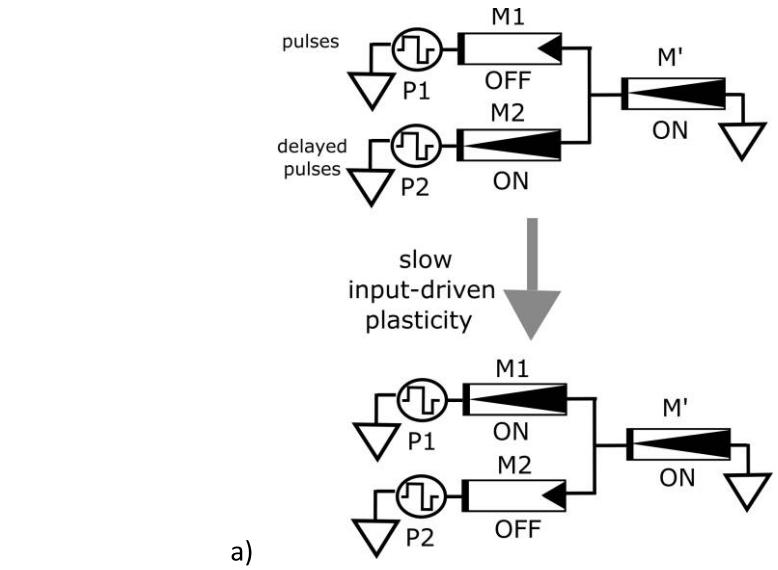
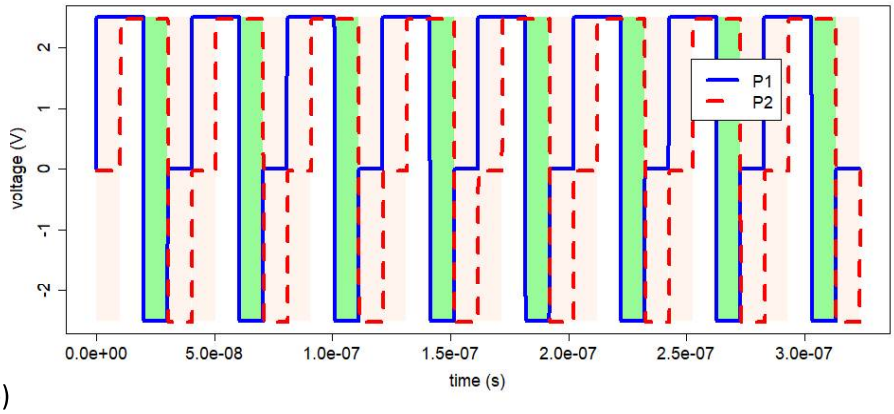


Figure 6.a) Initial and final states during fast input-driven plasticity change, b) applied voltage vs. time c) the gap between conductive filaments in memristors M1 and M2, d) the gap of the blocking memristor M'. In this this situation, as memristor M' is in the OFF state, 4 pulses are needed to reverse the synaptic state. Note: The voltage in figure b) is slightly jittered to allow for clearer presentation of voltage pulses.

The state of the blocking memristor M' plays a crucial role in regulating the speed of input-driven plasticity. In simulation in Figure 6 it was OFF. But when the blocking memristor is ON, the potential of the postsynaptic neuron directly influences the potential at the circuit's midpoint (i.e. between M1 and M'), which reduces the effect of the voltage divider between M1 and M2. The simulation is repeated in identical circumstances, as shown in Figure 7, with the exception that the blocking memristor M' is now in the ON state. In this case it can be observed by the simulations in Figure 7b and 7c, that 7 pulses are now needed to reverse the state of the memristors. In other words, if the blocking memristor M' is OFF, then the input-driven plasticity is easier to control (i.e. the synapse is learning more efficiently), whereas when M' is ON the input-driven plasticity is harder to modulate because it requires more pulses. In terms of learning, the latter configuration is more stable and less susceptible to change. Again, we note that the state of the blocking memristor did not change appreciably. In fact the gap of the blocking memristor rises from zero to only 13fm, which is less than one milllionth of the maximum model's gap.



a)



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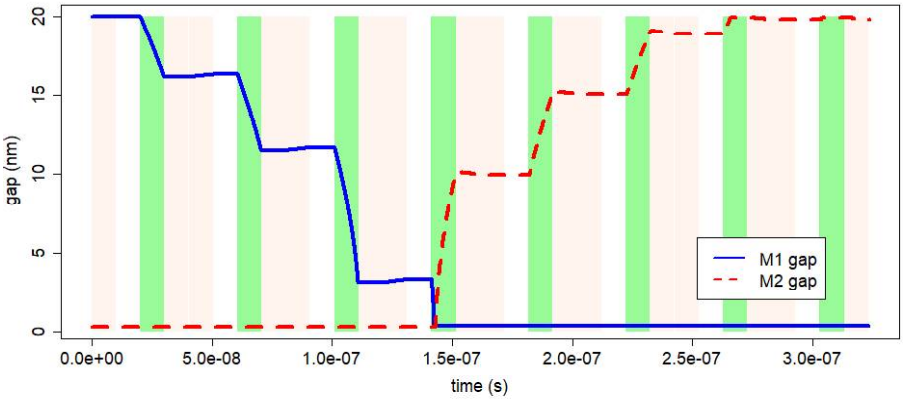

c)

Figure 7. Simulation of slow input-driven plasticity. Initial and final states of the circuit (a), voltage vs. time (b), and state variables of individual memristors (c). Note: In this this situation, as memristor M' is in the ON state, more pulses (7) are needed to reverse the synaptic state.

4.3. Spike-timing dependent plasticity

The final key operating principle demonstrated by this circuit is the interaction of presynaptic and backpropagation pulses. This case corresponds to the well-known STDP mechanism in memristors however there are some differences. Whilst it is observed that the STDP based potentiation functions in the same manner as that of single memristor synapses, depression has instead a slightly different behavior. The relevant circuit schematic for STDP potentiation is shown in Figure 8a and the resulting potentiation is shown Figure 8c.

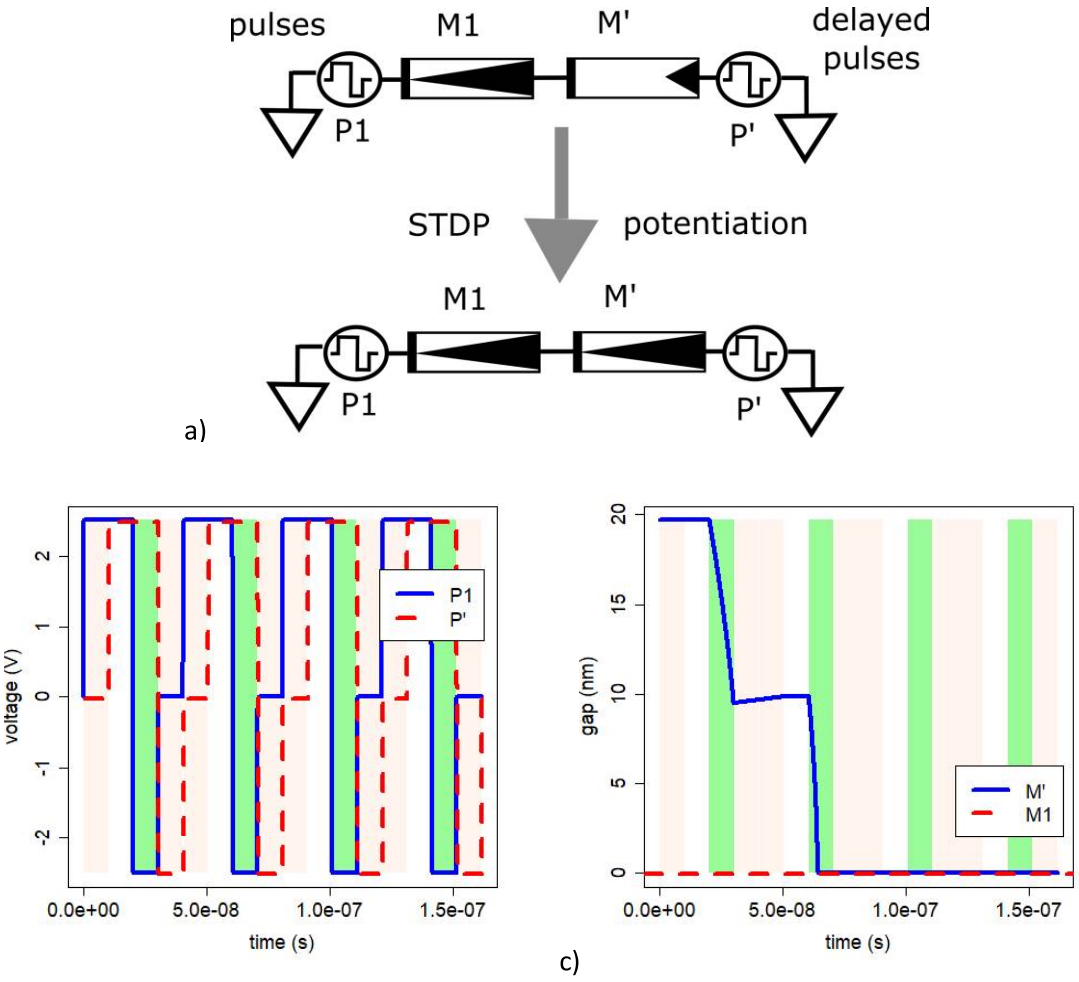

Figure 8. Simulation of STDP potentiation. Initial and final states (a), voltage vs. time (b), and time evolution of gaps in individual memristors (c).

In biological systems, STDP theory postulates that the depression of a synapse occurs when the post-synaptic backpropagation pulses precedes presynaptic by a small time offset. The circuit schematic of Figure 8a importantly demonstrates that much more subtle behaviour is possible. Consider the situation when both of memristors M1 and M‘ are exactly in the same state. The combination of preceding backpropagation pulse and following presynaptic pulse does not alter the state of the memristor circuit appreciably because the overall voltage is *exactly* divided among M1 and M‘. However, the situation changes if either M1 or M‘ are not *exactly* in the same state. In this case the memristor that has the larger gap will switch off much more quickly since a much higher potential falls across this memristor from the voltage divider. This is shown in Figure 9 for the case when M1 is not quite ON.

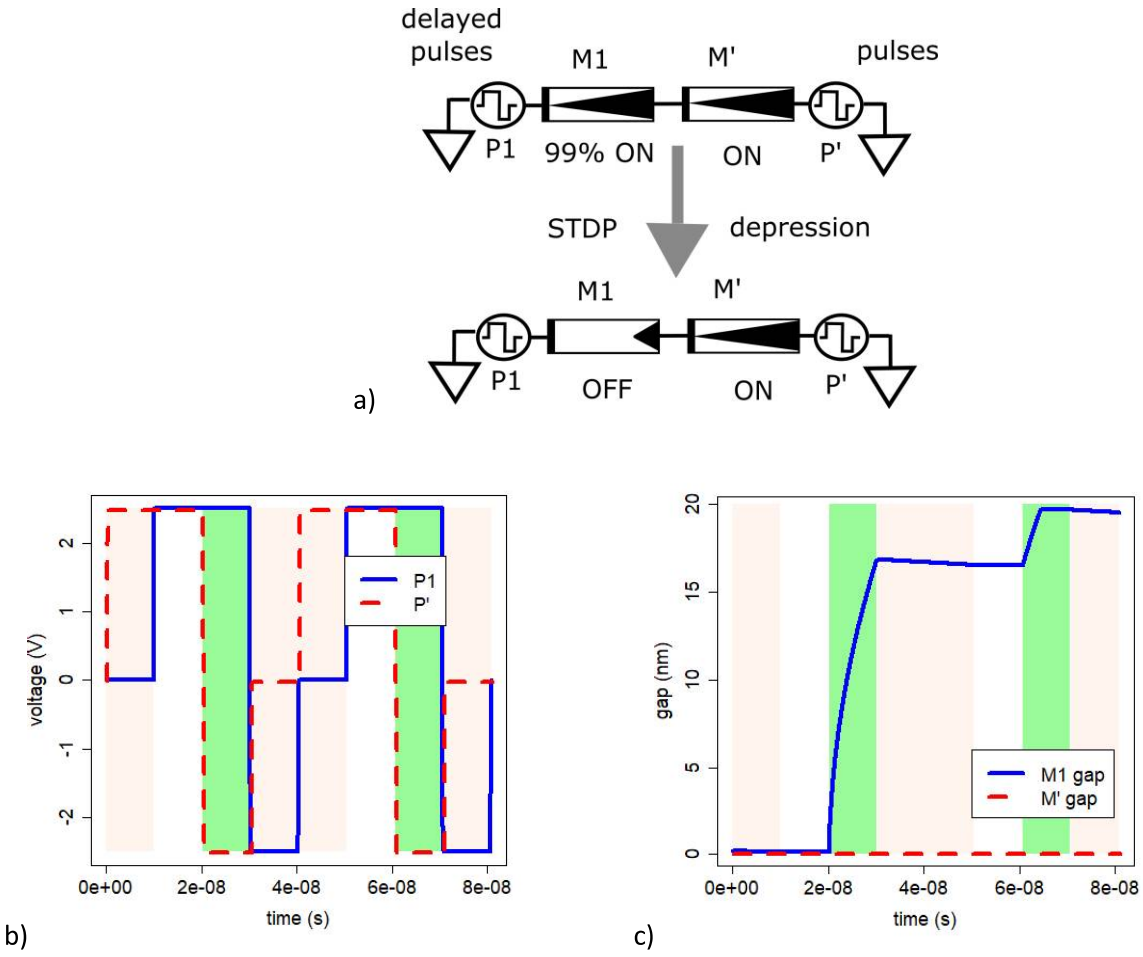

Figure 9. Simulation of STDP depression. Initial and final states (a), voltage vs. time (b), and time evolution of gaps in individual memristors (c).

Note that the analogous behavior happens if states of M1 and M’ are reversed. Then the blocking memristor M’ would RESET to the OFF state, while the synaptic memristor M1 would stay ON. Thus, STDP effects in this circuit can importantly mediate the transition of the synaptic circuit from the state allowing fast input-driven plasticity to the state exhibiting slow input-driven plasticity.

Finally we remark that by reversing polarities of memristors in Figure 1 we obtain a synaptic circuit (shown in Figure 10) that implements anti-hebbian STDP, a phenomemon observed in vivo [19].

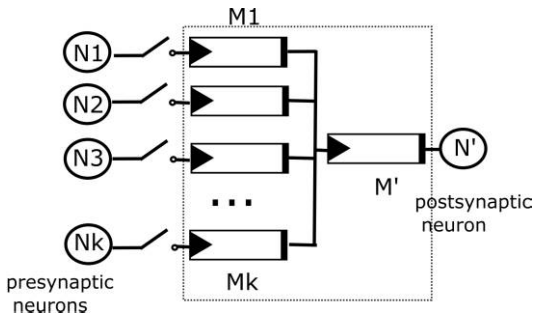

Figure 10. A passive circuit implementing anti-Hebbian STDP as well as input-driven plasticity.

5. Discussion and Conclusions

We have presented a new passive memristive circuit that provides two distinct mechanisms of plasticity of synaptic weights – STDP and input-driven plasticity. On the basis of the simulations done in the previous section it is possible to represent how STDP and input-driven plasticity alter the states of a synapse via the diagram shown in Figure 11. The key feature of this diagram is the possibility to change either the states via STDP (solid green) or input-driven adapation (dashed red). The four outer states with block memristor in ON state can be considered the stable states, where input-driven adaptation proceeds slowly. The three inner states with the block memristor M' in OFF state can be viewed as more sensitive to input-driven adaptation.

In the following we present several arguments as to why input-driven plasticity is useful in learning systems. Firstly, the state transitions achievable by a single input-driven plasticity require up to three times more STDP induced steps, thus leading to faster learning of weights. Secondly, input-driven plasticity may occur much more often than STDP. Consider the following heuristic. If there are *k* presynaptic neurons and all neurons fire independently, then there are *k(k-1)/2* ways to achieve input-driven change, each given by a pair of input terminals where the input pulses overlap. However, there are only *k* ways to achieve STDP, each identified by one presynaptic terminal. In mammalian brains, a typical value of *k* is well above 1000, thus input-driven plasticity would dwarf STDP changes [20]. Admittedly, the assumption of independence is unrealistic, since the postsynaptic neuron's activity is strongly correlated (if not completely determined by) the presynaptic spiking activity. The third agument as to why such a system is important is that in biological neurons, STDP is a relatively slow process requiring hundreds of replications, thus input-driven plasticity may prove as a more practical method of learning synaptic weights. The fact that the blocking memristor M' regulates the speed of input-driven plasticity is important. When the blocking memristor M' turns ON, it inhibits input-driven adapation by continually disturbing learnt weights and thus may guard against catastrophic forgetting, a well-known problem in neural networks [36]. Thus we may hypothesize, that in operation the input-driven plasticity would be the dominant learning mechanism with STDP serving only to regulate the speed of input-driven plasticity.

Much more research is needed to better understand the potential of the circuit. For instance, the model used for the ECM devices does not take into account the more complex plasticity observed in real ECM

devices, e.g. volatality of state [21]. More generally, the analysis of a circuits' behavior should be extended to encopass a wider variety of memristors, including VCM devices, or nonhomogenous elements. We have also not considered how such systems could be implemented. New designs compatible with VLSI are likely needed beyond previously studied spiking neurons [22,23]. Other issues that also need to examined include e.g. electroforming/initialization of the memristors, switches for isolating presynaptic neurons and regulation of neural activity.

The ultimate proof of utility of synaptic circuits with multiple plasticity rules could be provided by system-level implementation, which might obtain better learning rates on artificial intelligence problems compared to systems using STDP and its variants [24]. A simulation-based approach can be undertaken orthogonally to material science research by adopting high performance simulation platforms such as HBP SpiNNaker [25].

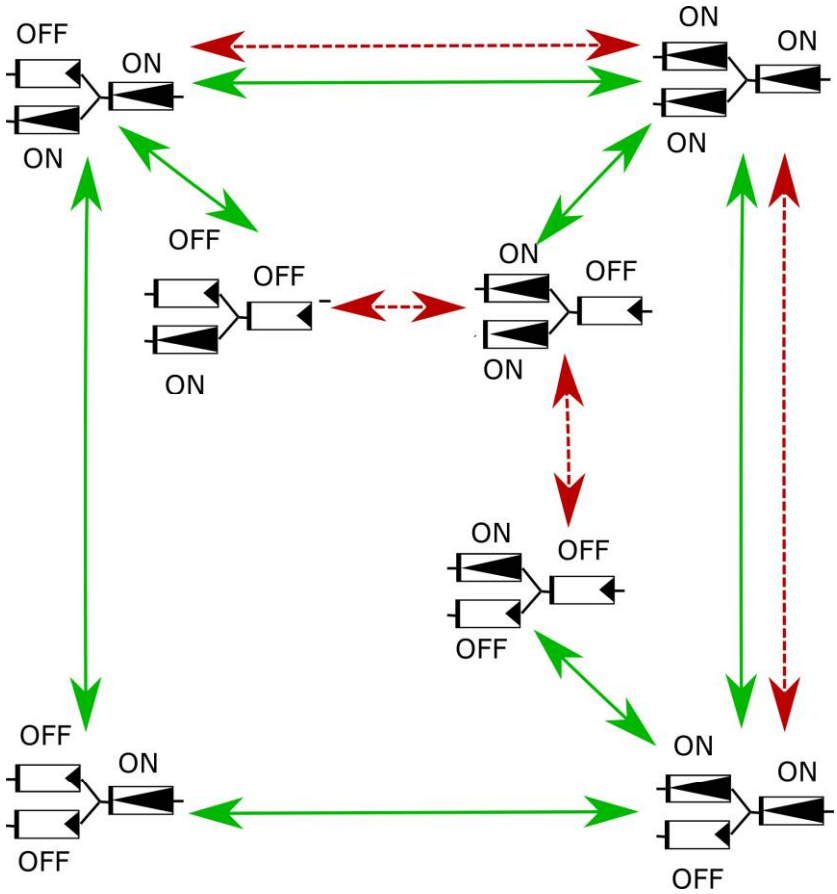

Figure 11. State changes attainable by STDP (solid green) and input-driven adapation (dashed red).

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Authors' agreement

We the undersigned declare that the manuscript entitled "Passive memristor synaptic circuits with multiple timing dependent plasticity mechanisms" is original, has not been full or partly published before, and is not currently being considered for publication elsewhere. We confirm that the manuscript has been read and approved by all named authors and that there are no other persons who satisfied the criteria for authorship but are not listed. We further confirm that the order of authors listed in the manuscript has been approved by the undersigned. We understand that the Corresponding Author is the sole contact for the editorial process. The corresponding author Ondrej Šuch is responsible for communicating with the other authors about process, submissions of revisions, and final approval of proofs.

Ondrej Šuch	Martin Klimo	Neil T. Kemp	O. Škvarek

Passive memristor synaptic circuits with multiple timing dependent plasticity mechanisms

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