THE UNIVERSITY OF HULL

DEPARTMENT OF ENGINEERING

138210 MSc Automatic Control

DISSERTATION REVIEW ON

A NEW CONTROL PERSPECTIVE ON PHASE-LOCKED LOOPS

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Abstract

The technique of phase-locked loop (PLL), an essential means for online frequency detection of incoming signal, which is widely used in our modern day's communication system. PLL is traditionally viewed as a non-linear feedback control loop that will automatically locks the adjustable frequency of a local oscillator in reference to the incoming signal.

However, the classic PLL technique has reviewed its first sign of weakness, limited convergence performance and complex in structure implementation. To overcome these weaknesses and to improve its current performance, the final outcome of the project is to bring about a better developed idea in frequency estimation compared with the present PLL technique.

A new approach known as adaptive observer method, which allowed direct estimation on frequency of an incoming signal, was recently proposed in the control literature. The underlying principle of this project is to investigate the possible use of adaptive observer method for detecting frequencies directly from any sinusoidal signals, and as well as to improve its ability in terms of better performance. Both classic PLL technique and adaptive observer method are compared through several aspects, for instance theoretical study and software simulation. However, due to adaptive observer method is significantly over-performed the PLL technique at the stage of simulation.

1. Introduction

The range of applications of Phase Locked Loops in modern technology is vast. PLLs are employed as an important module in almost every gadget used in household applications to high technology products. PLL is basically a closed loop frequency control system and its functioning is based on the phase sensitive detection of phase difference between the input and output signals of the controlled oscillator respectively.

Recently, a new approach, known as the adaptive observer method, was proposed in the control literature. The adaptive observer directly estimates the frequency of an incoming signal. Compared with the PLL, the new method has a better convergent performance and simple structure for implementation. This project aims to investigate possible use of the adaptive observer method for detecting frequency in comparison with the traditional PLL.

1.1 History of PLL

Superheterodyne receivers were widely used in the radio applications during 1930's. Edwin Howard Armstrong was the principal contributor for the design of superheterodyne receiver. But for the efficient operation of the radio receiver, a superheterodyne receiver with a number of tuned stages are required the maintenance of which was very difficult. In 1932 a team of British scientists came up with a receiver method, which could surpass the superheterodyne receiver in terms of simplicity. This new type of receiver, called the homodyne and later renamed as synchrodyne, first consisted of a local oscillator a mixer, and an audio amplifier.

The principle of Synchrodyne method consists of mixing of the input signal and the local oscillator at the same frequency and phase to produce an exact audio representation of the modulated carrier. Initially the results were encouraging, the maintenance of synchronism between the receiver signal's carrier frequency and the output of the local oscillator due to the slight drifts in the local carrier frequency.

To counteract this frequency drift, the frequency of the local oscillator is constantly compared with the input carrier frequency by a phase detector so that a correction voltage in proportional to the frequency error is generated which then would be fed back to the local oscillator to bring the frequency of the local oscillator in synchronous with the received signal frequency. This technique was already been employed in electronic servo systems even before used in the controllable oscillators. This led to the design Phase Locked Loop (PLL) system. Though initially the cost of PLL outweighed its advantage, with the advent of IC technology it was possible to incorporate to complete PLL in low-cost IC packages (Tony van Roon, 2004).

The first widespread usage of PLL(in 1940's) was in the synchronization of the horizontal and vertical sweep oscillators in television receivers to the transmitted sync pulses. Since that time electronic phase-locked loop principle was extended to many applications. For example, radio telemetry data from satellites uses narrow-band, phase-locked loop receivers to recover low level signals in the presence of noise. Other applications now include AM and FM demodulators, FSK decoders, motor speed controls, light-coupled analog isolators, robotics and radio control transmitters and receivers. The present technological products would have not existed without this technique (Tony van Roon, 2004).

1.2 Basic Structure of Phase-Locked Loop

The PLL consists of three basic functional blocks:

1. A Voltage Controlled Oscillator
2. A Phase Detector
3. A Loop Filter

4. A feedback interconnection

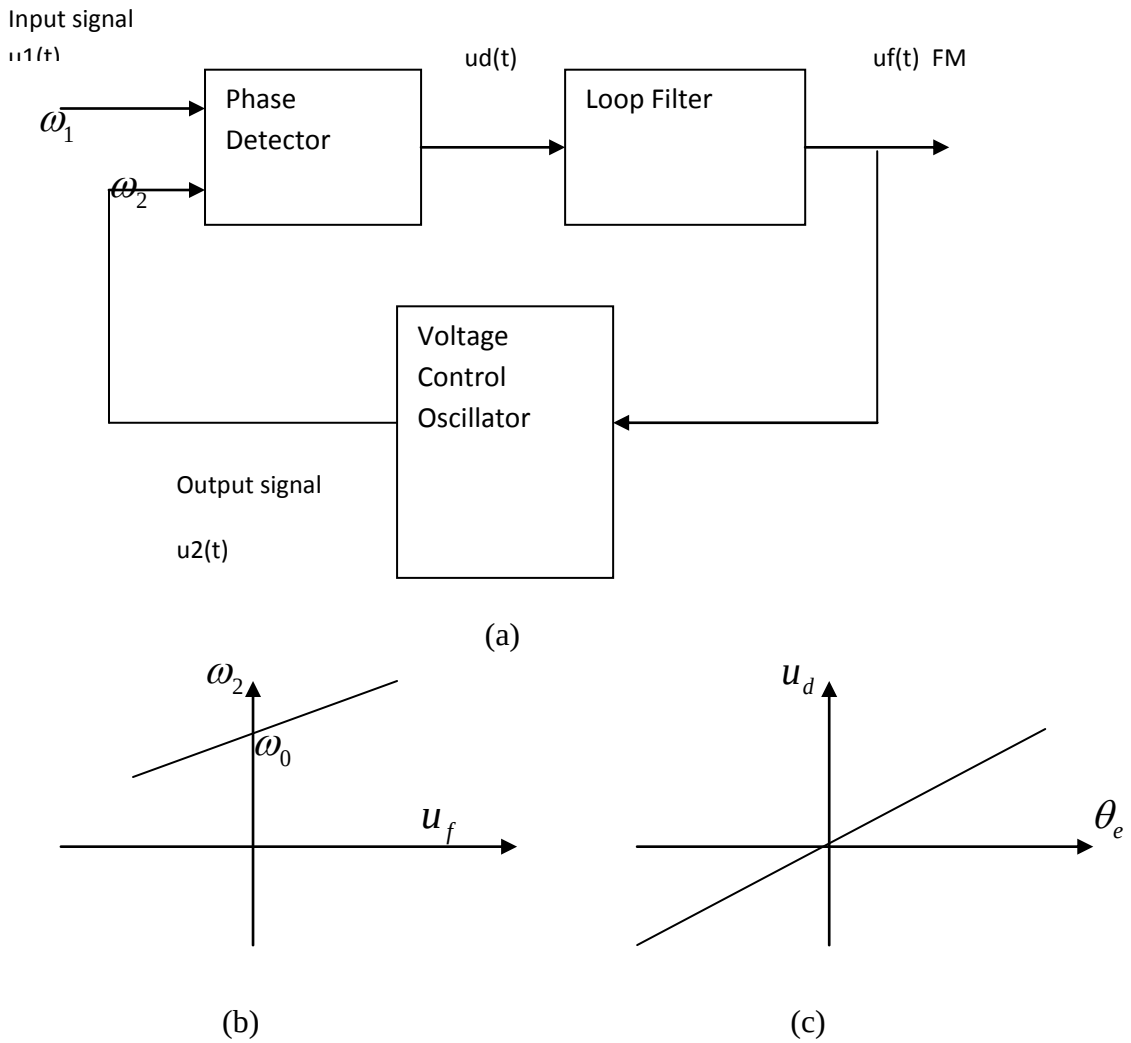


Fig: 1.1

(a) Block Diagram of the PLL (b) Transfer Function of the VCO (u_f = control voltage,

ω_2 = angular frequency of the output signal; (c) Transfer Function of the Phase Detector

$\bar{u}_d$ = average value of the phase-detector output signal; θ_e = Phase Error.

From Fig1.1(a), the Phase-Locked Loop consists of some functional blocks is described below(Best, 1997).

- **A phase detector (PD)**

This is a nonlinear device whose output contains the phase difference between the two oscillating input signals.

- **A voltage controlled oscillator (VCO)**

This is another nonlinear device, which produces an oscillation whose frequency is controlled by a lower frequency input voltage.

- **A loop filter (LF)**

While this can be omitted, resulting in what is known as a first-order PLL, it is always conceptually there since PLLs depend on some sort of low pass filtering in order to function properly.

- **A feedback interconnection**

Namely the phase detector takes as its input the reference signal and the output of the VCO. The output of the phase detector, the phase error, is used as the control voltage for the VCO. The phase error may or may not be filtered (Best, 1997).

In some PLL circuits a current-controlled oscillator (CC)) is used instead of the VCO. In this signal the output signal of the phase detector is a controlled current source rather than a voltage source. However the operating principle remains the same.

From Fig 1(a), the signals of interest within the PLL circuit are defined as follows:

- The reference (or input) signal $u_1(t)$

- The angular frequency ω_1 of the a reference signal
- The output signal $u_2(t)$ of the VCO
- The angular frequency ω_2 of the output signal
- The output signal $u_d(t)$ of the phase detector
- The output signal $u_f(t)$ of the loop filter
- The phase error θ_e ,defined as the phase difference between signals $u_1(t)$ and $u_2(t)$.

The operation of the three functional blocks is described as follows. The VCO oscillates at an angular frequency ω_2 , which is determined by the output signal u_f of the loop filter. The instantaneous values of angular frequency ω_2 is given by

$$\omega_2(t) = \omega_0 + K_0 u_f(t) \qquad (1)$$

where ω_0 is the center (angular) frequency of the VCO and K_0 is the VCO gain in $s^{-1}V^{-1}$.

The PD also referred as phase comparator – compares the phase of the output signal with the phase of the reference signal and develops an output signal $u_d(t)$ which is approximately proportional to the phase error θ_e, at least within a limited range of the latter

$$u_d(t) = K_d \theta_e \qquad (2)$$

Here K_d represents the gain of the PD. The physical unit of K_d is volts.

Fig 1(a) and 1(b) represents the equations (1) and (2).

The output signal $u_d(t)$ os the PD, consists of a DC component and a superimposed AC component. The letter is undesired and hence is cancelled by the loop filter. In most cases, a first-order, low pass filter is used as the loop filter (Best, 1997).

First we assume that the angular frequency of the input signal $u_1(t)$ is equal to the center frequency ω_0. The VCO then operates at its center frequency ω_0. Now the phase error θ_e is zero. If θ_e is zero, the output signal u_d of the PD must also be zero. Consequently, the output signal of the loop filter, u_f will also be zero. This is the condition that permits the VCO to operate at its center frequency.

If the phase error θ_e were not zero initially, the PD would develop a nonzero output signal u_d. After some delay, the loop filter would also produce a finite signal u_f. This would cause the VCO to change its operating frequency in such a way that the phase error finally vanishes.

Assuming that the frequency of the input signal is changed suddenly at time t_0 by the amount $\Delta\omega$. The phase of the input signal then starts leading the phase of the output signal. A phase error is built up and increases with time. The PD develops a signal $u_d(t)$ which also increases with time. With a delay given by the loop filter, $u_f(t)$ will also rise. This causes the VCO to increase its frequency. The phase error becomes smaller now, and after some settling time the VCO will oscillate at a frequency that is exactly the frequency of the input signal. Depending upon the efficiency of the loop filter used, the final phase error will have been reduced to zero or to finite value.

Let the VCO now operates at a frequency, which is greater than its center frequency ω_0 by an amount $\Delta\omega$. This will force the signal $u_f(t)$ to settle at a final value of $u_f = \frac{\Delta\omega}{K_0}$. If the center frequency of the input signal is frequency modulated by an arbitrary low-frequency signal, then the output of the loop filter is the ***demodulated signal.*** Thus the PLL can be used as FM detector.

Other interesting capability of the PLL is its ability to suppress noise super imposed on the input signal. Let us suppose that the input signal of the PLL is buried in noise. The PD tries to measure the phase error, between the input and the output signals. The noise at the input causes the zero crossings of the input signal $u_1(t)$ to be advanced or delayed in a stochastic manner. This causes the PD output signal $u_d(t)$ to jitter around an average value. If the corner frequency of the loop filter is low enough, almost no noise will be noticeable at the in the signal $u_f(t)$, and the VCO will operate in such a way that the phase of the signal $u_2(t)$ is equal to the average phase of the input signal $u_1(t)$. Therefore we can state that the PLL is able to detect a signal that is buried in noise.

The above applications shows that the PLL is nothing but a servo system which controls the phase of the output signal $u_2(t)$.

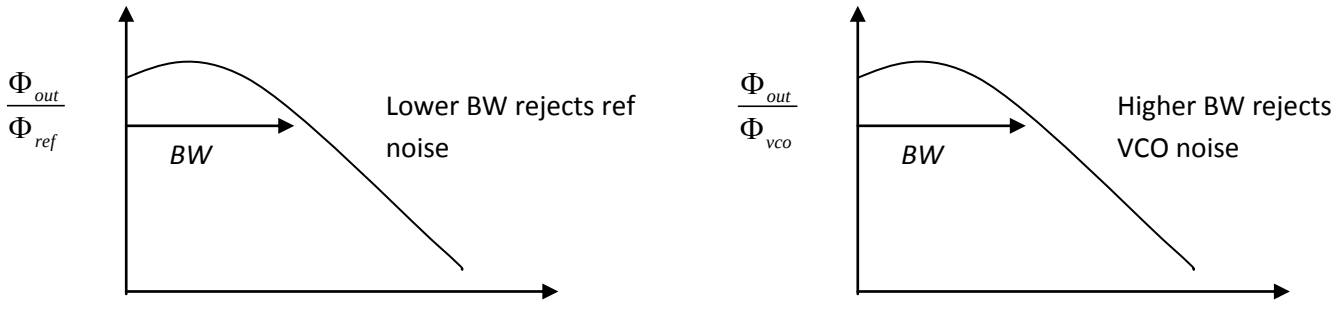
The PLL will always need to be able to track the phase of the output signal to the phase of the reference signal. A larger frequency step applied to the input signal could cause the system to "unlock". The control mechanism inherent in the PLL will them make it to get locked again (Best, 1997).

Basically two kinds of problems have to be considered in the PLL implementation.

- The PLL is initially locked. Under what conditions the PLL will will remain locked.
- The PLL is initially unlocked. Under what conditions will the PLL become locked (Best, 1997).

1.3 PLL Bandwidth

- PLL acts as a low-pass filter with respect to the reference modulation. High frequency reference jitter is rejected.
- Low frequency modulation is passed to the VCO clcok.
- PLL acts as a high-pass filter with respect to VCO jitter.
- 'Bandwidth' is the modulation frequency at which the PLL begins to lose lock with the changing reference (Best, 1997).



(a) (b)

Fig: 1.2 (a) Log (frequency); (b) Log (frequency) (Best, 1997)

2. PHASE-LOCKED LOOPS

2.1 Classifications of PLL

Different PLLs are built from different building blocks. There are four different types of PLLs.

- The Linear PLL (LPLL)
- The Digital PLL (DPLL)
- The All-Digital PLL (ADPLL)
- The Software PLL (SPLL)

2.1.1 The Linear PLL (LPLL)

From Fig 2.1 linear PLLs, the four quadrant multiplier is used as a phase detector. In most cases $u_1(t)$ is a sine wave with angular frequency ω_1, where as the output signal $u_2(t)$ is a symmetrical square wave with angular frequency ω_2. In the locked state the two frequencies are equal. The output signal $u_d(t)$ of the phase detector then consists of a number of terms. The first of them is a DC component and is roughly proportional to the phase error θ_e, the remaining components are AC components having frequencies of $2\omega_1$, $4\omega_1$, ….. Because these higher frequencies are unwanted signals, they are filtered out by the loop filter. Because the loop filter must pass the lower frequencies and suppress higher frequencies, it must be a low pass filter. In LPLL designs, a first-order low pass filter is used.

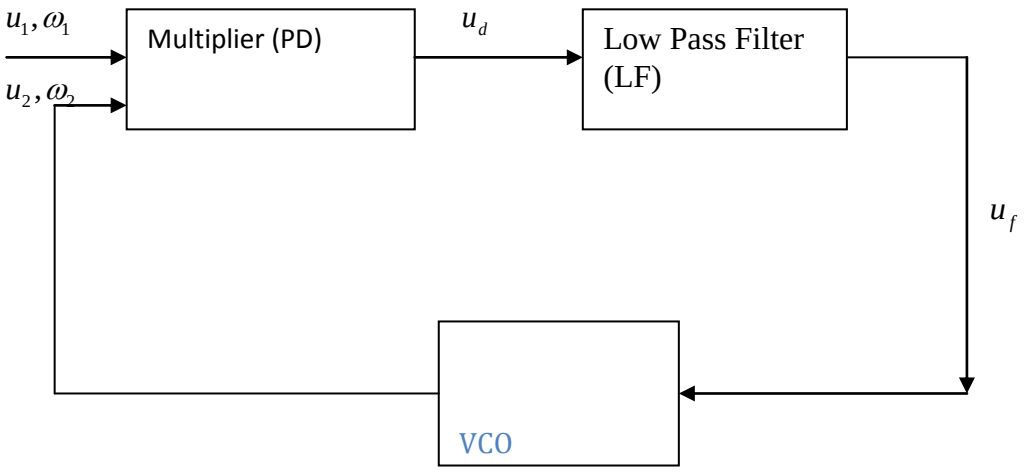


Fig: 2.1 Linear Phase-Locked Loop (Best, 1997)

Most applications of LPLLs are in the field of communications. LPLLs are widely used in the AM and FM receivers . The LPLLs are also used in the television systems. In a TV receiver, one LPLL is used for horizontal synchronization. Anaother PLL serves for vertical synchronization and still another reconstructs the color subcarrier. The LPLL found wide applications in the field of satellite communication. Here the LPLL's capabilities of extracting a signal from noise have proved very successful (Best, 1997).

2.1.2 The Digital PLL (DPLL)

The classical DPLL is actually a hybrid system built from analog and digital function blocks. The only part of the DPLL that is really digital is the Phase Detector. In many aspects the DPLL performs similar to the LPLL, so some parts of the LPLL theory can be adopted.

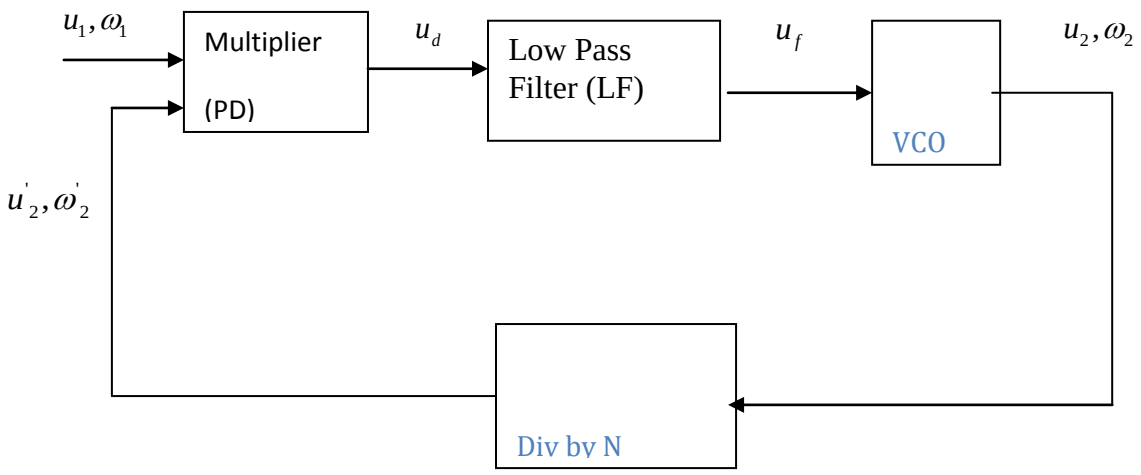


Fig: 2.2 Digital Phase-Locked Loop (Best, 1997)

Like the LPLL, it consists of the three known functional blocks ***phase detector, loop filter*** and ***voltage controlled oscillator*.** From Fig 2.2, In many DPLL applications a divide-by-N counter is inserted between VCO and phase detector. When such a counter is used the VCO generates a frequency which is N times the reference frequency. The loop filters used in DPLLs are the same as those used in the LPLLs.

The applications of the DPLL are so widespread. DPLLs are used in the frequency synthesis, clock signal recovery and motor speed control (Best, 1997).

2.1.3 The All-Digital PLL

The classical DPLL is a semi-analog circuit. Because it always needs a couple of external components, its key parameters will vary because of parts spread. Even worse, the center frequency of DPLL is influenced by parasitic capacitors on the DPLL chip. Its variations can be so large. Its variations can be so large that trimming can become necessary in critical applications.

- **Classical Digital Phase-Locked Loop (CDPLL)**

The next architecture is classical digital phase-locked loop (CDPLL), as shown in Fig 2.2(a), was developed in the 1970's which contained both analogue and digital parts. The distinct difference from APLL is the phase detector, which was now digital and it work using binary values. It is not a digital sampled data system as the term digital would imply to control theorists. Instead, it is an APLL implemented with a digital phase detector. In this case, the output of the digital phase detector is seen as a continuous time voltage. On the other hand, both VCO and analogue loop filter are remained as analogue devices. This version of PLL is also known to as "Hybrid phase-locked loop", where one or more loop components are digitally implemented (Best, 1997).

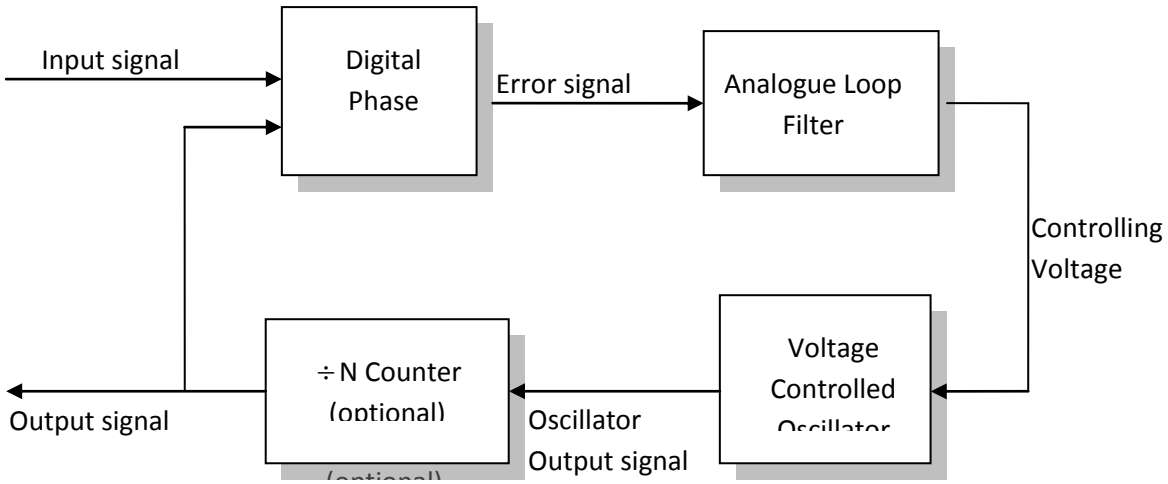


Figure 2.2(a): Fundamental blocks of classical digital phase-locked loop (Best, 1997)

- **All Digital Phase-Locked Loop (ADPLL)**

The ADPLL or all digital phase-locked loop came along a few years after the CDPLL and was an exclusive implementation from a digital blocks, thus all other passive components such as resistors and capacitors are rejected in this design. The advance of ADPLL is having a very small chip size due to inexistence of any passive components. On the other hand, ADPLL has their own algorithm and protection, thus they are complex in implementation and difficult in selling.

The major difference between ADPLL and CDPLL is in the use of the digital phase detector. For some case in ADPLL, the phase detector used to generate analogue voltages in continuous time and its output is considered a digital quantity, either pulses or multi-bit values. Moreover, ADPLL replaces the analogue loop filter with phase detector and the VCO with a digital controlled oscillator.

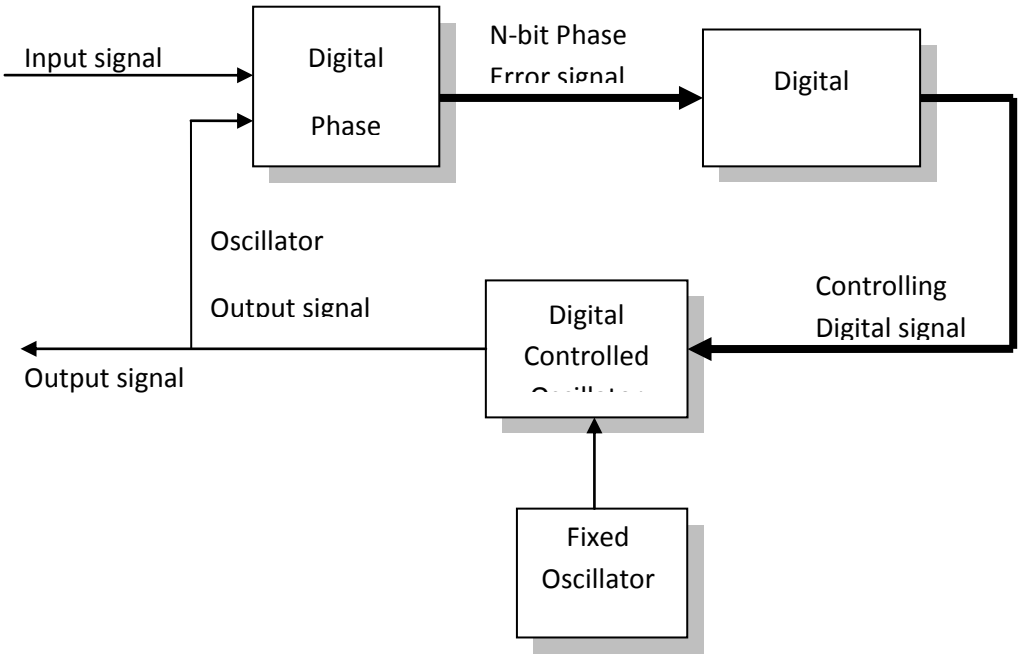


Fig 2.3: First version of all digital phase-locked loop (Best, 1997)

There are two types of ADPLL; Fig 2.3 shows the building blocks of first version of ADPLL which is also known to as charge-pump phase-locked loop. It uses its digital phase detector to produces samples of phase error in an n-bit value. This value is then fed to the digital loop filter which the devices will adjusts the frequency of the digital controlled oscillator.

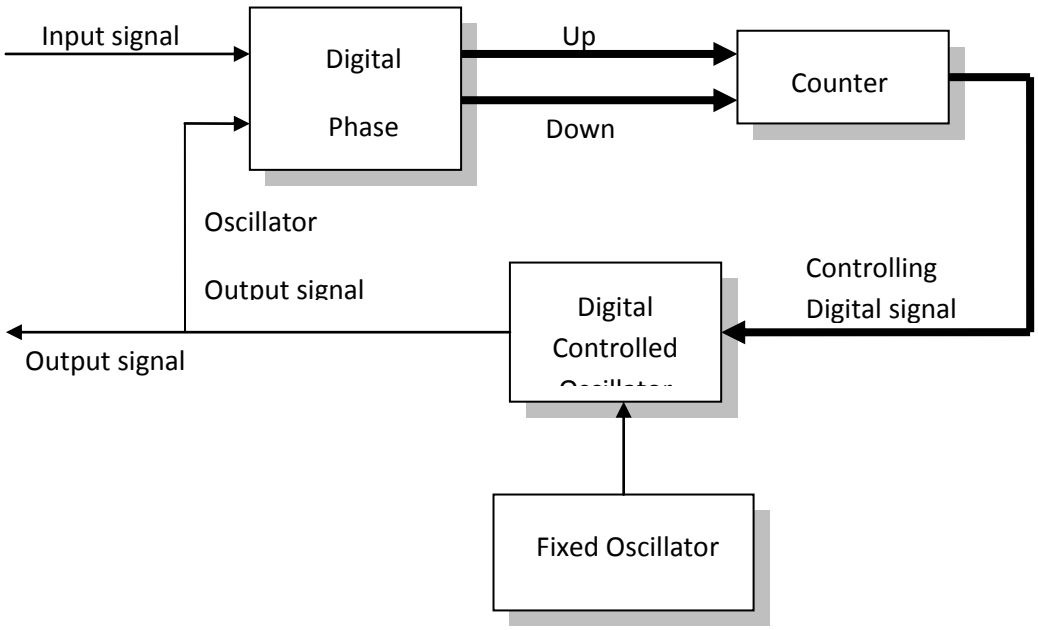


Fig 2.4: Second version of all digital phase-locked loop (Best, 1997)

Mean while for the second version of ADPLL, as shown in Fig 2.4, it operates on a difference principle than the first version ADPLL, such that the digital phase detector generates pulses that go into count up or count down inputs of the counter which used to replaced the digital loop filter. The counter then enables and adjusts the frequency of the digital controlled oscillator.

2.1.4 Software Phase-Locked Loop (SPLL)

The most recent PLL type available is called software phase-locked loop (SPLL) and with its block diagram shown in Fig 2.5. With better technologies available, PLL can now be implemented by software and all the functions required by the system are performed by the software. Whenever the data can be sampled at a rate substantially faster than the loop centre frequency, the entire loop operation can be implemented using software. As a result, it has the advantage of flexibility. Moreover, any type of PLL model can be implemented in software, if only the sample rate is high enough. Software loops have a lot in common with simulation, one key difference is that the software loops deal with real data. SPLL may operate on the data in real time, but can also be used in the post processing of measured data. However, one cautionary note is that certain operations which are highly effective in hardware, such as limiters which have a lot of high frequency content, create real sampling issues for software loops (Best, 1997).

In the age of microcontrollers and DSPs it is an obvious idea to implement a PLL system by software. When doing so the functions of the PLL are performed by software. The designer realizing software PLL trades electronic components for microseconds of computation time. As the parts count for the hardware PLL increases with the level of sophistication, the number of computer instructions rises with the complexity of the required PLL algorithms. (Best, 1997)

Of course the SPLL can compete with a hardware solution only if the required algorithms are executing fast enough on the hardware platform which is used to run the program. If a given algorithms runs too slowly on a relatively cheap microcontroller and the designer is forced to resort to more powerful hardware, a price trade-off also come into play. The high speed and low cost of available PLL ICs makes it difficult for the SPLL to compete with

its hardware counterpart. Nevertheless, SPLLs can offer particular advantages, especially when computing power is already available.

When comparing SPLLs with hardware PLLs, firstly it should be recognized that an LPLL or a DPLL actually is an analog computer which continuously performs some arithmetic operations. When a compulter algorithms has to over that job, it must replace these continuous operations by a discrete-time process. The signals of hardware PLLs contains a fundamental frequency, which can be equal to its reference frequency f_1 or twice that value. According to the sampling theorem, the algorithm of the SPLL must be executed two or even four times in each cycle of the reference signal. If the reference frequency is a modest 100kHz, the algorithm must execute a minimum of 200,000 times per second, which leaves not more than 5 μ sec for one pass through.

Today's microcontrollers easily work with clock frequencies of 200MHz or more, which says that one machine cycle is 5ns or less. The clock frequency of some newer 64-bit μCs even exceed 500 MHz. For most microcontrollers, however, one instruction needs more – often much more – than one machine cycle to execute. There is a risk, therefore, that the microcontrollers on the lower end of the price scale fail to deliver the required computational throughput. Using DSPs instead brings us a big step forward, because they not only are fast with respect to clock frequency, but also offer Harvard-Plus and pipeline architecture. Harvard architecture means that the DSP has physically separated data and program memories, hence can fetch instructions and data within the same instruction cycle. In even more sophisticated DSPs, the machine can fetch one instruction and several data words at the same time. The term "PIPELINE" implies that the arithmetic and logic units of the machine are fully decoupled, so that the DSP chip is able, for example, to perform one instruction fetch, some operand fetches (data fetches), one or more floating point additions, one or more floating multiplications, one or more decoding of instructions, one or more register-to-register operations and perhaps even more in one single machine cycle. This greatly enhances computational throughput but results in higher cost (Best, 1997).

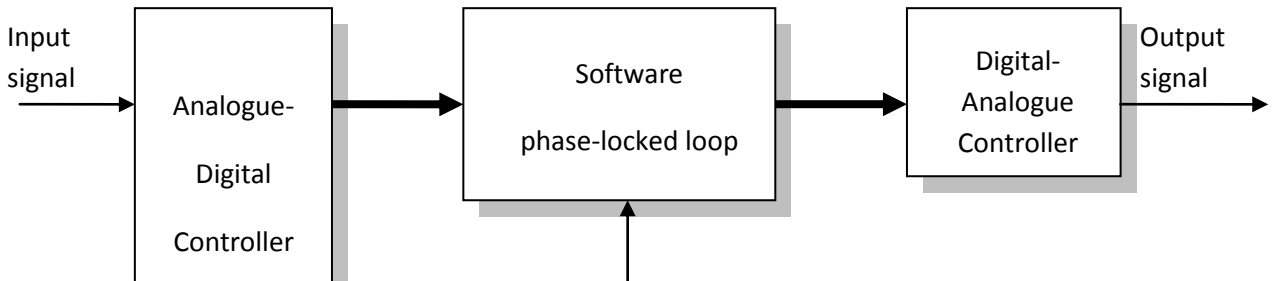


Fig 2.5: Conceptual block diagram of software phase-locked loop (Best, 1997)

An example of SPLL blocks diagram that enable clock or data recovery is shown in Figure 2.6. The heuristic loop uses a zero crossing detector on the sampled input and the effective sample rate is derived from the average bit zero crossing rates.

The all-digital PLL does away with these analog circuitry problems. In contrast to the DPLL, it is entirely digital system. All the functional blocks of the PLL i.e. Phase Detector, VCO and Loop Filter are digital systems (Lindse, 1981).

Because of the availability of low-cost ADPLL ICs this type of PLL can replace the classical DPLL in many applications today. The ADPLL is mainly used in the field of digital communications. This system can be found in FSK decoders (Best, 1997).

2.2 Description on Loop Components

According to section 2.1, there are several types of PLL models available nowadays. However, the PLL model which proposed to implement is the CDPLL (see Fig 2.2) system rather than the APLL (see Fig 2.1) or other higher level PLL models with specialised design techniques. Reasons for selecting CDPLL model are because of:

- A system is required to operate under normal conditions, to have a simple structure and can be analyzed using continuous time linear feedback theory. Thus other higher PLL design such as ADPLL or SPLL, which with specifically design technique and complex in analysis are not to be considered. (Skelton, 1998).

- Although APLL satisfies the first specification, there are a variety of reasons to use digital circuitry to implement PLL system rather than the classic analogue technique. For example, a CDPLL has better performance than APLL in terms of lower signal-to-noise ratio (SNR), less affected by signal distortion by using square waves, very high frequencies (multiple Gigahertz) implementation with very reliable logic and better pull-in range. Beside that, the digital phase detector has the advantage of having low frequency response of linear rather than sinusoidal detector (mixing).
- Moreover, in order to obtain better accuracy in comparison between results from software simulation and prototyping, thus using similar PLL model for both implementations are essential. Moreover, built-in CDPLL IC chip is commonly manufactured and easily to obtain compared to others.

Description on loop components used and the design method used for CDPLL system are to be discussed on the following sections.

2.3 Applications of PLL

An incomplete list of specific tasks accomplished by PLLs includes carrier recovery, clock recovery, tracking filters, frequency and phase demodulations, phase modulation, frequency synthesis and clock synchronization. PLLs find themselves into a huge set of applications, from radio and television, to virtually every type of communications (wireless, telecom and datacom), to virtually all type of storage device, to noise cancellers and the like (Best, 1997).

2.4 Linear Analysis Methods of Classical PLLs

The PLL model in the below given Fig 2.6 is a closed-loop feedback system.

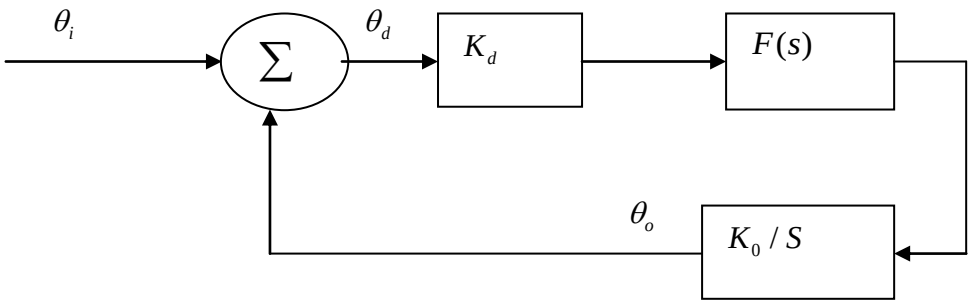


Fig: 2.6 Conceptual block diagram of linear PLL (Abramovitch, 1988)

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This is derived from the sine detector loop by assuming that the phase error is small and thus $\sin(\theta) = \theta$. This is the model with which most analyses of phase-locked loops are done.

The complimentary sensitivity transfer function from reference phase input VCO phase output, T(s), can be obtained as

$$T(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_d F(s) K_v / s}{1 + K_d F(s) K_v / s}$$

$$= \frac{K_d K_v F(s)}{s + K_d K_v F(s)}$$

Similarly, the sensitivity transfer function from the reference phase input to the phase error, S(s) is

$$S(s) = \frac{\theta_d(s)}{\theta_i(s)} = \frac{1}{1 + K_d F(s) K_v / s}$$

$$= \frac{s}{s + K_d K_v F(s)}$$

Among the basic properties of interest in this transfer function are the loop stability, order and the system type.

The order of the PLL system must be obvious from the denominator of T(s).

The stability of the system can be determined by a variety of classical methods including root locus, Bode plots, Nyquist plots and Nichols charts. (Abramovitch, 1988)

2.5 The Hold Range

The hold range $\Delta\omega_H$, is defined as that frequency range at which the PLL is able to statically maintain phase tracking. (Hsieh, 1996)It is determined by calculating the frequency offset at the reference input that causes the phase error to be beyond the range of linear analysis. For a multiplying or XOR phase detector, This phase error is $\pi/2$ (Abramovitch, 1988).

2.6 The Lock Range

The lock range, $\Delta\omega_L$, is defined as that frequency rage within which the PLL locks within one single-beat note between the reference frequency and output frequency. Abramovitch, (1988) The lock range must be calculated from a non-linear equation, but there are several useful approximations that are made.

2.7 The Pull-In and Pull-Out Range

The pull-in range, $\Delta\omega_P$, is defined as the frequency range in which the PLL will always become locked. The pull-out range, $\Delta\omega_{PO}$, is defined as the limit of dynamic stability for the PLL (Abramovitch, 1988).

2.8 The Steady State Error

Steady state errors can be obtained from the linear analysis via use of the Final Value Theorem, i.e.

$$\lim_{t\to\infty}\theta_d(t) = \lim_{s\to 0} s\theta_d(s) = \lim_{s\to 0} s\theta_i(s)S(s)$$

2.9 System Terminology

The lock range, $\omega_{L,}$ is the range of frequencies about VCO quiescent frequency, ω_q for which the system remains locked once it has captured the signal ($\omega_{in} = \omega_o$).

The capture range, ω_c, is defined to be range of frequencies for which an unlocked loop will acquire lock on the input signal, ω_{in}. A general approximation,

If $F(s) = 1$ (no loop filter), then $\omega_c \approx \omega_L$

If $F(s) = \dfrac{1}{\dfrac{s}{\omega_c} + 1}$ (low-pass RC filter), then $\omega_c < \omega_L$

Lock and Capture range relationships are shown graphically in Fig 2.7.

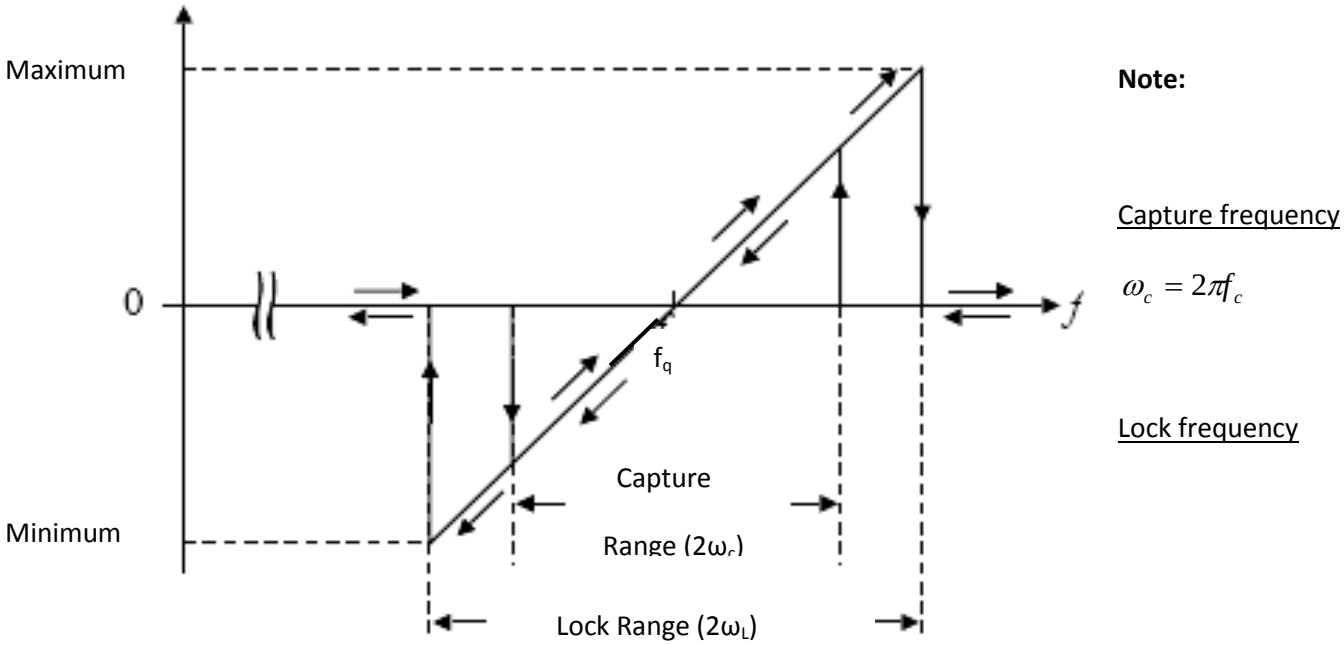


Fig 2.7: Lock and Capture range relationships (Best, 1997)

2.10 Digital Phase Detector: Exclusive OR gate (XOR)

Digital phase detector is defined to be a device that compares the phase at each input and generates an error signal $V_d(t)$, which proportional to the of phase difference between $V_{in}(t)$ and $V_o(t)$ inputs. There are several types of digital phase detector designs (e.g. two state phase detector, Hogge phase detector, Alexander (bang-bang) phase detector, phase-frequency detector, linear clock phase detector, sampled and hold detector), which are shown from Fig 2.8-2.10. However, the simplest design among all digital phase detectors is by using an Exclusive-OR (XOR) gate. One advantage of such a phase detector is that the loop gain is independent of input signal amplitude. Furthermore, the XOR phase detector is linear in phase over some region, thus linear analysis can be accurately applied. However, the disadvantage is that the linearity of the baseband response is affected by the relative duty cycle of the input signal $V_{in}(t)$ and VCO output signal $V_o(t)$. Therefore, in order to maximize the lock range, a 50% duty cycle of the input signal is preferred.

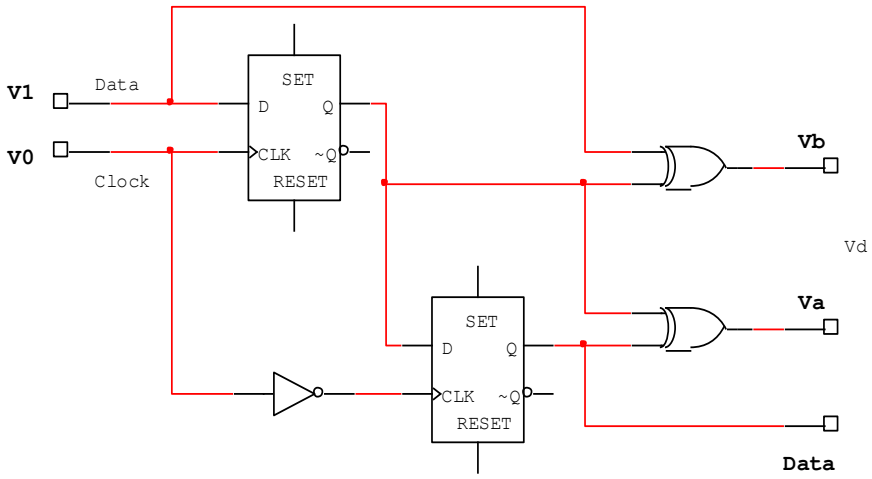


Fig 2.8: Linear clock phase detector (Best, 1997)

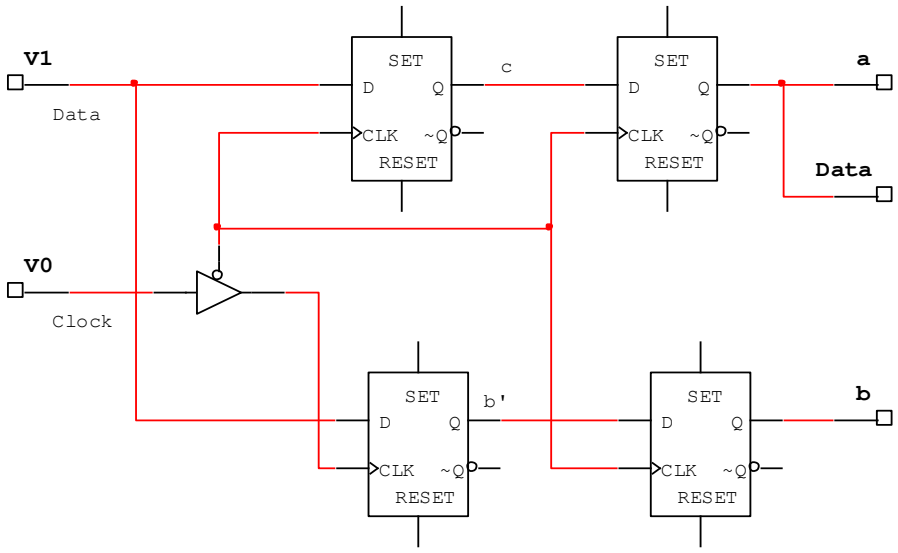


Fig.2.9: Alexander (bang-bang) phase detector (Best, 1997)

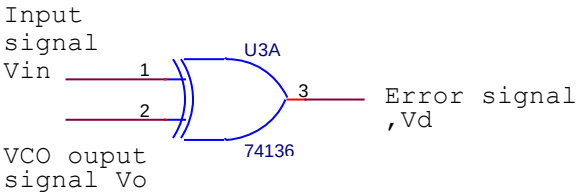


Fig 2.10: XOR phase detector (Best, 1997)

The output signal from the XOR phase detector can be obtained through

$$V_d(t) = K_d\theta_e = K_d(\theta_{in} - \theta_o) \qquad (2\text{-}1)$$

where θ_e is the phase different between θ_{in} (phase of $V_{in}(t)$) and θ_o (phase of $V_o(t)$), which can be seen in the example given in Fig 2.10. The logical principle of the XOR phase detector works is based on XOR truth table, which is shown in Table 1. An XOR gate will gives high output when the signals are of opposite sign and a low output when they are of the same sign. When the signals are in phase, the output is 0. While if they are in anti-phase or with phase difference π radians, thus the output is a constant high value of 1. The XOR phase detector works as if the two

signals are of different frequency, the phase relation will change continuously and the output will be a series of pulses. The effect on the VCO will be to change the frequency in either one direction then another way, but in general the changes in the proper direction will be a bit longer and thus raising the VCO frequency to the input frequency. Then, the phase relations are stable and the delay is to provide the average voltage necessary to the VCO. Although the two input signals are brought to the same frequency, not necessarily to the same phase. Nevertheless, the phase difference is constant (Halkias, 1977).

Exclusive OR (XOR)		
$V_{in}(t)$	$V_o(t)$	$V_d(t)$
0	0	0
0	1	1
1	0	1
1	1	0

Table 2.1. Truth table of XOR phase detector (Best, 1997)

The analysis of XOR phase detector is shown in Fig 2.11 and Fig 2.12. Basically, XOR response can be split into 2X term and residual term, but the average of the residual term "baseband" is the parameter to be taken into account. In Fig 10, a phase shift of π/2 between the input signal $V_{in}(t)$ and with the VCO output signal $V_o(t)$ produces a residual of zero value.

$V_{in}(t)$

$V_o(t)$

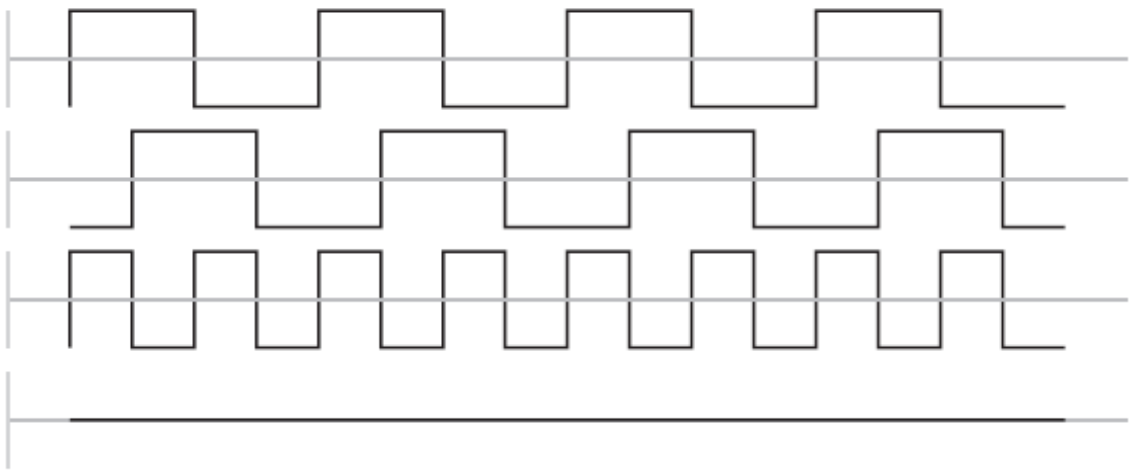


Fig 2.11: Phase shift of $\pi/2$ (Best, 1997)

Meanwhile in Fig 2.12, a relative phase shift of π/4 between input signal $V_{in}(t)$ and with the VCO output signal $V_o(t)$, thus produces a nonzero residual. Output amplitude of error signal $V_d(t)$ is either 1V or 0V due to the behaviour of a XOR phase detector which is fundamentally a logic gate characteristic, as explained in Table 2.1.

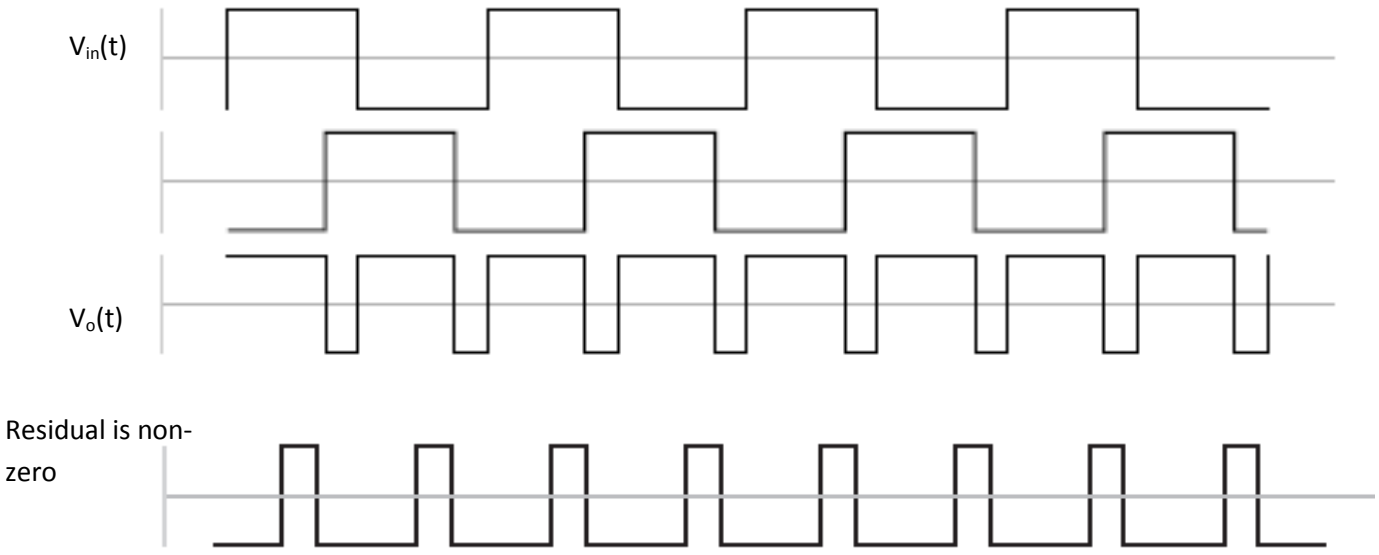


Fig 2.12: θ_e, phase shift of π/4 (Best, 1997)

Fig 2.13 shows the relation between the inputs phase difference at XOR phase detector against the average output voltage (V_{dd}) at output of loop filter.

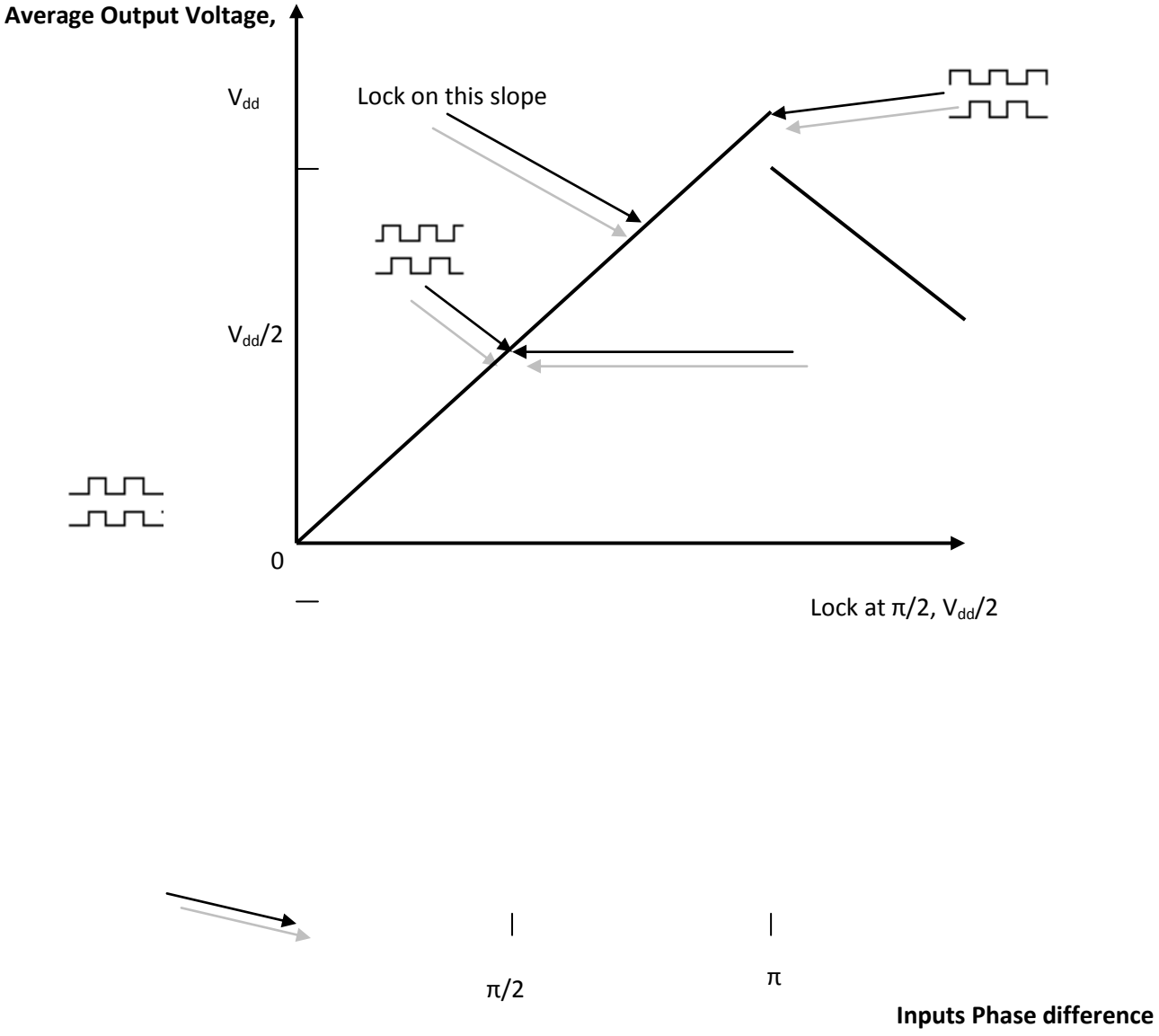


Fig 2.13: XOR phase detector characteristic at loop filter (Best, 1997)

K_d is the gain of the digital phase detector and the units of K_d are volts/radians or simply volts assuming all phase shifts are in radians and not degrees. At a constant phase shift of $\pi/2$, the

output voltage at low-pass filter will be $V_{dd}/2$ which produced a zero residual, thus the system is said to be 'locked' (output displaying frequency at the input). Since XOR phase detector with phase range of π, thus the gain is:

$$K_d = V_{dd}/\pi \qquad (2\text{-}2)$$

For example in physical design, if voltage supply (V_{dd}) applied to the IC is 5V with equation (2-2) is to be applied to calculate the gain K_d, thus K_d =1.592 V/radian.

2.11 Analogue Loop Filter: Low-pass RC Filter

Loop filter is defined to be a component that eliminates unwanted signals which usually high frequency signals in the PLL. Therefore, in order to filter high frequency components from error signal $V_d(t)$, a low-pass filter is usually implemented. There are three types of loop filters commonly presented in PLL theory: passive filter (see Fig 2.14), active filter (see Fig 2.15), and PI (Proportional + integral) filter (see Fig 2.16). Perhaps the most important design part of the feedback loop is the loop filter because the selection of the loop filter is a very important decision since it determines the behaviour and characteristic of the PLL under various conditions, such as lock-in range, pull-in range and hold range. However, a vast majority of phase-locked loops are second order and their loop filters are typically first order.

A first-order passive low-pass RC filter, also known as to be Lag low-pass filter, will be concerned in the CDPLL design. This is because a simpler low-pass RC filter will be sufficient to complete the filtering task; its schematic circuit is shown in Fig 2.17.

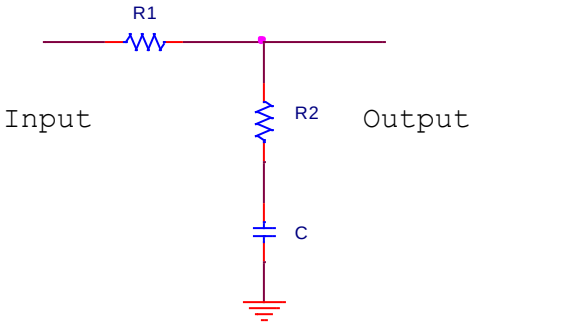


Fig 2.14: Second order passive filter

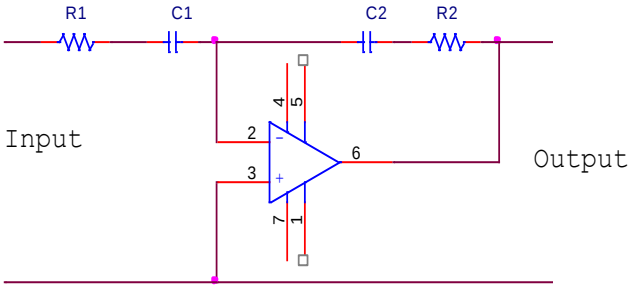


Fig 2.15: Second order active filter

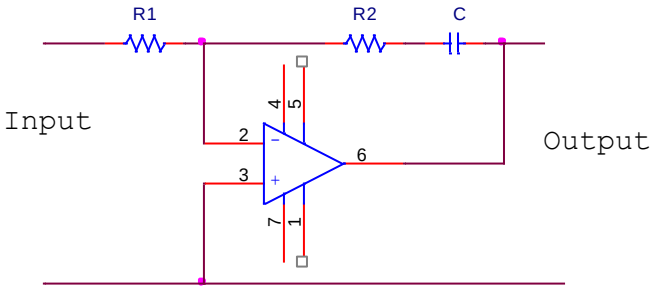


Fig 2.16: Second order PI filter

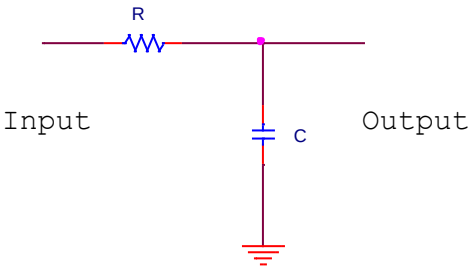


Fig 2.17: First order passive low-pass RC filter

In order to be able to understand the principle of first-order low-pass RC filter used, analysis of the filter is carefully considered below. The RC filter belongs to the first-order filter with only one resistor and one capacitor.

While, the closed-loop voltage transfer function of the filter is:

$$F(s) = \frac{1}{s(RC)+1} = \frac{1}{\frac{s}{\omega_c}+1} \qquad (2\text{-}3)$$

where, Cut-off angular frequency, $\omega_c = \frac{1}{RC}$ (2-4)

Cut-off frequency, $f_c = \frac{1}{2\pi(RC)}$ (2-5)

$|F(j\omega)| = K_f$ is known as the filter gain which an ideal (maximum) value of K_f =1 for a first-order RC low-pass filter. However in physical design, pass and stop bands are not clearly defined. Therefore, $|F(j\omega)|$ varies continuously from its maximum toward zero. As a result, the cut-off angular frequency ω_c at which $|F(j\omega)|$ is reduced to $0.7K_f$ as its maximum value, this is shown in Fig.2.18.

|F(jω)|

K_f

0.7 K_f

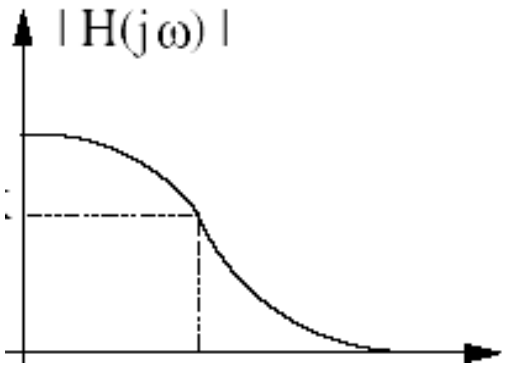


Fig 2.18: Cut-off frequency, ω_c (or f_c) (Best, 1997)

The RC low-pass filter will only allows ω_f usually equal to or below the cut-off frequency $\omega_c (\omega_f \leq \omega_c)$, so that the voltage control signal $V_f(t)$ to the VCO is relatively steady. Generally speaking, a slower PLL responds is preferable in order to provide a flywheel action that damps out noise and unwanted variations.

2.12 Voltage Controlled Oscillator (VCO)

Voltage controlled oscillator or knows as VCO, is defined as a device which produces a periodic signal with frequency changes based on the control signal $V_f(t)$ applied from the low-pass filter. However, VCO is the main contribution of noise in PLL design. There are several VCO architectures available, for instances ring oscillator, relaxation oscillator, LC-tank oscillator and resonant oscillator. Ring oscillator and resonant oscillator are common architectures of VCO in PLL, as shown Fig 2.19 below:

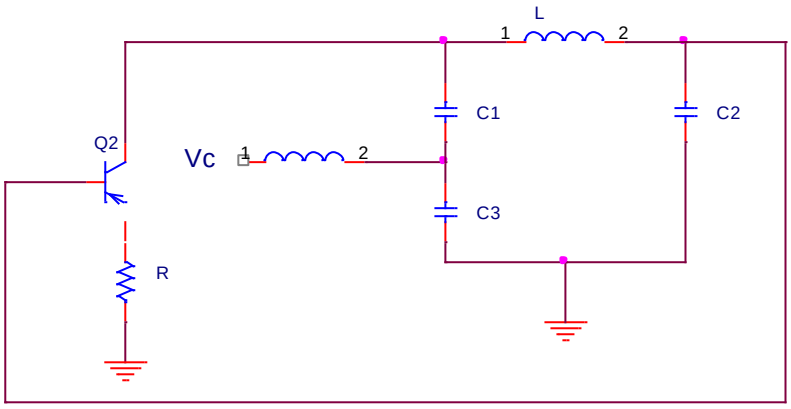


Fig 2.19: Resonant Oscillator (Best, 1997)

VCO is a non-linear device, but in PLL applications analysis, it is treated as linear and time-invariant system. Control signal $V_f(t)$ from the low-pass filter indicates the phase shifting at the inputs. In order to obtain an error signal $V_d(t)$ or filtered control signal $V_f(t)$ to maintain at required lock value, thus phase of $V_o(t)$ can be changed through VCO to follow the phase $V_{in}(t)$ signal. If for example the control signal $V_f(t)$ is 0.5 V ($V_{dd}/2$), thus the VCO will generates only the quiescent frequency, ω_q (centre or nominal frequency). On the other hand, if the control signal $V_f(t)$ is other than 0.5V ($V_{dd}/2$), then the VCO will response by changing its operating frequency, ω_o.

Equation (2-8) summarized the operation of the VCO,

$$\omega_o = \omega_q + K_o V_f(t) \qquad (2\text{-}8)$$

Where K_o represents the sensitivity of the VCO or also known to be gain of VCO (radian/s/V or hertz/V). The constant K_o, represents the change of instantaneous frequency as function amplitude of the control signal following a linear proportion between them. As mentioned in section 2.9, in order for the CDPLL system to be 'locked', $V_f(t) = V_{dd}/2$ and $\theta_e = \pi/2$ at XOR

detector. The principle behind is that quiescent frequency, ω_q (centre or nominal frequency) in VCO is always set to be at $V_f(t) = V_{dd}/2$ (shown in Fig 2.20). Therefore with $V_{dd}/2$, the PLL system must be 'locked' at $\theta_e = \pi/2$ at XOR detector (see Fig 2.21). Indication of signals used within the system is shown in Fig 2.22.

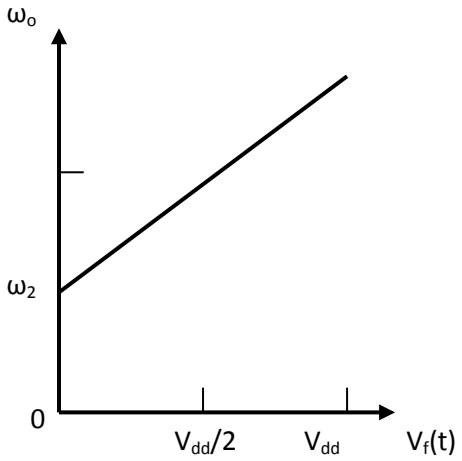


Fig 2.20: If ω_2 required, $V_f(t) = V_{dd}/2$ (Best, 1997)

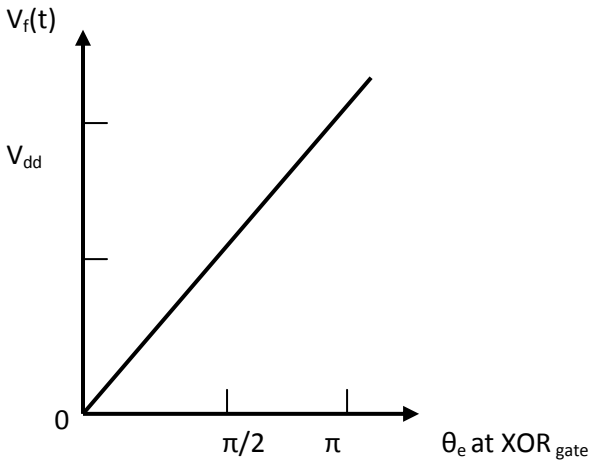


Fig 2.21: With $V_f(t) = V_{dd}/2$ required, $\theta_e = \pi/2$ (Best, 1997)

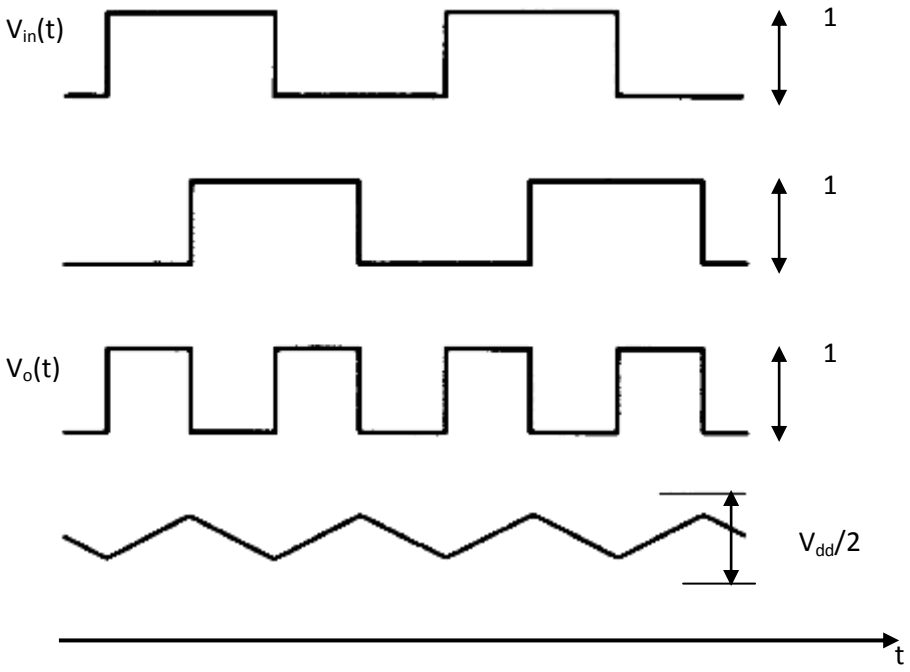


Fig 2.22: Indication of various signals used (Best, 1997)

2.13 Loop Gain

From the above equations and discussions, a PLL can be seen as a servo control system that establishes synchronization generating an estimated replica of the input signal. However this is only true when the input signal is not modulated through any form. If the input signal is modulated (carrying some type of information), the PLL will lock on its carrier. Besides that, the PLL system is a kind of adaptive filter. The algorithms and parameters used in analysis are similar to those applied for filters, for instances Bode plot, 3-dB plot, poles and roots. However, a distinct difference is that the PLL has a very large loop gain.

$$\text{Loop gain} = K_d K_f K_o \qquad (2\text{-}9)$$

K_d – Gain of the phase detector (XOR phase detector)

K_f – Gain of the low-pass filter (K_f =1 for first order passive low-pass filter)

K_o – Gain of the VCO

In order to minimise the phase error or, θ_e, the loop gain is preferred to be high (verified in equation (2-10) with reference back to Fig 2.20 and Fig 2.21).

$$\theta_e = (V_{dd}/2)K_d = (\omega_2 - \omega_1)/K_d K_f K_o \qquad (2\text{-}10)$$

As a result, high loop gain is beneficial for reducing phase error θ_e, thus improving system lock performance.

2.14 Single-Phase PLL Techniques

The single-phase phase-locked loop consists of three main components. A phase detection scheme, Loop filter (LF), and voltage controlled oscillator (VCO) in Fig 2.23. The phase detection scheme, generally implemented using a multiplier, is responsible for finding the difference between the phase angle of the input signal and the output signal.

The output of the phase detection scheme consists of two components. The first component is a function of the phase difference between the input signal and output signal and the second component is at a frequency of twice the signal frequency (this is called the double frequency ripple). Since the second component of the phase detection scheme output is not useful, it can be partially removed using the loop filter. The bandwidth of the loop filter should be small so that it

can remove both the double frequency ripple as well as any unwanted noise. However, if the bandwidth is too small, then this will affect the dynamics of the system. Thus, choosing a proper filter bandwidth is an important PLL design consideration.

The output of the loop filter then contains only the first component which is a function of the phase difference between the input and the output signals, otherwise called the phase error. This error signal is then used to drive the voltage-controlled oscillator to generate an output signal. Ideally, the phase error should be zero, so that the phase angle of the output signal is identical to the phase angle of the input signal. The VCO produces a periodic output signal, the frequency of which changes depending on the applied control signal. When the phase error signal is zero the VCO generates an output signal at the center frequency. However, when the phase error is not equal to zero, the VCO responds by changing its operating frequency. Since the phase angle of the output signal is a function of its frequency (the phase angle is equivalent to the integral of the frequency over a certain period of time), and vice versa, the phase angle of the output signal can be modified to become equal to the phase angle of the input signal by changing the operating frequency of the output signal. Essentially, the VCO is able to drive the phase error to zero by modifying its operating frequency. It generates an output signal with a phase angle equivalent to the phase angle of the input signal.

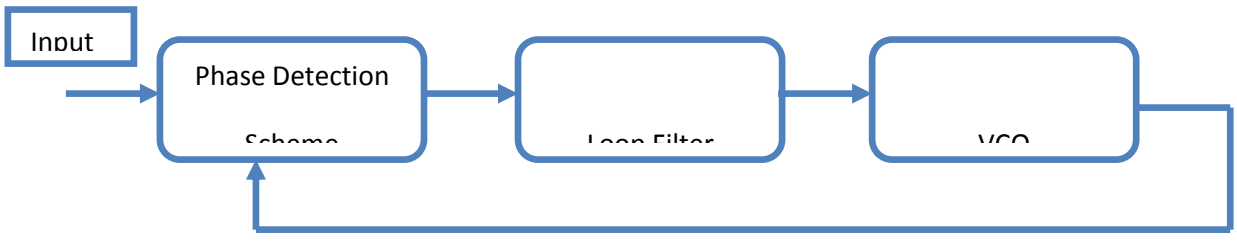


Fig 2.23: General Structure of the Single-Phase Phase-Locked Loop (Lee, 1999)

The main drawback of the single- PLL is that the loop filter is not able to completely eliminate the double frequency ripple without noticeably slowing its performance. Another important drawback of the single- PLL is that three-phase power systems are more common than single-phase power systems, There have been various works proposed to improve the performance of the single-phase PLL. Since the single-phase PLL has no internal harmonic cancellation and generates a double frequency ripple, these works have focused on rectifying this problem.

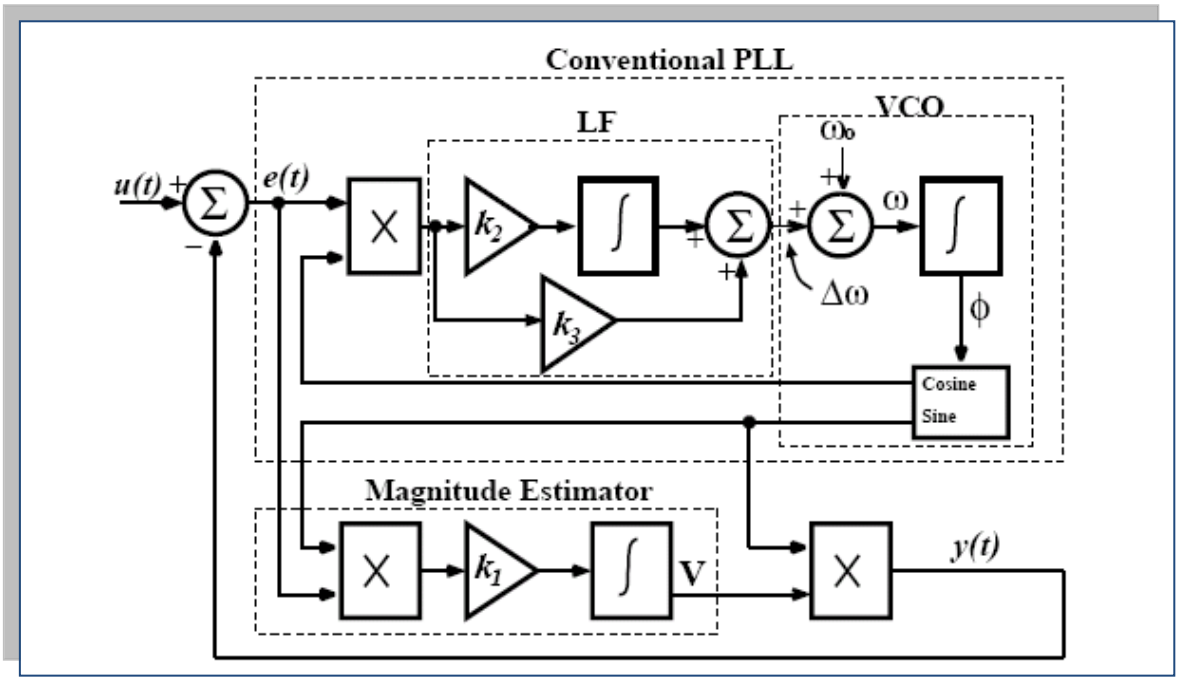


Fig 2.24: Conventional Phase locked loop (Lee, 1999)

Then through the use of a closed-loop control system it regulates the q component, representative of the error signal, to zero by generating a phase angle that is equal to the phase angle of the input signal. In Fig 2.24 the closed-loop control system there is a PI controller (loop filter) which is responsible for providing a filtered output. When adjusting the control parameters of the loop filter it is important to consider that there is a tradeoff between the speed of the response and the accuracy of the filtering. Thus, if the control parameters of the loop filter are set such that it is designed to perform as a very sharp filter, then the speed of the system response

will suffer. Conversely, an increase in the speed of the system response requires a sacrifice in the quality of the filtering. In practice, the filtering is sharp enough such that it is able to eliminate high order harmonics, but not sharp enough to eliminate the low-order harmonics.

signal passes through the loop filter, it is converted from a frequency value to a phase angle value through integration. This integration can be implemented through the use of a voltage-controlled oscillator (VCO). The approximated transfer function of the closed-loop system is given in equation

If the grid is operating at an ideal utility voltage (e.g., balanced, constant frequency, no harmonics) then the phase-locked loop provides a highly fast and accurate synchronizing signal. However, when the input signal to the SRF-PLL becomes unbalanced, double frequency ripples are generated. Unbalance occurs if the input signals have unequal magnitudes or phase-displacements that are unequal to 120 degrees. When unbalance is present in the input signal, the Input signal can be decomposed into three components; the positive-sequence, negative-sequence (see equation 2.11), and the zero-sequence. The zero-sequence term which is present in the input signal is not considered in equation set (Lee, 1999).

$$V = \left\{ \begin{array}{l} V+\cos(\omega t) \\ V+\cos(\omega t - 2\Pi/3) \\ V+\cos(\omega t + 2\Pi/3) \end{array} \right\} \left\{ \begin{array}{l} V-\cos(\omega t) \\ V+\cos(\omega t + \alpha - 2\Pi/3) \\ V+\cos(\omega t + \alpha - 2\Pi/3) \end{array} \right\} \quad (2\text{-}11)$$

Since the SRF-PLL first transforms the input signal into the αβ frame, the input signal becomes separated into the following two components,

$$V\alpha = V^{+}(\cos \omega t) + V^{-}\cos(\omega t+\alpha) \quad (2.12)$$

$$V\beta = V^{+}(\text{Sin } \omega t) + V^{-}\text{Sin}(\omega t+\alpha) \quad (2.13)$$

Finally, the signal is transformed from the αβ into the dq frame, and the q component becomes the error signal. Since the input signal had a negative-sequence component, there is double frequency ripple present in the q component, which can be seen in the following equation,

Simulations in Matlab/Simulink demonstrate that when there is input voltage unbalance (i.e., when there is a negative-sequence component in the input signal), a significant double frequency ripple is presented. in the error signal of the SRF-PLL. Harmonic distortions in the input signal also lead to distortions in the phase and frequency output.

Most of the proposed PLL methods in the literature focus on removing the negative-sequence. One of the most recognized PLL methods of this kind is the decoupled double synchronous reference frame phase-locked loop proposed, which is used to detect and extract the positive-sequence component of an unbalanced voltage vector thereby eliminating the negative-sequence component causing the voltage unbalance. It does this by expressing both the positive- and negative-sequence components on the double synchronous reference frame. The results given by this modified PLL are very good, but there is some room for improvement when the input signal is distorted with harmonics (Yazdani, 2006).

The most state-of-the-art synchronization technique, however, is the phase-locked loop. The conventional single-phase PLL is able to swiftly generate an output signal with a phase angle equivalent to the phase angle of the input signal. However, it also generates a double frequency ripple which cannot be removed without the single-phase PLL losing a significant amount of speed. The conventional PLL tracks the phase angle of the input signal quickly and accurately. Its limitations are that it cannot remove harmonic distortions, nor can it remove the double frequency ripple which it generates when the input signal is unbalanced. Finally, it is unable to operate satisfactorily when there are changes in the input frequency. Various modifications have been proposed in the literature to the PLL to deal with these limitations, and they have had varying degrees of success.

3. ADAPTIVE OBSERVER METHOD

3.1 Over view

In control engineering, in order to achieve a feasible control signal capable of making a considered plant behaved in a desired way, it is essential for the control signal to be based on the mathematical model of the plant, on reference signals capable to be tracked and on measured signals. However, there are situations uncertainties not only occur in the model, but it also occurs in the partial measurement of the state. Furthermore, it sometimes can be very costly or even impossible to allocate a physical sensor into a plant (e.g. in environments where sensors cannot operate accurately or large quantities of sensors are required compared to the observers needed) for the purpose of direct measuring specific quantities, and quite often these unmeasured quantities are somehow crucial to a control system. For all the reasons mentioned above, one of the best solutions will be adapting observer into the design.

An observer is defined as an auxiliary system driven by the available measurements and the plant's inputs; its purpose is to provide estimates of unmeasured states of the plant . Generally, an observer is an algorithm that reconstructs the internal immeasurable states of the system from the measurable output. The theory of observers for linear systems dates back to the early years of the development of modern control theory, see Luenberger. In a linear system, the observer theory is well investigated; both observability and detectability properties are closely connected to the existence of observers with strong convergence properties. However in a nonlinear system, the observer design problem has a systematic solution only if the nonlinearities are functions of the measurable output and the input (Roubal, 2006).

Assuming a general construction of a plant with an observer is shown in Fig 3.1. A plant is said to be observable if any initial state can be determined after a finite time interval. Besides monitoring a behaviour of a plant (shown in Fig 3.1), observers can be implemented in other controllable designs, for instance observer-based control and observer-based adaptive control. Basically, the observer operates by integrating information available, such as input and feedback response, from the known plant in order to produce an estimated signal.

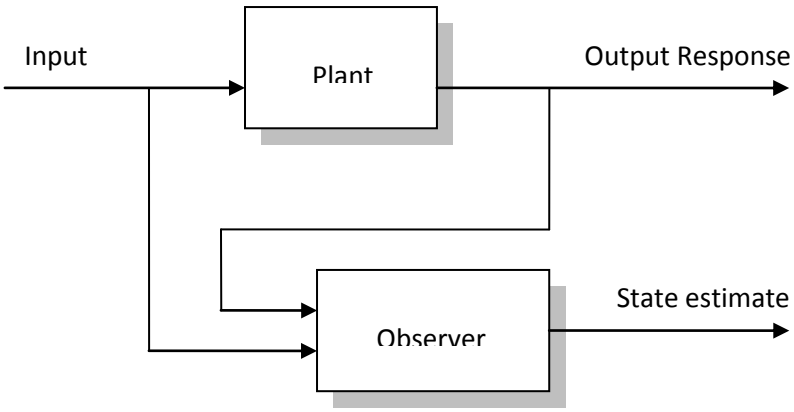


Fig 3.1: Feedback control system with observer attached (Roubal, 2006)

For a clearer view on the observer method, consider a veteran rally driver turning at a very sharp bend in a competition. The driver must apply braking in order for the car to avoid falling off the track, shown in Fig 3.2. However, to be able to complete this in the shortest time, the driver must now consider the braking behaviour of his car together with his braking response, shown in Fig 3.3.

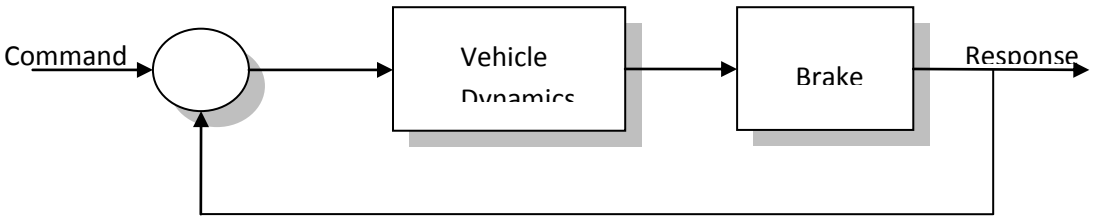


Fig 3.2: Braking system without observer (Roubal, 2006)

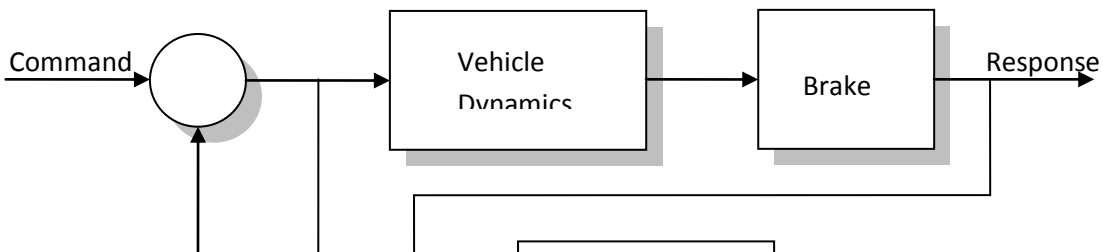


Fig 3.3: Braking response with observer attached (Roubal, 2006)

The objective of having an observer is to combine measured feedback together with the estimated system state, thus the precision can be increased. On the other hand, if the observer within the system is inaccurate or bias, thus the outcomes will not be correctly presented. For example, if the rally driver who is no experience in driving a wagon, thus the rally driver will have difficulties in applying the correct braking response (without observer) to keep the wagon on the track. This is due to the behavior of the wagon's braking response is now difference from a rally car. However, if consideration on the vehicle's braking behavior is taken into account, it is now possible to keep the vehicle not falling off the track.

3.2. Observer for Linear Dynamic System

Consider a linear system represented in a state-space form

$$\dot{x} = Ax + Bu \qquad (3\text{-}1)$$

$$y = Cx$$

where the vectors x, u and y stand respectively foe the state, input and output; A, B and C are constant matrices with entries a_{ij}, b_{ij} and c_{ij} (constant coefficients) respectively.

With the assumptions that the (3-1) satisfy the observability theorem section 3.2.1 above, the observer for (3-1) can be described as

$$\dot{\hat{x}} = A\hat{x} + Bu + L(y - C\hat{x}) \qquad (3\text{-}2)$$

$$\hat{y} = C\hat{x}$$

where $L(y - C\hat{x})$ is the linear output injection with observer gain matrix , L . For the purpose of verifying $\hat{x}$ converges to the real x , hence subtraction of (3-2) into (3-1) gives

$$\dot{e}_x = Ae_x - LCe_x \qquad (3\text{-}3)$$

$$\dot{e}_x = (A - LC)e_x \qquad (3\text{-}4)$$

where $e_x = x - \hat{x}$ is the error signal. The observation error dynamics (3-3) is a stable system if and only $A - LC$ in (3-4) has all eigenvalues with negative real parts, hence $e_x \to 0$ as $t \to \infty$. As a result, $\lim_{t\to\infty} \hat{x}(t) = x(t)$ (Marquez, 2003).

3.3 Observer and Observability of the State Variable Feedback

State variable design is straightforward, but in reality all the states are seldom available as measurements. It is shown here that, given only measurements of some specified outputs of a dynamical system, all the states can be reconstructed using an OBSERVER if the system satisfies a property known as '*observability'*. Observability means that there are enough independent outputs to be able to determine what is going on with the full internal state of the system. It indicates that the chosen measurement scheme is suitable one.

The complete controller is then given as the observer in cascade with the SVFB. In effect, the observer functions as a '*dynamic compensator'*, for the system. (Lewis, 1999)

3.3.1 Full State Feedback Control

A system can be expressed in state variable form as $\dot{x} = Ax + Bu$

with $x(t) \in R^n, u(t) \in R^m$. The initial condition is. Assuming that all states are measurable

one can easily find a state-variable feedback (SVFB) control

$$u = -Kx + v \qquad (3\text{-}5)$$

that gives desirable closed-loop properties. In fact, all the closed-loop poles can be arbitrarily placed as long as the system is *reachable*, which is equivalent to the full rank of the reachability matrix

$$U = [B, AB, A^2B, ...A^{n-1}B] \qquad (3\text{-}6)$$

Reachability means that the control inputs have enough richness to effectively control the internal states.

The closed-loop system using SVFB control becomes

$$\dot{x}\left(A - BK\right)x + Bv = A_c x + Bv \qquad (3\text{-}7)$$

with A_c the closed-loop plant matrix and $v(t)$ the new command input.

Two techniques that can be used to find the SVFB are:

1. Ackermann's formula (when there is only one input, m=1)

$$K = e_n U^{-1} \Delta_D(A) \qquad (3\text{-}8)$$

where $e_n = [0, 0, 0, ...1]$ and the desired closed-loop polynomial is $\Delta_D(s)$

2. The Linear Quadratic Regulator (LQR) equations

$$\begin{aligned} &A^T P + PA + Q - PBR^{-1}B^T P = 0 \\ &K = R^{-1}B^T P \end{aligned} \qquad (3\text{-}9)$$

The first of these is a matrix quadratic equation known as the Riccati equation. Weighting matrices Q, R are user-selected parameters. (Lewis, 1999)

3.3.2 Observer Design with Reduced Measurement Information

In actual practice, all the states cannot be measured so that SVFB cannot be used.

Instead, only a reduced set of measurements given by

$$y = Cx + Du \qquad (3\text{-}10)$$

is available. Where $y(t) \in R^p$. We assume here that the direct feed matrix D is zero, though the following development can be modified if it is not.

We would like to build a dynamical system known as an *observer* that can estimate the internal state x(t) given knowledge of the control inputs u(t) and the outputs y(t). This can be accomplished using the scheme known as Full-Order Observer shown in the below.

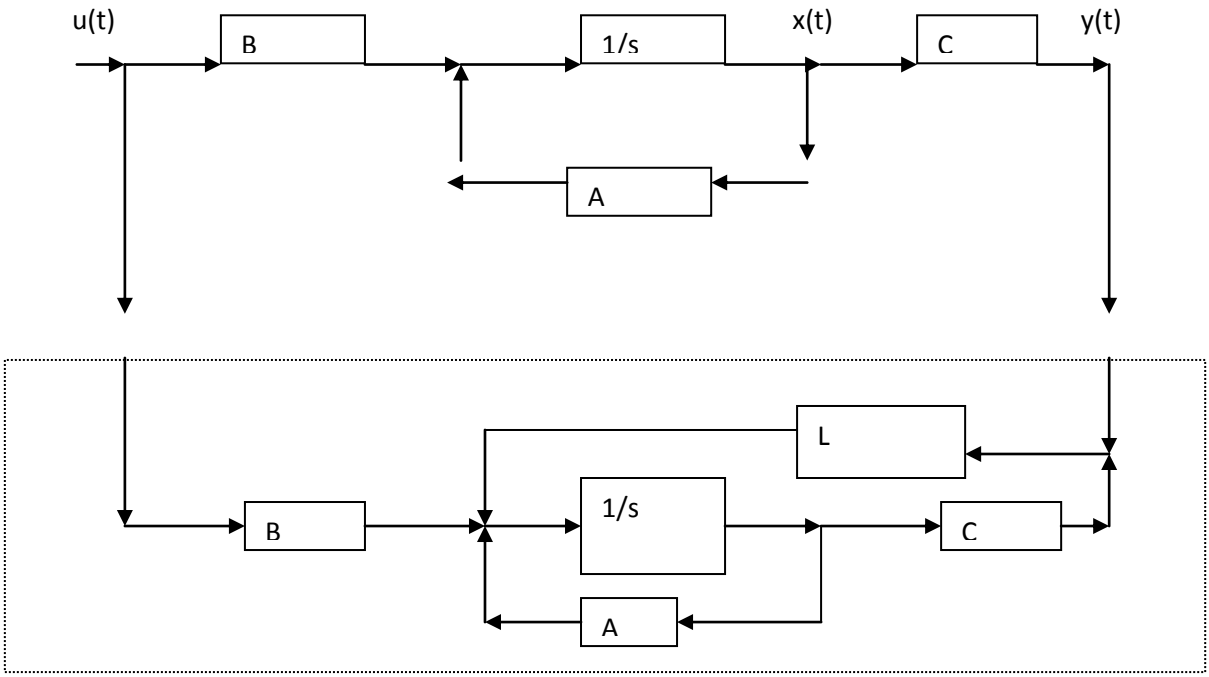


Fig: 3.4 Full-Order Observer (Roubal, 2006)

The aim of the State Observer design is to estimate ***x*** with control input ***u***, measured output ***y*** and system matrices (A,B,C).

3.4 Luenberger Observer:

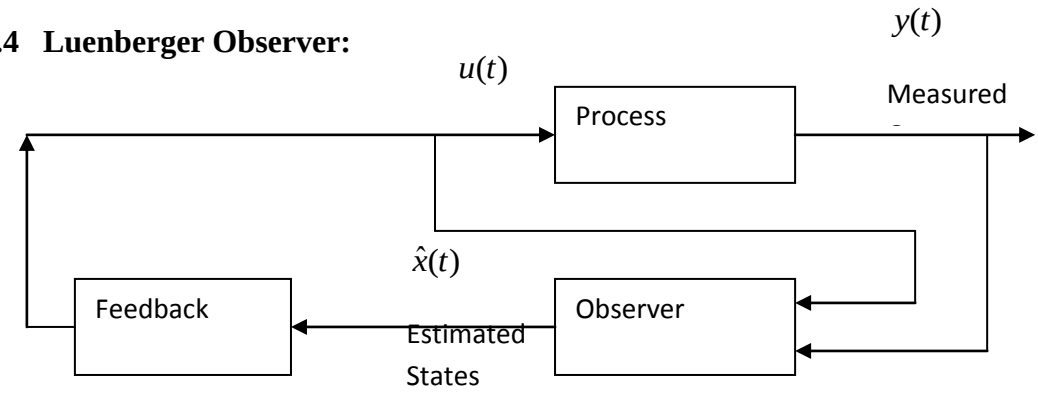


Fig: 3.5 Luenberger Observer (Roubal, 2006)

Luenberger Observer Form:

$$\dot{\hat{x}} = A\hat{x} + Bu + L(y - \hat{y}).$$
$$\hat{y} = C\hat{x} \qquad (3\text{-}11)$$

L is the observer gain matrix to be determined.

Observer Error Dynamics

Denote $e(t) = x(t) - \hat{x}(t)$ as the state error (3-12)

The main purpose of the state error design is to make

$$e(t) = x(t) - \hat{x}(t) \to 0 \quad \text{as} \quad t \to \infty \qquad (3\text{-}15)$$

The error dynamics can be described by

$$\dot{e} = (A - LC)e \qquad (3\text{-}16)$$

The stability of the error dynamics is determined by eigen values of the observer matrix (A-LC).

If (A-LC) is stable then $\hat{x}(t) \to x(t)$ as $t \to \infty$

- **Luenberger Observer and State Feedback Controller Design can described in the following points:**

Observer design:

Choose L so that

$$\det(sI - (A - LC)) = \Delta_{des1}(s) \qquad (3\text{-}17)$$

State Feedback Control design:

Choose K so that

$$\det(sI-(A-BK))=\Delta_{des2}(s) \tag{3-18}$$

The Observer design problem can be re-written as

$$\det(sI-(A-LC))=\det(sI-(A^T-C^TL^T)) \tag{3-19}$$

Luenberger Observer design can be seen as State Feedback Controller design for the dual system $\left(A^T,C^T\right)$

Observability is a property of a system representation that is concerned with determining whether or not the state of that system representation may be determined from known measurements of the output vector *y* over some finite interval of time. According to its theorem, a system is said to be observable if the rank of the observability matrix, defined as

$$\Gamma=\begin{bmatrix} C \\ CA \\ CA^2 \\ \dots \\ \dots \\ CA^{n-1} \end{bmatrix} \tag{3-20}$$

The complete control system with observer is

$$\begin{bmatrix} \dot{x} \\ \dot{e} \end{bmatrix}=\begin{bmatrix} A-BK & BK \\ 0 & LC \end{bmatrix}\begin{bmatrix} x \\ e \end{bmatrix} \tag{3-21}$$

The Separation Principle is used such that the controller design ensures (A-BK) has desired eigen values, the observer design ensures (A-LC) has desired eigen values The stability of the complete system is determined by closed loop state matrix for the complete system. This principle ensures that the state feedback controller design and observer design are decoupled (Roubal, 2006).

3.5 Adaptive Observer Design

A device that estimates or observes state variables of a system is called a state observer. A state observer utilizes measurements of the system inputs and outputs and a model of the system based on differential or difference equations. Three main quantitative state observers are: Luenberger observer, adaptive observer and Kalman filter. However, when the parameters of a system are unknown or time varying only adaptive observer can be applied (Ishitobi, 1988).

A Luenberger observer allows asymptotic reconstruction of the state variable vector of a linear system from measurements of its input and output, provided that the system parameters are known. If, as usually is the case, the plant parameters are unknown, the state observation is subject to error. This fact leads to the use of tile adaptive observer having parameter identification scheme for practical application (Ishitobi, 1988).

In this area of control technique, the most prominent adaptive control method is a model reference adaptive control approach where the controller gains are determined in order that the unknown system asymptotically behaves as a given reference model. However, this approach essentially requires that the plant is a minimum phase system. On the other hand, adaptive control using adaptive observer is a natural extension of tile usual state feedback control system synthesis and no assumption such as stable invertibility is made of plant characteristics. Although the control system design concept seems to be simple in case of state feedback control using an adaptive observer, the principal difficulty is the complexity of the proof of the stability of the closed-loop system because it closely depends on the structure of the parameter identification scheme included in the adaptive observer. (Ishitobi, 1988)

A PLL can be viewed as state feedback control system, for which an observer specifically an Adaptive Observer can be designed and implemented for the better understanding of the states.

4. SIMULATION & ANALYSIS

The simulation results for the following PLLs are obtained with the operating frequency of 1.1MHz frequency.

The performance of each PLL is evaluated at a medium frequency of 1.1MHz.

The transient response for each PLL are shown below.

1. CPPLL:

The SIMULINK model for the CPPLL is shown below:

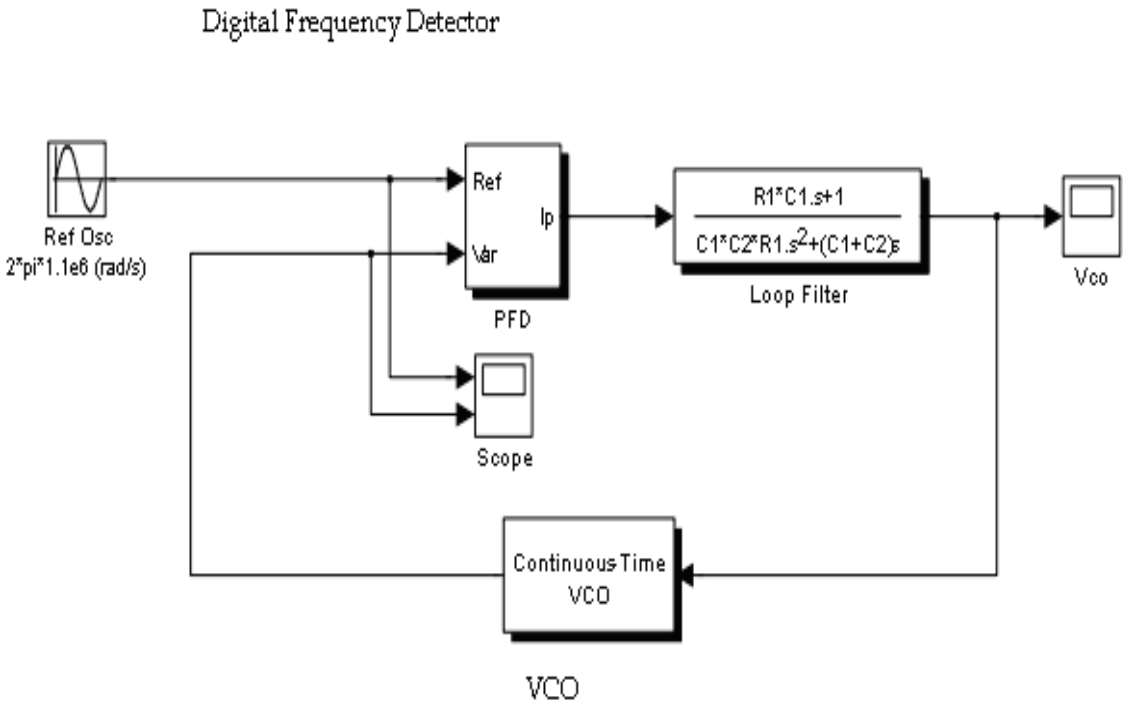


Fig:1.1 CPPLL

Implement the charge pump with a Gain block. Set the gain parameter to 260e-6 (Ampere). A behavioral model for the loop filter can be created with a simple Transfer Function block. To set the parameters of this block, we need to find the transfer function for the loop filter. Applying the Laplace transform to the differential equations yields:

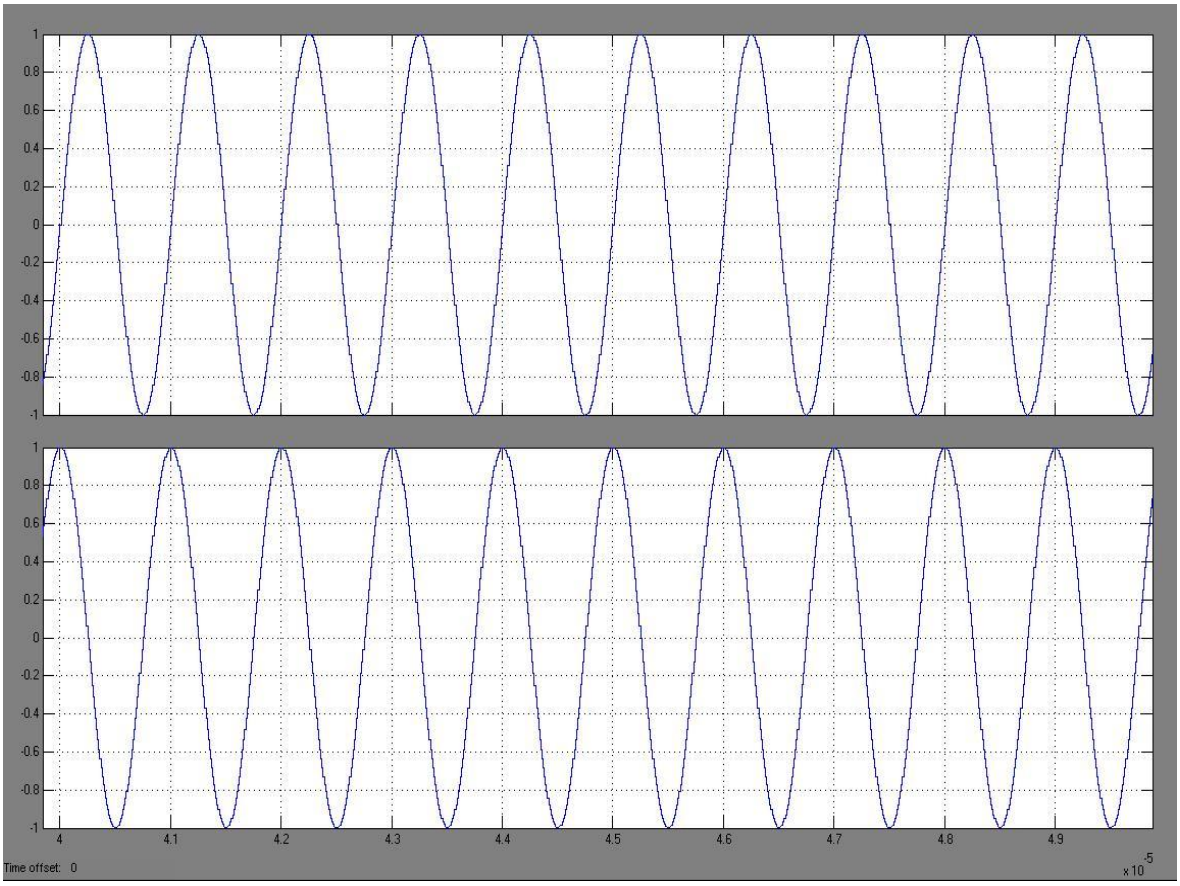
Set the Numerator coefficient of the Transfer Fcn block to [R1*C1, 1], and set the Denominator coefficient to [C1*C2*R1, (C1+C2), 0]. Next, adjust the loop gain by changing the Input Sensitivity of the VCO to 3e5. Change the Initial phase to –pi/2.

Assign values to variables C1, C2 and R1 in the MATLAB workspace:

C2 = 15e-12;

C1 = 80e-12;

R1 = 21e3;



Output Results

The transient response for an operating frequency of 1.1MHz is shown below.

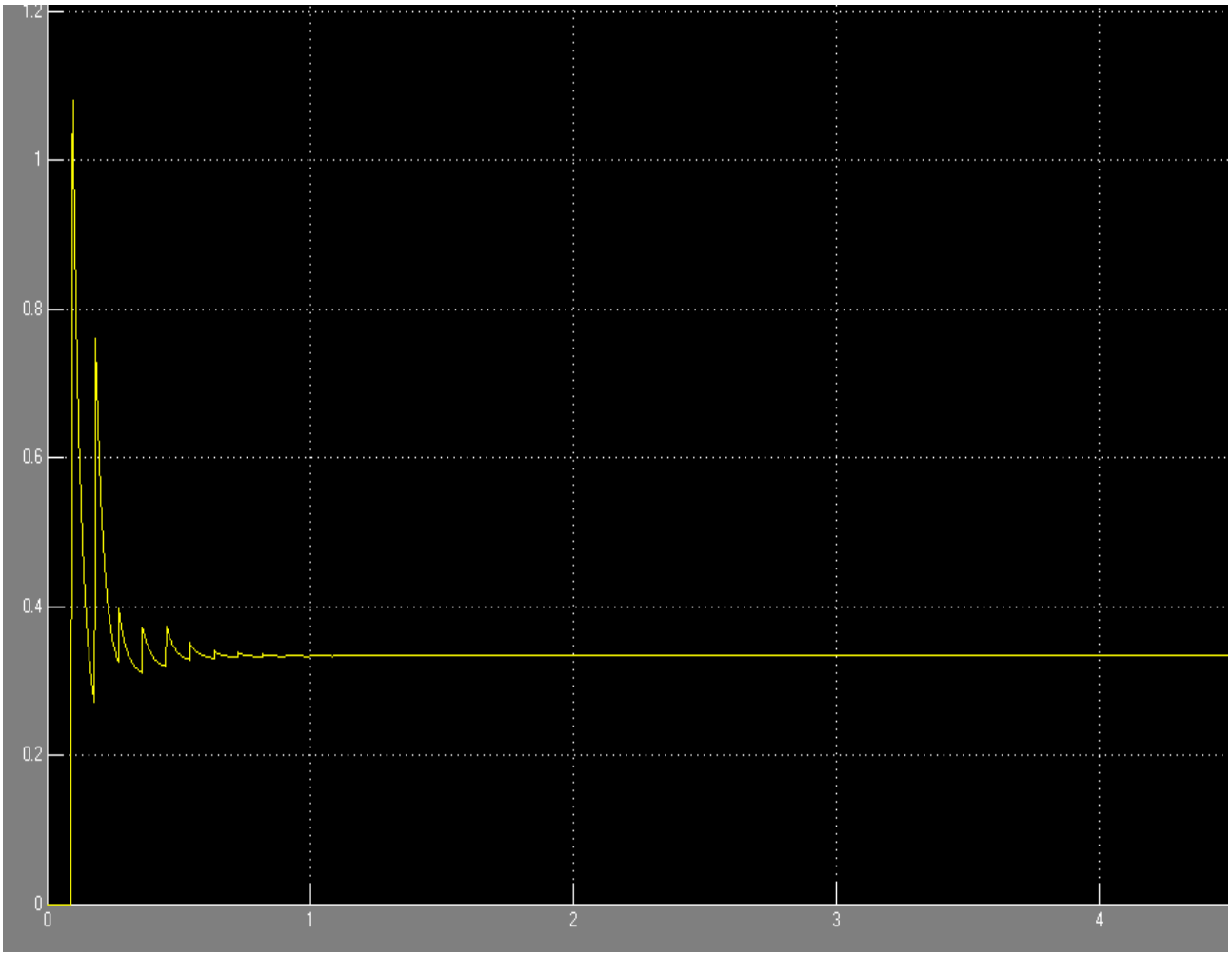
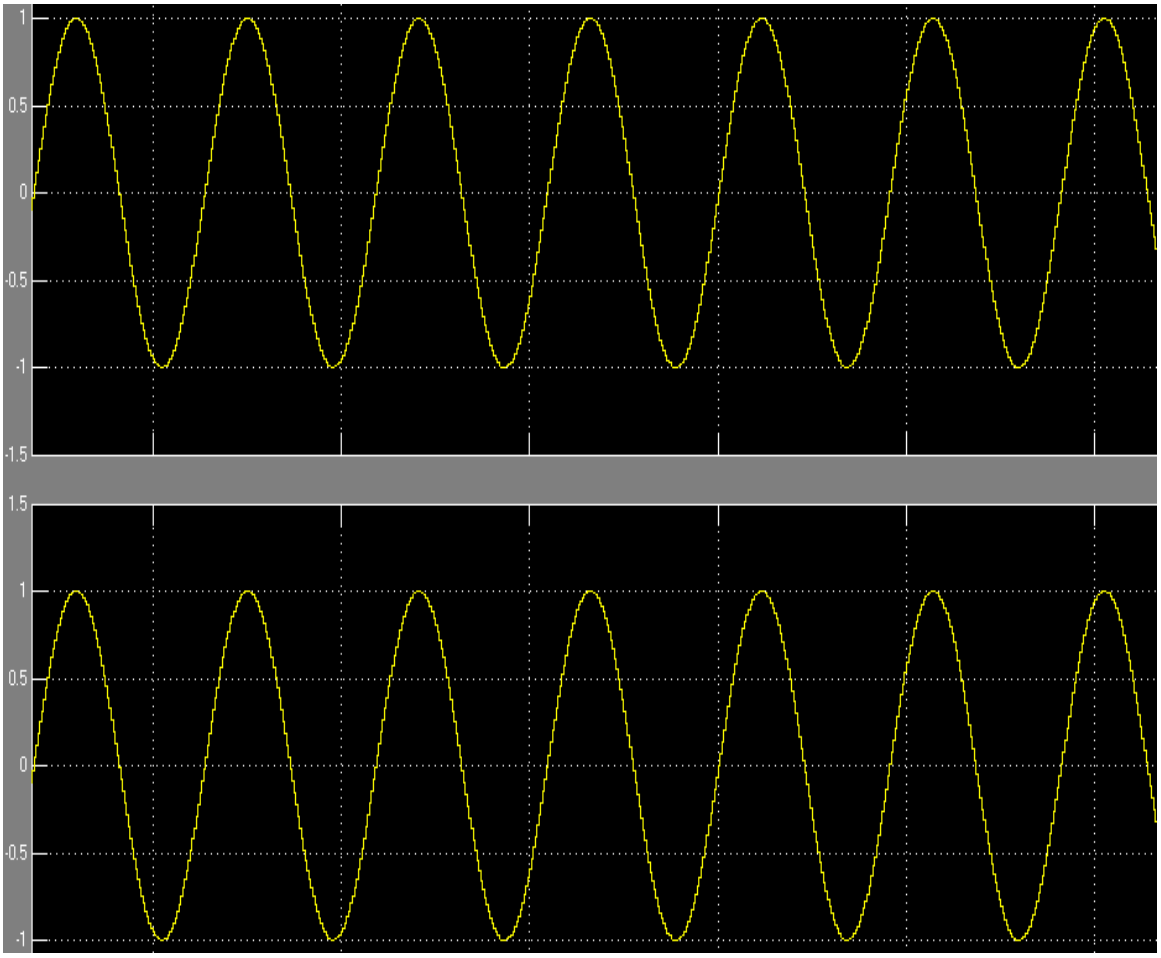


Fig:1.1 Output Waveform

The input frequency and the frequency of the output signal of VCO of CPPLL are shown below:



2. DPLL

The SIMULINK model for the DPLL is shown below:

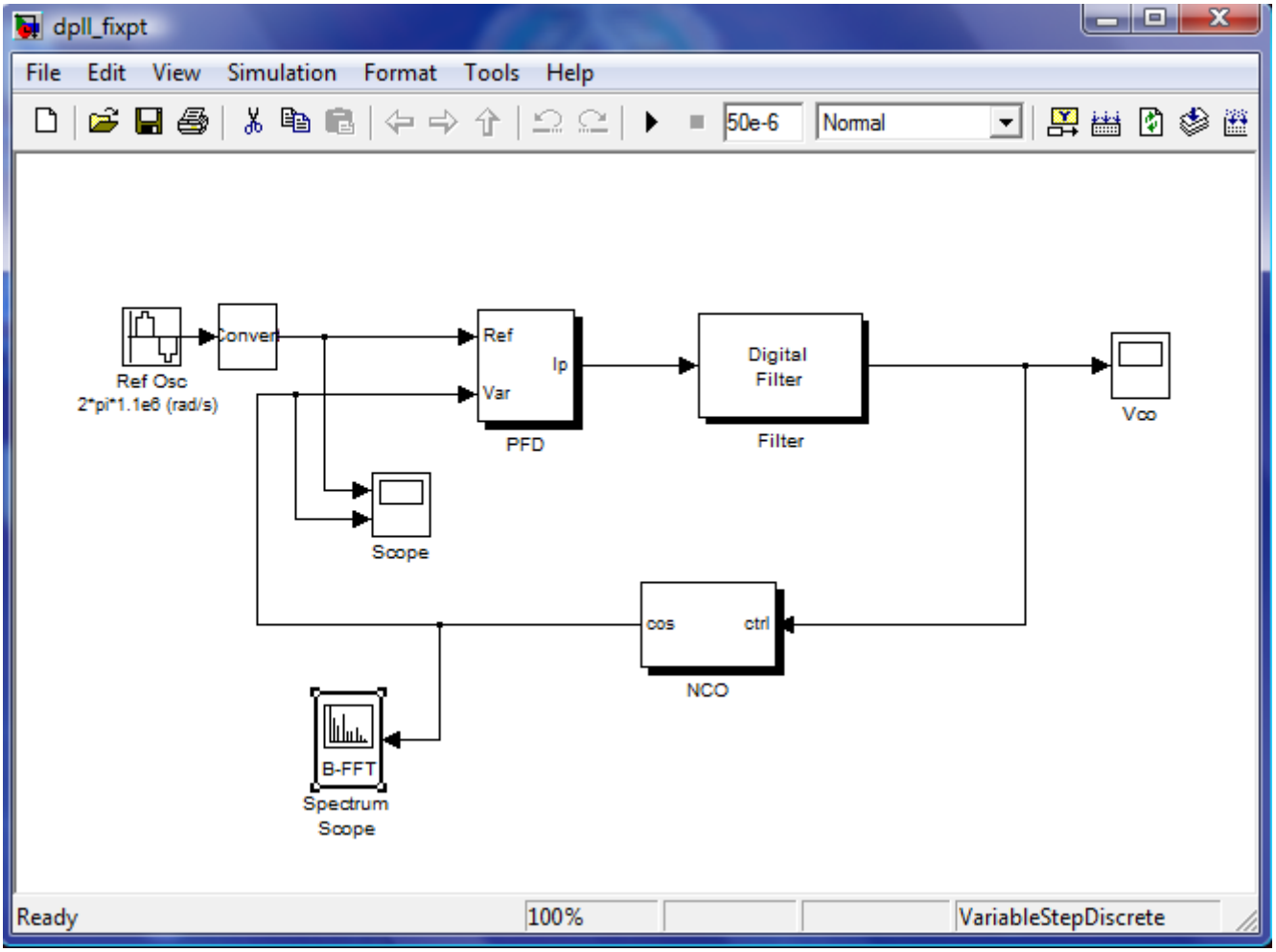


Fig: 2.1 Digital Phase-locked loop

We obtain the best results can be achieved with a charge pump and a filter. The charge pump, "pumps" current into a 2nd order filter. The branch voltage of the filter is used as input to the VCO. A digital phase frequency detector (PFD) determines whether a positive or negative current is pumped into the filter. Phase lead corresponds to a negative frequency (output and thus VCO frequency decreases) whereas phase lag corresponds to a positive current.

The PFD is characteristically a finite state machine that responds to zero-crossings of the input signals. If the orientation signal has a positive edge first a switch is turned on those pumps a positive current into the loop filter, until a positive edge of the VCO signal is detected (phase lag).

Output Results

The transient response for an operating frequency of 1.1MHz is shown below.

Fig: 2.1 Output Waveform

The output spectrum of the VCO is shown below:

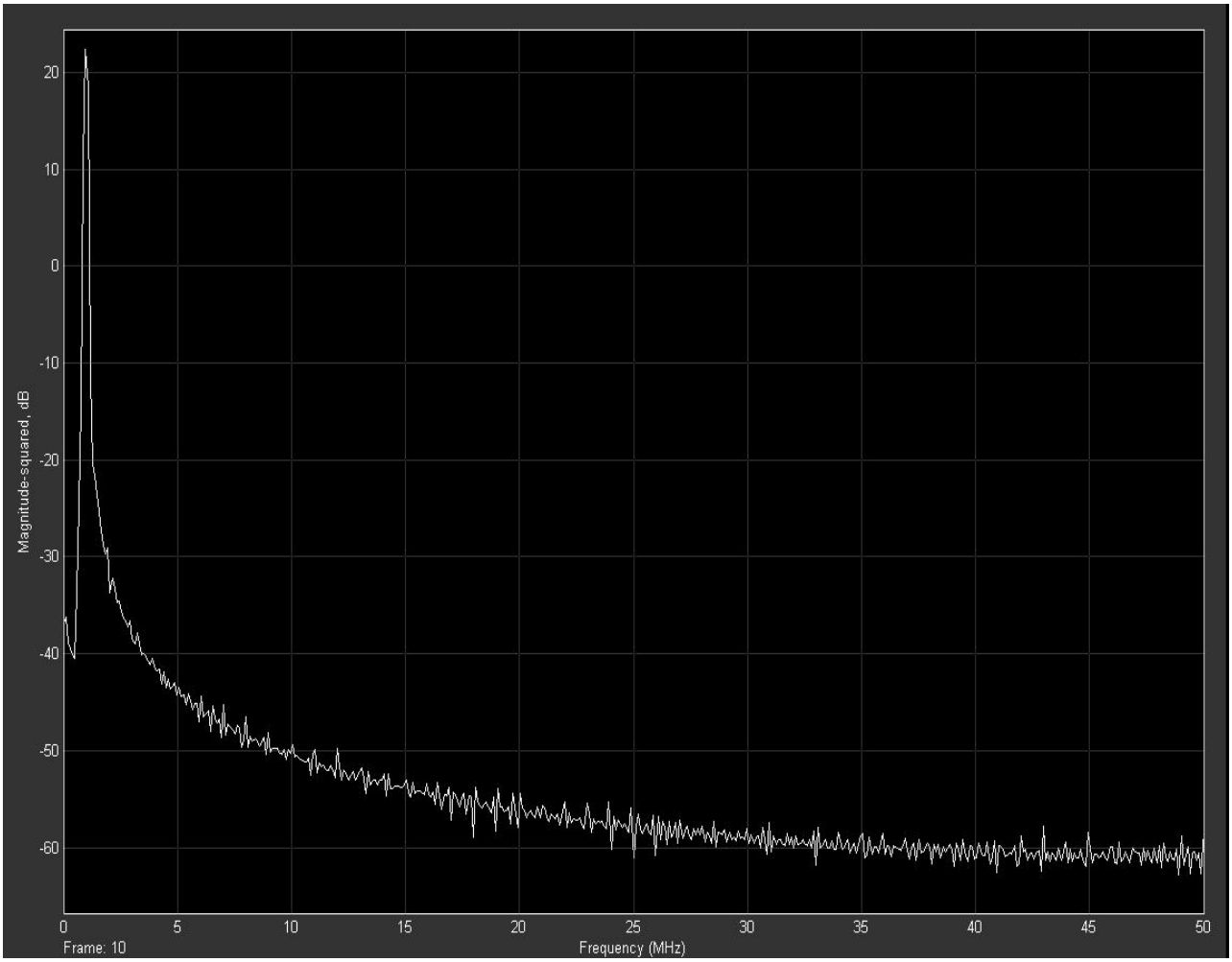


Fig: 2.2 Output Waveform

3. Linear PLL

The SIMULINK model for the CPLL is shown below:

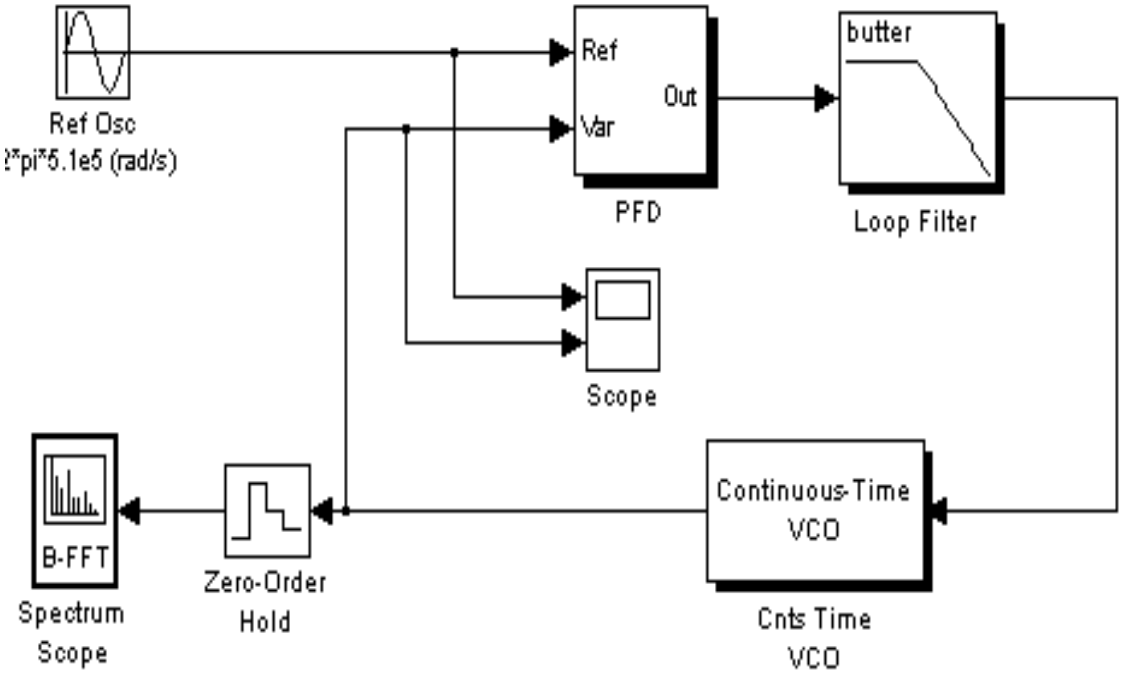


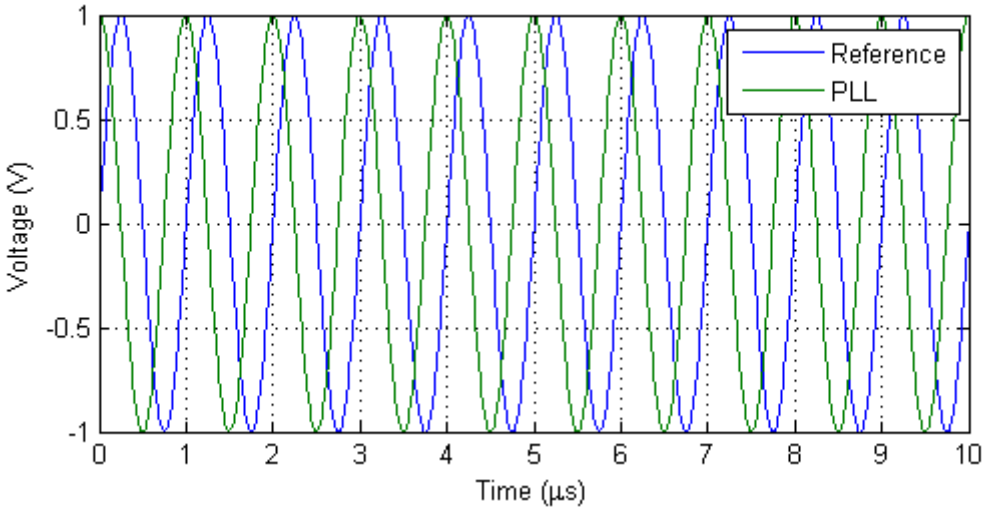
Fig: 3.1 Linear Phase-locked Loop

In order to simulate the system, we could do with a test input and visualization. To accomplish this, add a Sine wave block (Sources Library - Simulink) and a Scope block (Sinks library - Simulink) to the model. Set the constraints of the Sine wave to:

We set the values for Sine Wave block; Frequency: 2*pi*1e6,

All other constraints: default.

Add other axes to the Scope block, and bond the two inputs to the outputs of the Sine Wave block and the VCO block. Alter the simulation time to 50 periods (50e-6). Tie the second Scope block to the output of the filter.



To charge the value of the PLL we are going away to look at the spectrum of the generated signal. Add a Spectrum Scope block from the Signal Processing Sinks library and vary it's parameters:

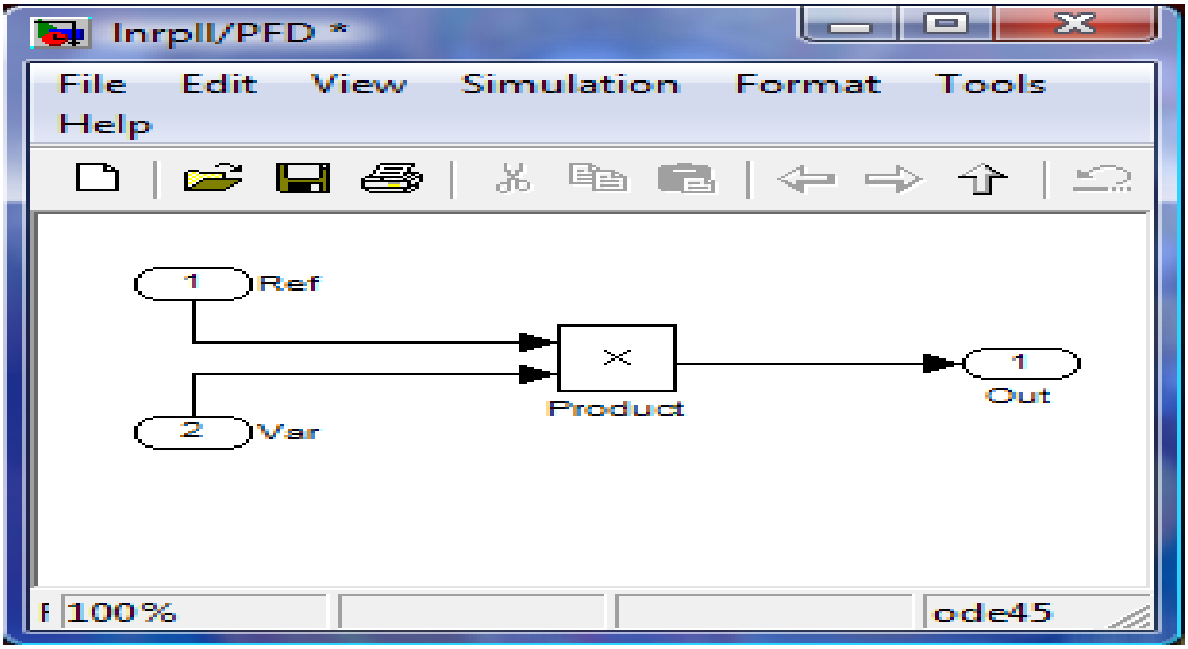


Fig: 3.2 Linear PLL/Phase-Frequency Detector (PFD)

While Robustness of the PLL perform to phase and frequency dissimilarity we can change the Frequency and Phase offset parameters of the Sine. For instance, the PLL locks at frequencies up. Also, for frequencies other then 1 MHz, the generated signal will have a phase offset with respect to the carrier (the reason being that the filter doesn't have a pole at zero. Also note the ripple on the control signal, which is due to the second harmonics of the multiplication.

Output Results

The transient response for an operating frequency of 1.1MHz is shown below.

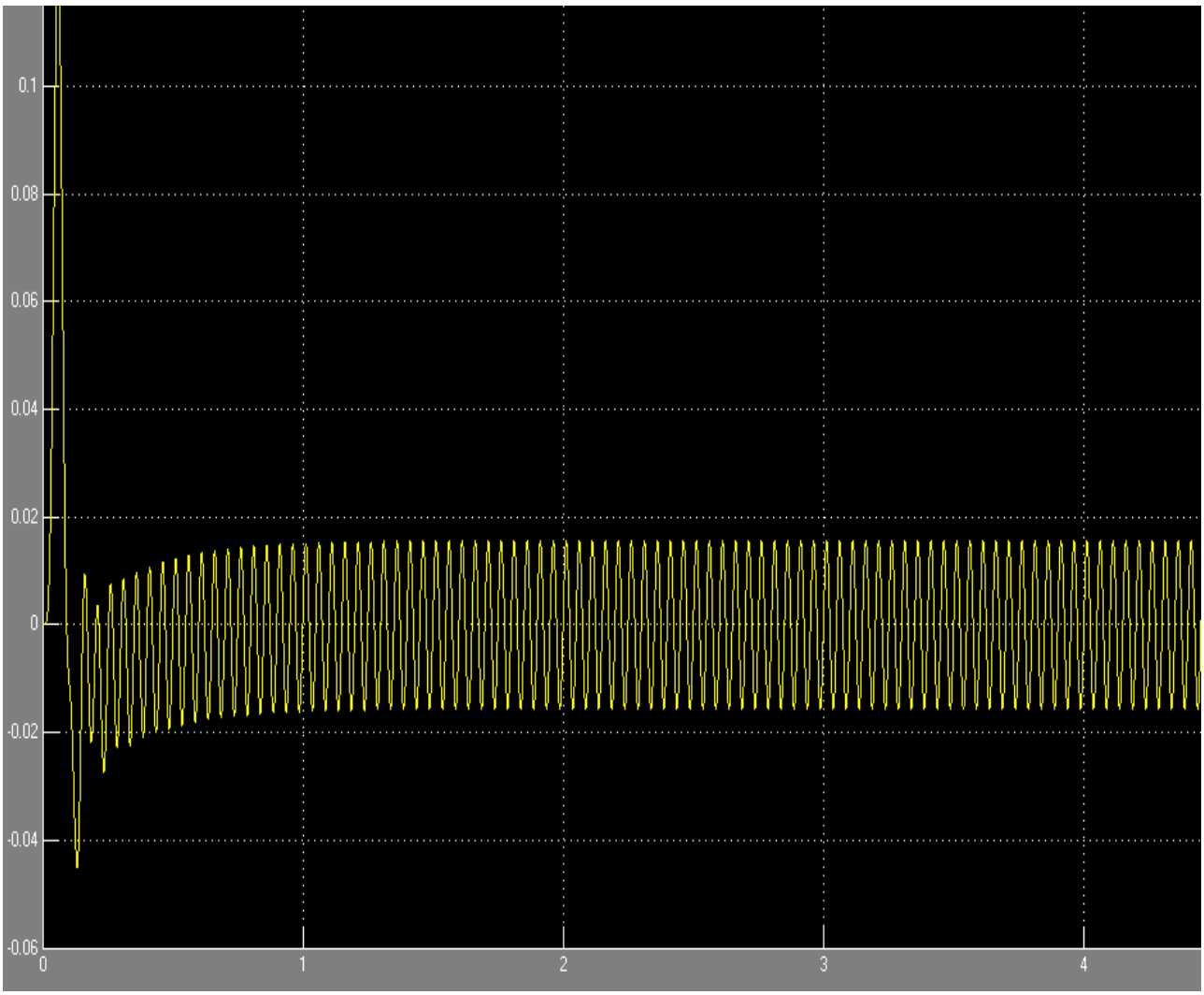
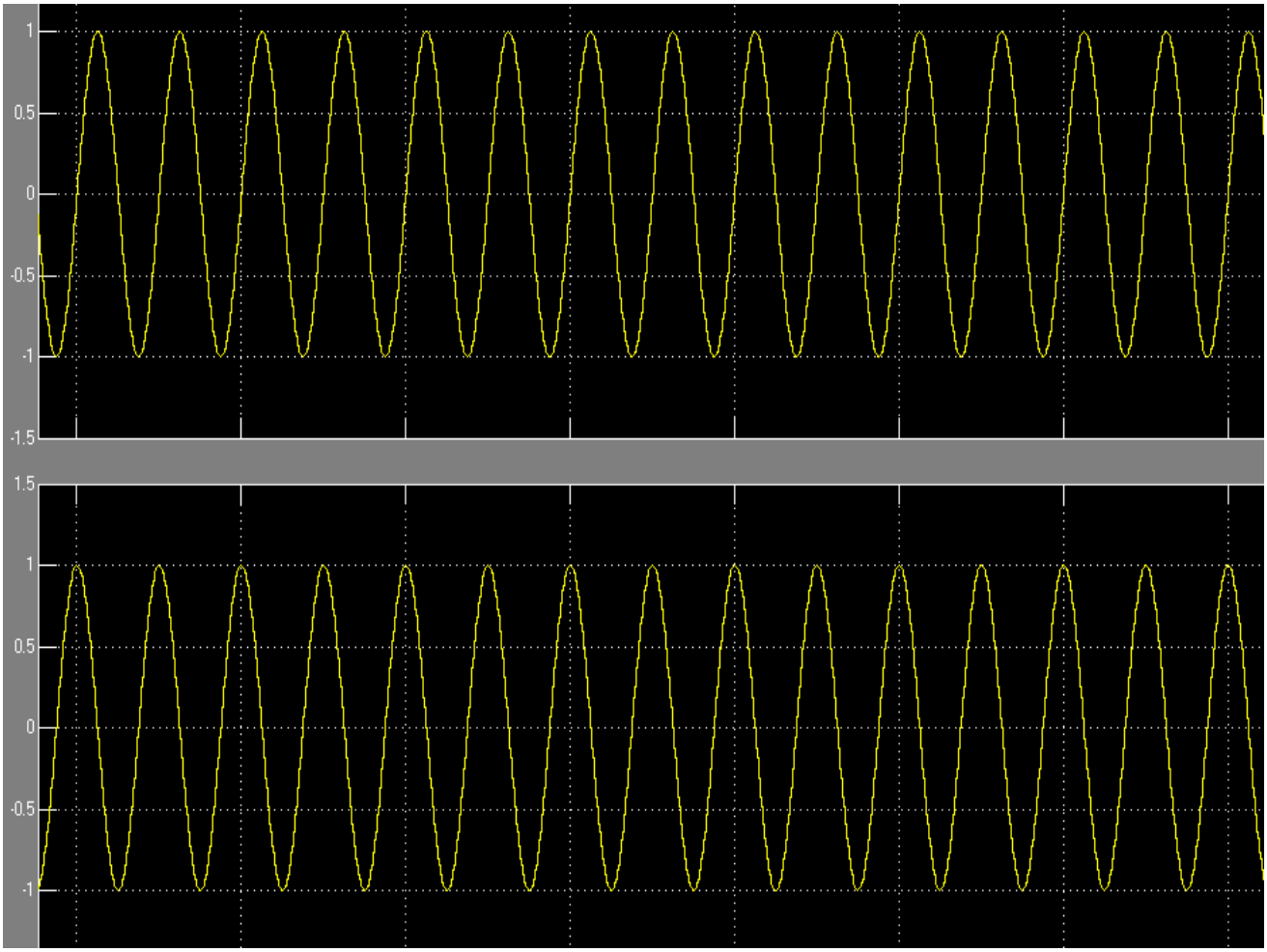


Fig: 3.1 Output Waveform

The input frequency and the frequency of the output signal of VCO of CPLL are shown below:



4. PWR(Power) PLL

The SIMULINK model for the PWR-PLL is shown below:

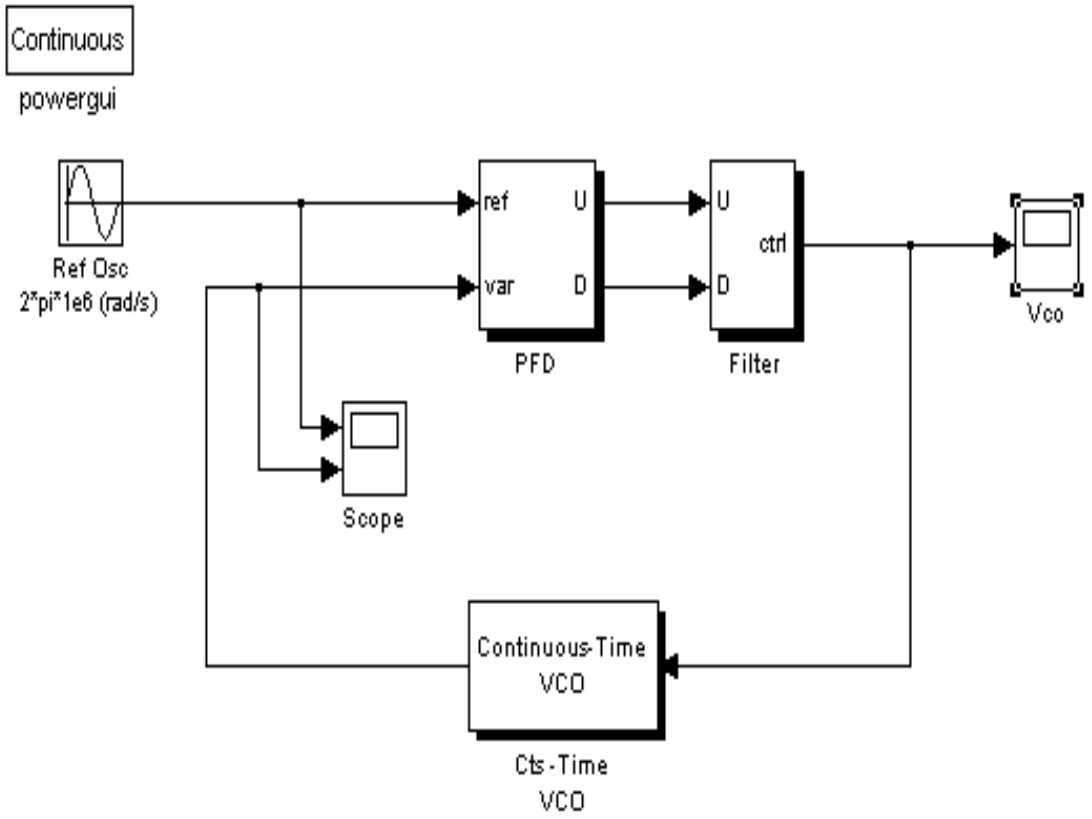


Fig: 4.1 PWR Phase-Locked Loop

In this PWR PLL model we have reference oscillator, power factor detector, filtering circuit, continuous time VCO.

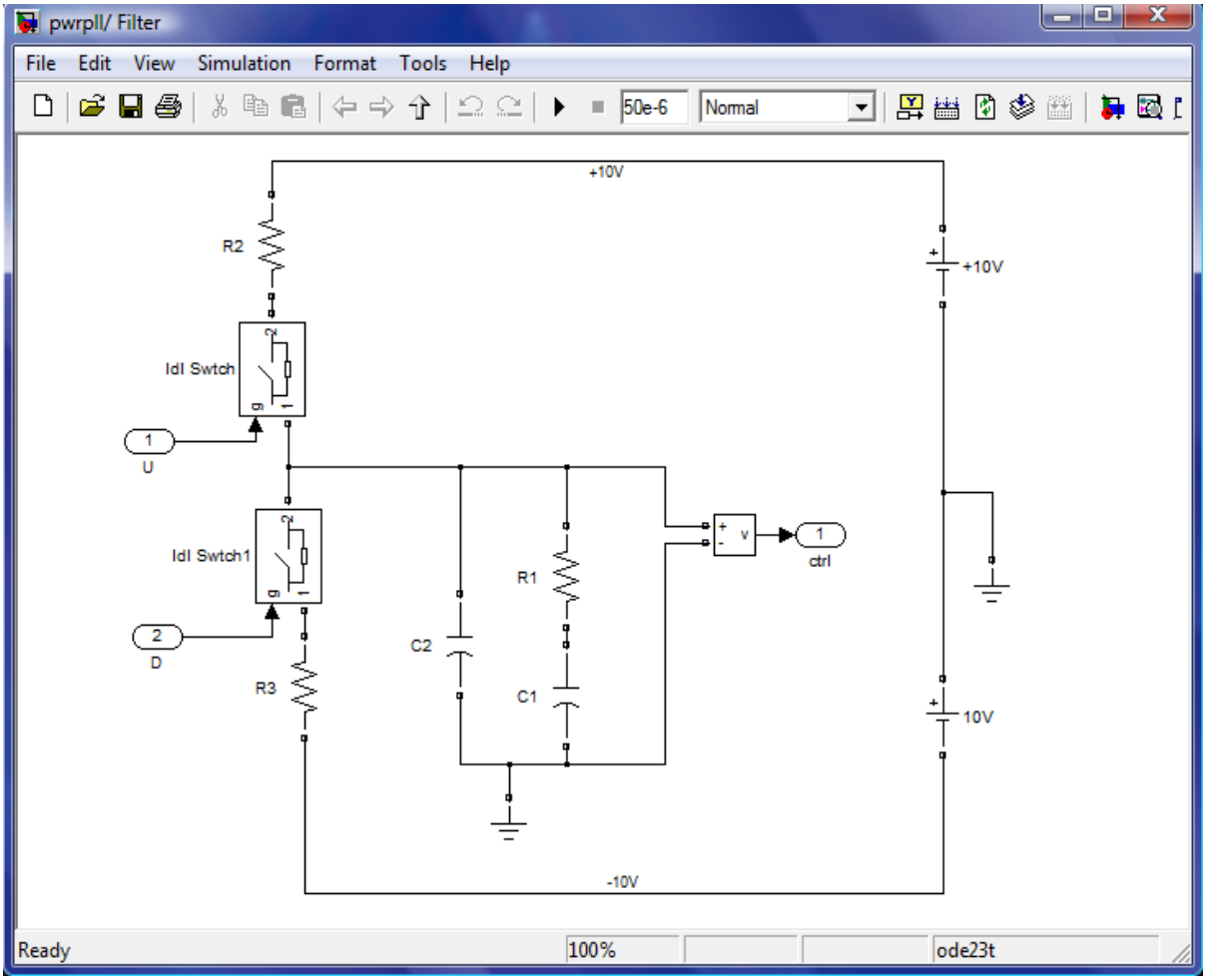


Fig: 4.2 PWR PLL/Filter

In the bove PwrPll/Filter, two identical switch is used, idl swith and idl swithc1 are pass to the capactor and combination of resistor and capacitor and voltage differences to output leads. Supply is given to the idl switch through Resistor R2.

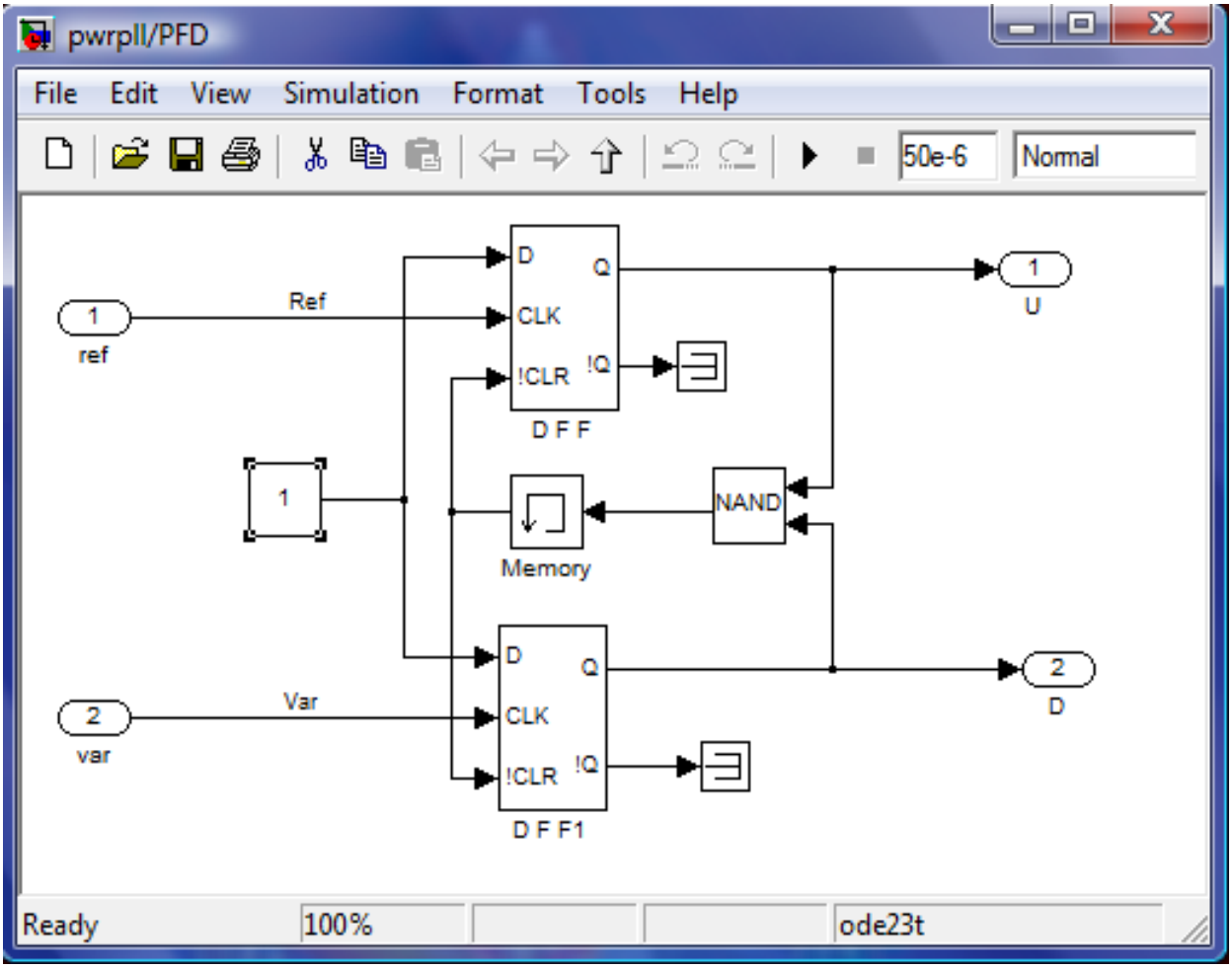


Fig: 4.3 Pwr PLL/Phase-Frequency Detector (PFD)

In the above Pwrpll/PFD, the phase frequency detector is implemented by two flip-flops and a NAND gate. With the help of sim power system toolbox is used to design the Filter and other basic building blocks .

This lean-to to Simulink constructs it possible to sketch electrical circuits in a straight line in Simulink. This gets rid of the necessity to develop differential equations and transfer functions and facilitates experimenting with different network topologies.

Output Results

The transient response for an operating frequency of 1.1MHz is shown below.

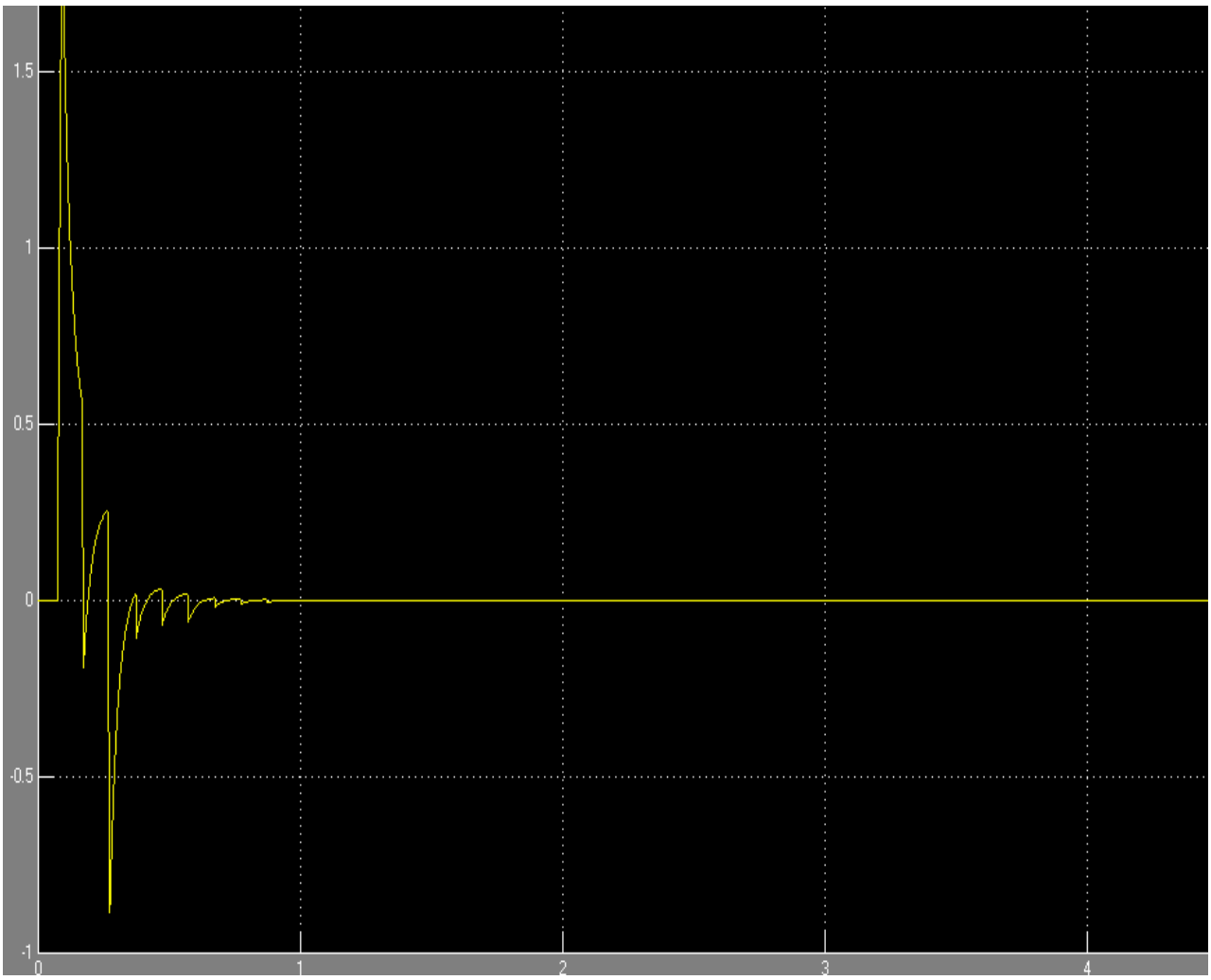
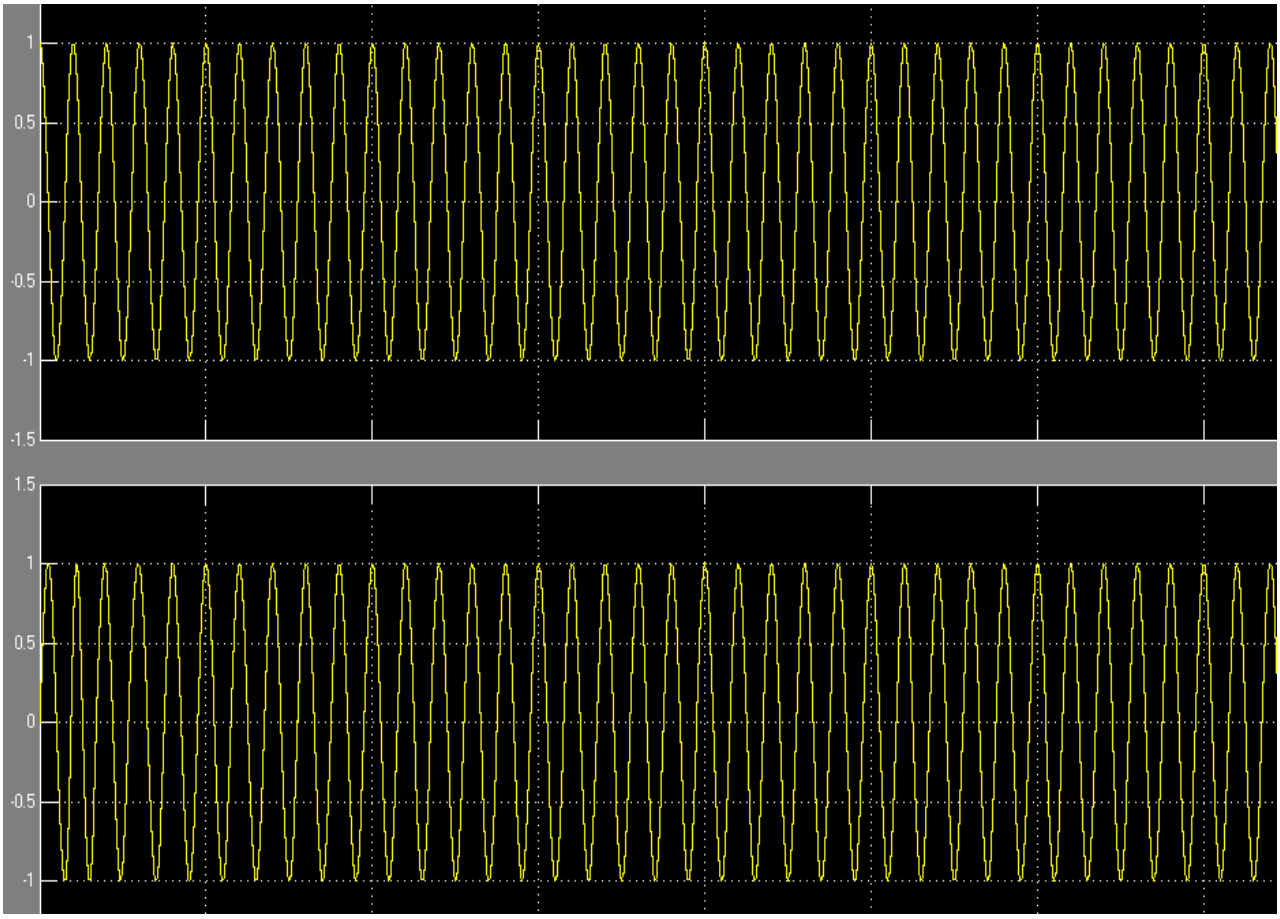


Fig: 4.1 Output Waveform

The input frequency and the frequency of the output signal of VCO of CPPLL are shown below:



5. Conclusion

The examination of the settling time show showed that higher values of phase margin than about 50° should be evaded, as that leads to a sharp enlarge of the settling time. The scrutiny of the residual frequency variation showed that the modus operandi which leads to optimal residual phase deviation performance, must be avoided in tuning systems which will be used in frequency-modulation systems, since it always results in a sub-optimal remaining frequency deviation performance. It was confirmed that design for spectral purity piece often leads to unsatisfactory settling performance, because of different requirements on the loop bandwidth and on the position of the poles and of the zero of the closed-loop transfer function. The adaptive architecture described it's resolved these paradoxical requirements, without the necessity of switching circuit elements in the loop filter. The adaptation of loop bandwidth occurs continuously as a function of the phase error in the loop, without interaction from outside of the tuning system. During frequency jumps, high bandwidth and high phase margin are obtained by bypassing filter sections. When the loop is locked, the architecture allows heavy filtering of spurious signals. The implementation of the dead-zone block was presented and the basic trade-offs of the concept were discussed. The adaptive PLL was optimized for use in a multi-band (global) car-radio tuner IC which featured inaudible background scanning. Design and architecture of the PLL building blocks were discussed, and measurement results were presented.

Although there are still much to be improved and developed, I believe I have done my best. I am pleased with the outcomes of the project and achievements I made. In addition, I have gained confidence in operating MATLAB/ SIMULINK and other software.

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