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Structural and Electrical Characteristics of $CdS - Cu_2S$ Thin Film Solar Cells

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To my wife Amal and my daughters Najla and Bayan

ABSTRACT

A study has been made of a variety of factors influencing the efficiency and operational stability of front-wall CdS-Cu_2S solar cells. In the course of this work ~ 1 cm^2 cells were fabricated with conversion efficiency of up to 8% without attempting to reduce reflection losses.

The CdS films were produced by vacuum evaporation and the electrical and structural characteristics of these films were studied as a function of the rate and temperature of the deposition. Previously there had been some controversy concerning the nature of the CdS source material required for fabricating high performance CdS-based solar cells, but this work has shown that a variety of CdS sources can be employed successfully provided that the film deposition parameters are suitably chosen.

A conventional chemical exchange technique was employed to convert the CdS film surface to Cu_2S, with the thickness and stoichiometry of the resultant Cu_2S layer being examined by means of electrochemical analysis.

Changes in the electrical properties of the CdS-Cu_2S cells due to post-fabrication anealing under a variety of different conditions were studied and correlated with structural changes monitored by means of Auger electron spectroscopy with the aid of argon ion etching. Depth profiles of the constituent element concentrations indicate that, for samples annealed in air, a deep penetration of copper into the CdS layer occurs together with a significant out-diffusion of cadmium from the CdS after only a few minutes at 100°C. In contrast, the copper penetration which results from vacuum or hydrogen annealing treatment is substantially less and no significant out-diffusion of cadmium is observed for annealing temperatures up to 400°C. Two different diffusion processes, one in the grain boundaries and one in the mid-grain regions, have been identified and their relative importance has been studied for annealing cycles performed under the same three different ambient atmospheres (air, vacuum or hydrogen). The normally rapid and undesirable grain boundary diffusion of copper was found to be significantly inhibited by the use of flowing hydrogen during annealing. A further technologically important observation concerns the effect of the deposition of a film of copper over the copper sulphide layer of a cell and subsequent annealing of it in air. The improved electrical stability which this treatment yields has been shown to be directly associated with reduced interdiffusion at the CdS-Cu_2S interface. This interfacial diffusion has also been shown to be influenced by the CdS stoichiometry in the vicinity of the junction.

Finally, a brief investigation was made into the use of the ion implantation technique as a means of doping the upper layer of the CdS film with copper without annealing the completed cell. The results have demonstrated the feasibility of this technique, with the best results being obtained using a copper ion fluence of 5.10^{14} ions cm^{-2} at 50 keV ion energy.

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Chapter 1

Introduction

1.1. Energy Sources

The world energy scene is characterised by a steadily increasing demand for energy for the production of goods and services, a rapidly depleting store of fossil fuels and increasing pollution hazards associated with excessive burning of these fossil fuels. In view of this unsatisfactory situation, a search is going on all over the world for an energy source which is renewable, inexhaustible and clean. Solar energy is perhaps the most popular choice in this regard. It is almost inexhaustible, clean and distributed all over the globe. It is for this reason that intense efforts are being made in many parts of the world to make more extensive use of solar energy to meet out growing energy needs.

Essentially, there are three main approaches towards the utilization of solar energy. These are: (i) the thermal approach, in which solar radiation is absorbed by passive collectors and converted into thermal energy which can be used for a variety of purposes such as water heating, drying, industrial process heating etc. (ii) direct energy conversion, in which solar energy is directly converted into electricity using either photovoltaic or thermoelectric modules, and (iii) biological conversion, in which solar energy is used to promote, through photosynthesis, the production of biomass which can be used for the production of transportable fuels or electricity.

Intense research and development work is going on in each of these approaches, and it is expected that each will make a significant contribution to the future world energy requirements. In particular, the direct conversion approach has been shown to be technically feasible and,

in addition to its convenience as a system which can stand alone or be linked to a national grid supply, it is considered likely to be economically attractive in the long run.

Photovoltaic solar cells (particularly silicon p-n junctions) have been known and in use for quite some time. Indeed, they have served as the most reliable power source for both the manned and unmanned space flights. In the development of space quality solar cells, no consideration was given to the cost of the solar cells. The main emphasis then was on reliability of these cells to produce the required electric power but, today, greater consideration is being given to producing drastic cost reductions as well as achieving the reliability and long term stability required for terrestrial applications. Already a number of large scale installations have been planned and a 1 MW station began operation in Southern California early in 1983 making use of the expensive Si wafer cell modules (1), but it is probable that the main worldwide market will be for cheaply produced systems in the small and medium power range. It is expected that much cheaper production costs can be achieved by replacing the single crystal wafers of Si with Si ribbon, polycrystalline or amorphous Si films. Alternatively, a wide variety of materials (2) other than Si have been investigated. In particular, much attention has been paid to CdS - Cu_2S cells in thin film form. Because of the relatively little amount of material required for large area devices, the ease of production, and the low energy pay-back period, this system is full of promise.

1.2. Materials for Solar Cells

The key to the development of any efficient, low cost photovoltaic

device lies in the choice of suitable materials or tailoring of these materials to the required specifications together with the adoption of processing techniques which have a suitably low energy consumption. However, the performance of a solar cell must be analysed in terms of criteria which relate not only to the cell itself but also to the application in which it is designed to be used. The definition of these criteria will identify research directions in relation to promising materials and lead to the development of appropriate energy conversion devices.

From the basic nature of the photovoltaic phenomena (discussed in chapter 3), it follows that a photovoltaic device should essentially be comprised of two components, one which absorbs the incident sunlight and generates the minority carriers (known as the absorber-generator) and the other, that collects these charge carriers and converts them into majority carrier (this is known as the collector-convertor).

In selecting suitable absorber materials, three important material parameters need be considered, these are (i) band gap, (ii) absorption coefficient and (iii) minority carrier diffusion length. Theoretically, it has been demonstrated that any semiconductor with a band gap between 0.8 and 2.4 eV could achieve 10% conversion efficiency [3,4]. However, these calculations of the efficiency as a function of energy band-gap, shown in Fig. (1.1), assume absorption and collection efficiency as 100%, i.e. all the photons greater than the band gap energy are absorbed, each produces one electron-hole pair in the material and, finally, all of the charges which are generated are collected by the electrodes without any recombination. However, due to reflection losses and the other losses discussed below, the theoretical efficiencies cannot be fully attained in practice.

The second parameter of considerable importance in determining the efficiency is the absorption coefficient. Figure (1.2) shows the absorption coefficient $\alpha(\lambda)$ of several semiconductor materials as a function of the incident photon energy [5]. It follows that except for Si, other materials with an energy band gap between 1.0-1.7 eV absorb 90% of the photons in a 5 μm thick layer. Si will absorb about 70% of the useful photons in 10 μm thickness and 90% of the photons in 100 μm layers. Other materials such as GaAs, CdTe, Cu_2S, Cu In Se_2, etc. absorb the same number of photons in a much smaller thickness (less than 1 μm). For instance, Cu_2S absorbs 90% of the sunlight with energy greater than its band gap energy within a thickness of only 0.4 μm.

The third parameter of relevance is the diffusion length of the minority carriers (L) in the absorber material because, after achieving photon absorption and carrier generation, the generated carriers must be transported to the junction region with minimum loss. The diffusion length depends on doping and impurity concentration in a material and also on the structure of a material, i.e. on whether it is crystalline or noncrystalline (oriented polycrytalline, polycrystalline, or amorphous). Clearly, the thickness of the absorber layer in a photovoltaic cell is limited by the minority carrier diffusion length.

The collector-convertor is designed to collect the minority carriers generated in the absorber and to convert them into majority carriers. There are three material characteristics for consideration, (i) Electrical conductivity, (ii) Electron affinity and (iii) Lattice constant. The collector material must be of the opposite conductivity type to the absorber so that the generated carriers are not lost by recombination and are converted to majority carriers in this material. Secondly, the collector material must have an electron affinity matched to the absorber

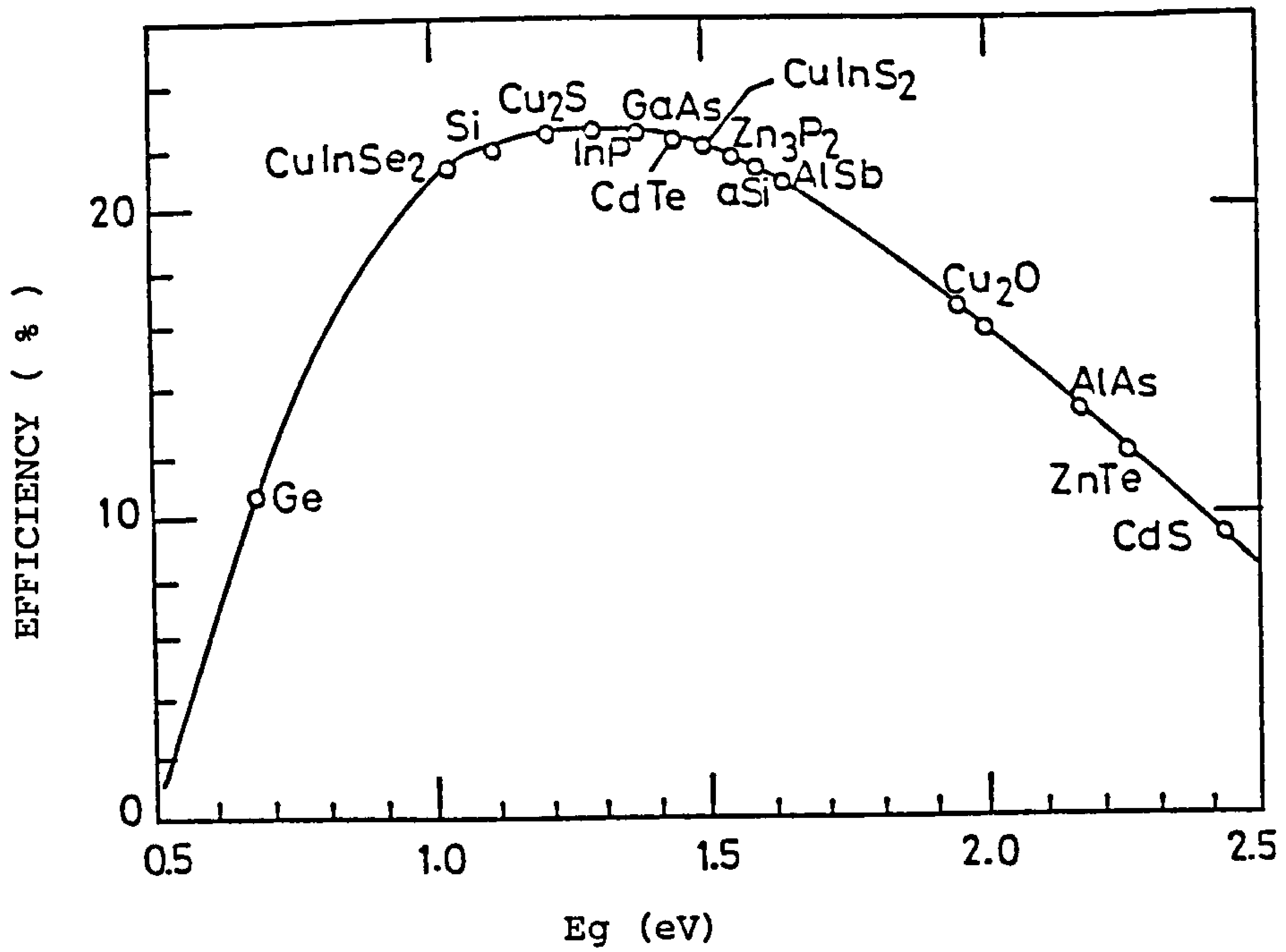

Figure (1-1) Maximum conversion efficiency versus energy band-gap for several semiconductor materials possessing photovoltaic absorber qualities. (From M. Prince ref.3.)

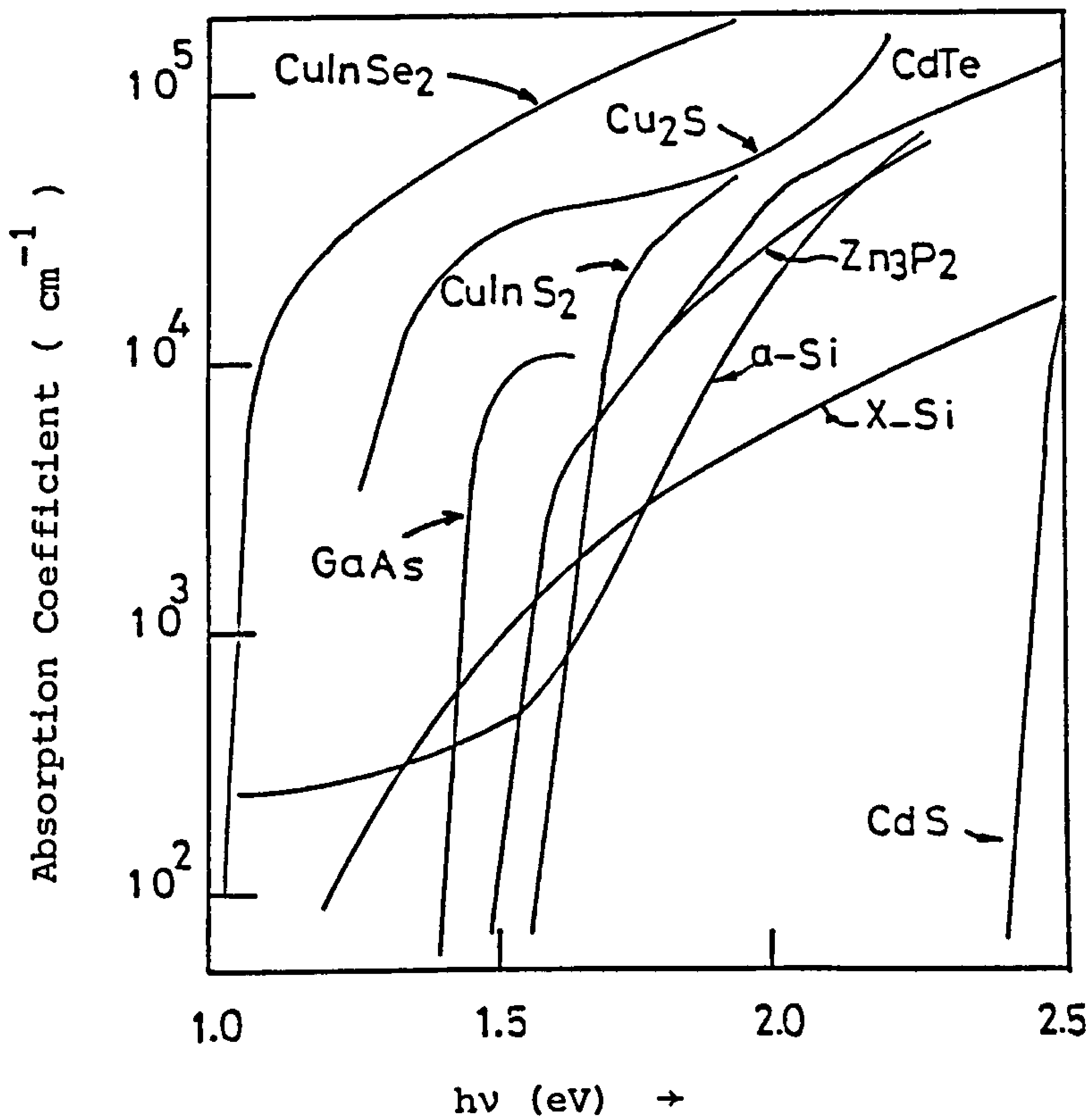

Figure (1 - 2) Absorption coefficient for several absorber materials as a function of photon energy. (From A.M. Barnett and A. Rothwarf ref. 5)

because any mismatch in electron affinity leads to a decrease in the photovoltaic efficiency. The third parameter is the lattice constant which must match the absorber material. Any lattice mismatch produces interface states [6] at the junction which can then act as a recombination surface leading to a reduction in the photogenerated current collection efficiency.

1.3 Thin Film Solar Cells

Thin film polycrystalline solar cells are leading contenders in the search for low-cost, mass produced large area devices. However, one of the main problems with polycrystalline thin films is the existence of internal surfaces in the form of grain boundaries. The grain boundaries are regions of increased disorder with both structural defects and segregated impurities in large densities. Thus they are generally regions of increased recombination. In addition, charge trapping at grain boundary energy levels can form potential barriers that impede carrier transport. Therefore, these grain boundaries can degrade current generation, photovoltage, and the stability of the cells.

A number of different materials (e.g. Cu_2S, CdTe, CdS, $CuInSe_2$, Zn_3P_3, GaAs and amorphous silicon) have been used in devices which have exhibited respectable efficiencies under laboratory conditions and, although their full potential has yet to be realised, an improved understanding of the associated problems is gradually being developed. This is clearly demonstrated in the case of CdS - Cu_2S cells which are the subject of this thesis. The intense research effort centred on these devices has led to a steady improvement in reported efficiencies to nearly 10%. Table (1-1) shows the performance achieved with a number of thin-

Table (1-1). Representative efficiency of some thin-film solar cells.

cell	Best efficiency reported (%)	ref.
a-SiC/a-Si	10.1	7
GaAs p^+/n homojunction	8.1	8
$CdS/Cu\,In\,Se_2$	9.53	9
$Zn_x\,CdS_{1-x}/Cu\,In\,Se_2$	10.98	14
CdS/Cu_2S	9.15	6
	7.93	This work
$Zn_x\,CdS_{1-x}/Cu_2S$	10.2	10
CdS/CdTe	10.5	11
$CdS/CuInS_2$	3.25	12
CdS/InP	5.7	13
$Mg/Zn_3\,P_2$	4.3	15

film solar cells. It is clear that at the present time, the CdS - Cu_2S solar cell remains one of the leading members of the group of thin film photovoltaic devices and in the light of the results and experience, so far obtained, these devices are now seen to offer a serious alternative to more expensive single crystal Si solar cells. However, a number of problems have yet to be solved before sufficient confidence is developed for large scale commercial exploitation.

1.4 The Aims of This Work

As indicated above, the devices which have been studied during this research project have been the subject of numerous previous investigations. While this previous work has led to a steady improvement in reported efficiencies, there has been some controversy concerning the best fabrication procedures for achieving high efficiency and there is still much uncertainty about the factors which are inhibiting further improvement and which cause cell efficiencies to degrade during operation.

In order to develop an understanding of such matters it is necessary first to obtain detailed information about the fundamental processes which occur during cell formation, during any post-fabrication treatment and during subsequent operation. While the main aim of this work has been to provide such information, considerable time and effort were spent initially in developing reliable cell fabrication procedures. As discussed in Chapter 2 (which provides some of the background to the current study) the cell properties are critically dependent on every component part of the device so that a very high degree of control is required at every stage of cell construction in order to achieve suitably reproducible results.

Having gained the required proficiency in cell fabrication, a wide

ranging investigation was undertaken to analyse the structure, the composition profiles, the optical properties and the electrical properties of the devices and to study the changes in these characteristics associated with changes in fabrication and post- fabrication treatments. As might be expected, a wide variety of analytical and measuring techniques were employed during the course of this investigation. The basic theory, of semiconductor junctions in terms of which some of the experimental results have been interpreted is given in Chapter 3 while a description of the apparatus and other experimental details can be found in Chapter 4. A full account of the results obtained from each part of the investigation is given in Chapter 5. In Chapter 6 these results are discussed and assessed in relation to the initial aims of the study. Finally, the work is summarised and the main conclusions presented in Chapter 7.

Chapter 2

2. Developments in Photovoltaic Solar Cell Technology

2.1 General Historical Review

It was Becquerel [16] in 1839 who first observed that a voltage was developed when he directed light on to one of the electrodes in an electrolyte, the so-called "photovoltaic effect". 38 years later, Adams and Day [17] observed the effect in selenium. In 1891 Appleyard [18] suggested the use of photovoltaic cells as energy conversion devices. A number of other early solid-state research workers including Lang [19], Grondahl [20] and Schottky [21] pioneered selenium and cuprous oxide photovoltaic cells. A bench mark in the development of photovoltaic devices occurred in the early 1940s with the discovery by Ohi [22] of photovoltaic action at a p-n junction situated within a silicon crystal. A few years later, p-n junction photovoltaic devices [23-26] were fabricated using PbS and Ge. But it was not until 1954 that solar cells with acceptably high conversion efficiency for electrical power generation came on the scene. In that year, Chapin et al. [27] reported that they had made a diffused silicon solar cell with a conversion efficiency of 6%. Subsequently Reynolds and coworkers [28] made a similar breakthrough with a single crystal cadmium sulphide device, and Rappaport [29,30] achieved practical efficiencies using a Si p-n junction to convert the energy in particle radiation into electrical energy (the betavoltaic effect). With the achievment of these relatively good results in 1954, the development of photovoltaic devices for solar energy conversion began.

The first analytical treatment of solar cell efficiency was published in 1955 by Prince [3], and then Loferski [4] showed that there is an optimum energy-band gap of about 1.5 eV for the semiconductor materials of

p-n homojunction solar cells. This stimulated investigation into some materials such as gallium arsenide, cadmium telluride and indium phosphide which have energy band gaps close to optimum [33]. In the 1960's and early in 1970's many laboratories were involved in the study of solar cells produced using many different materials and techniques [34,35]. Most of the cadmium chalcogenides were investigated, including CdTe-Cu_2Te [36], CdTe-CdS [37] and the graded band-gap Cd_xSTe_{1-x} anisotype heterojunction. [38]

A comprehensive treatment of basic solar cell characteristics was produced by Hovel [39] in 1975. Backus [40] compiled a volume of classic papers on solar cells up to 1974 and Stanley [41] reviewed the development of thin film CdS cells up to 1975. More recent reviews have been contributed by Hill [42] on thin film solar cells, and by Shirland and Rai-Choudhury [43] who have discussed photovoltaic device configurations and the system arrangements that could be built using various low cost materials. In 1979 Savelli and his colleagues [44] considered again the problems and promises of the CdS-Cu_2S solar cells, and in the same book Fahrenbruch and Aranovich [45] gave a general account of heterojunction phenomena and interface defects in photovoltaic converters. Since the beginning of the 1980's the ever increasing interest in photovoltaic devices has lead to a succession of review articles on all aspects of the subject. Kazmerski [46] produced a good book about polycrystalline and amorphous solar cells but much attention has continued to be focussed on CdS-Cu_2S thin film solar cells. For example, Rothwarf [47] has reviewed the basic anomalous effects observed in CdS-Cu_2S solar cells and Burton [48] has discussed the utility of using $Zn_xCd_{1-x}S$ in place of CdS in conjunction with a Cu_2S layer. In 1981 in a book on photovoltaic and photo electrochemical systems, Bloss and Schock [49] reviewed the CdS-Cu_2S

thin film solar cells, while Townsend [50] discussed the Schottky barrier solar cells. In the same year Hall [51] reviewed the progress made with silicon photovoltaic solar cells. The most recent paper on CdS-Cu_2S cells was published by Martinuzzi [52] and in 1983 a book on fundamentals of solar cells was produced by Fahrenbruch and Bube [2] where they considered a variety of systems including CdS-Cu_2S thin film solar cells. However the progress on solar cell research and development including fundamental studies of devices, their deployment and economic problems can be followed most simply through the proceedings of the regular photovoltaic specialists conferences which have been organised by the I.E.E.E. in the U.S.A. since 1963, and by the Commission of the European Communities in Europe since 1977.

2.2 The Properties of Cadmium Sulphide Thin Films

2.2.1 General

Cadmium sulphide has found application as a semiconductor in many different systems including photovoltaic solar cells, photoconductive devices, light amplifiers, phosphors and electroluminescent devices, thin film transistors and diodes. This has stimulated enormous interest in cadmium sulphide and many laboratories throughout the world have established research programmes to study the structure, the electro-optical properties and the overall physical chemistry of this material.

Cadmium sulphide is a member of the technologically important II-VI group of compounds, with a direct band gap of about 2.4 eV at room temperature. It is n-type semiconductor as a result of sulphur vacancies, induced by the presence of excess Cd during film or crystal growth.

Although some workers have attempted to prepare p-type CdS, its existance has never been established beyond question that the tendency towards self-compensation is very strong in CdS. Initial studies of photovoltaic devices were made using single crystal materials. Subsequently ceramic and evaporated thin film cells were developed with the aim of providing low cost, light weight solar energy converters suitable for terrestrial applications.

2.2.2 CdS Film Deposition Techniques

CdS polycrystalline films can be obtained by various methods including vacuum deposition using either thermal evaporation or sputtering, chemical spraying, silk screen printing, sintering, chemical printing and electro phoretic deposition. Up to the present time, the highest efficiency thin film CdS - Cu_2S solar cells have been produced using vacuum deposition techniques [6, 49].

Developments in the fabrication of the CdS thin films and studies of their properties have been reviewed by Massie [53], Shirland [54], Crossley et al.[55], Perkins [56], Stanley [41] and more recently by Hill [42] and Bloss and Schock [49]. The first polycrystalline CdS thin films for solar cells were made by Carlson et al.[57]. Attempts have subsequently been made to reduce the bulk resistance of the CdS films in order to reduce the high series resistance for the CdS - Cu_2S solar cells. Gorski [58] tried to reduce the series resistance by means of more thickly deposited CdS films up to 100 μm. Other workers tried to reduce the resistivity of CdS films by doping with donor atoms. Three methods have been adopted for doping these films: (i) deposition of the dopant onto the completed thin films followed by annealing, (ii) introduction of the dopant into the CdS

source prior to evaporation, (iii) coevaporation of CdS and dopant using separate sources. In general when a doped evaporation source is employed, the dopant concentration in the film is different from that in the source material [59]. Indium has been the most common dopant usually introduced into the charge as chloride or sulphide. In one investigation, Shirland et al.[60] evaporated a series of films onto glass substrates from CdS charges which contained various concentrations of indium up to 1 mole %. In addition to its effect on resistivity, the dopant also caused a change in the optical transmission of the film which varied linearly with the doping level up to 0.1 mole %. Avignon et al.[59] used an electron beam method to evaporate In, I, Ag or Cu doped source material. It proved impossible to deposit CdS films doped with Al by doping the charge with $AlCl_3$. This is believed to be due to conversion of $AlCl_3$ to Al_2S_3, which has a very low vapour pressure [61]. Early CdS cells at the Clevite Corporation [60, 62, 63] were In-doped and gave reasonable efficiencies, as long as their thickness was over 5 μm. Doping with Zn was found to improve the ohmic contact with the substrate, but also lowered the efficiency. Doping by CuCl was found to lower the efficiency due to loss of the open-circuit voltage. An attempt to deposit $CdCl_2$ mixed with the CdS onto a pre-evaporated CdS film caused the latter to be attacked by chlorine [63]. On the other hand, David et al.[64] observed that doping with CuCl and $CdCl_2$ decreased the series resistance and improved the photovoltaic response. Also, Hill [42] found that a CdS charge composed of pure CdS in the bottom half of the ampoule and CdS + 0.01 % $CdCl_2$ in the top half of the ampoule, gave rise to a CdS thin film in which the resistivity was low at the back surface, leading to an improved contact with the molybdenum substrate and increased resistivity towards the outer surface. The conversion efficiencies of the cells made with these layers

were higher than those made with uniformly doped CdS layers, mainly due to an increase in the photogenerated current.

An easier and potentially more reproducible way to produce low resistivity CdS films for photovoltaic solar cells is to introduce donor native defects (sulphur vacancies) during the CdS deposition, which can be done by controlling the evaporation parameters such as substrate temperature, evaporation rate and the stoichiometry of the source materials. However, there are many conflicting reports in the literature concerning the influence of the deposition parameters on the properties of the resultant films. The majority of such studies have shown that the resistivity of CdS films increases with increasing substrate temperature and decreases with increasing the deposition rate. On the other hand, Wilson and Woods [65] found that, the resistivity decreased with decreasing the deposition rate and increasing the thickness of CdS films, while Arya et al.[66] observed a decrease in the resistivity as the substrate temperature was increased. Moreover, in the latter case, the CdS films had a higher resistivity when the source temperature was held at 1100°C than when held at 1050°C. This result was considered to be due to the composition of the CdS source material, which was deficient in sulphur.

CdS in the form of powder, crushed crystals or pellets can be used for evaporation. It is usual to contain the CdS in a quartz or carbon ampoule to avoid chemical attack of heated metal containers. Tantalum, for example, was found to get brittle after a short time of operation due to the formation of Ta_2S_5 [61, 67], spattering of CdS particles during the sublimation can be reduced by using a quartz wool or sintered glass plug. A comprehensive review of the vacuum deposition of CdS has been given by Stanley [41] and Hill [42]. Typical parameters for CdS deposition are: substrate temperature in the range of 200-250°C, source temperature about

1000°C, with deposition rate in the range of 1-1.5 μm min^{-1}.

A wide variety of substrates have been used for CdS thin film deposition. The most successful to date being, zinc-coated copper, molybdenum, and metallised Kapton for front wall cells, and glass with a transparent conducting coating (e.g. SnO_2, In_2O_3). The substrate must have a thermal expansion coefficient close to that for CdS. Molybdenum and Ni-Fe are both suitable in this respect, but Mo tends to oxidise at high substrate temperatures leading to poor adhesion of CdS film and to high contact resistance [42]. Adhesion problems have also been experienced with Ni-Fe substrates but it appears that these have now been solved [68]. Studies of growth of CdS on smooth and rough copper surfaces have shown [69] that the resistivity, the photoluminescence and the grain size were similar in both cases, but the adherance of the CdS on a smooth surface was not as good as on the rough surface.

2.2.3 Crystal Structure and Surface Topography of CdS Films

In general evaporated CdS films have a hexagonal wurtzite phase structure if the substrate temperature is higher than 150°C, [41,42,49,65], with a preferred orientation along the c axis, which is almost perpendicular to the substrate. The film consists of a thin base layer of randomly oriented crystallites covered by a thicker layer of highly oriented crystallites [70], forming a columnar grain structure. The presence of the cubic sphalerite phase is strongly temperature dependent, and also depends on the nature of the substrate, the presence of impurities and the rate of deposition [65, 71].

The orientation of the crystallites is not perfect but assumed to have

a range of angles with respect to the substrate. Foster [79] noted that films deposited on glass substrates were oriented at approximately 20°. Shallcross [72] has shown that the degree of preferred orientations increases with the thickness of the films. In addition Klerk and Kelly [73] and later Wilson and Woods [65] emphasized the influence of the deposition rate. They found that the degree of preferred orientation was increased by decreasing the deposition rate. It is evident that the degree of preferred orientation is a function of substrate temperature. At low temperatures the mobility is low and the orientation is poor [74].

Bujatti [75] investigated the effect of temperature gradients in the substrate, he found that below 280°C the temperature gradient has no effect, while in the range from 280° to 400° a temperature gradient of 50°C cm^{-1} reduced the preferential orientations by a factor of more than 3. Other authors [76-78] have shown that the columnar structure of CdS can be modified by doping. Chlorine, in particular, has been found to destroy the orientation, while indium and gallium, have a small influence and silver and sulphur appear to have no effect [79].

Problems of non-uniformity in the film thickness and c-axis orientation arise when large area films are being deposited from a single source. In an attempt to improve this situation by using a multiple source system [80], four sources have been employed in a square formation. The uniformity in film thickness improved substantially with this arrangement but the c-axis of the crystallites were found to be oriented as if there had been just one source.

Under appropriate evaporation conditions the columnar grains with a width of 2-5 μm in films exceeding a thickness of 20 μm can be achieved [49]. Shallcross [72] found a marked increase in grain size with increasing the substrate temperature, and lowering the deposition rate.

Transmission diffraction data have confirmed that the crystallite size was larger on the top surface than on the substrate surface. Improvements in crystallite size have been obtained recently using quasi-rheotaxy as reported by Romeo [81, 82].

Norian and Edington [83] have made a detailed study of the CdS microstructure. They determined the grain size, dislocation density and microscopic defect structure of CdS films. The topography of the CdS surface was seen to contain hills and valleys. The hills were found to be faceted and were approximately 5 μm high with a base line between 10 and 15 μm.

An attempt was made at RCA [84] to improve the cell performance by reducing the number of grain boundaries and increasing the grain size by re-crystallization of the CdS layer. Various annealing treatment have subsequently been reported, such as annealing in vacuum [85, 86], or in a variety of different gas atmospheres, for example, argon, nitrogen, oxygen, and cadmium vapour [87-89] and utilization of a Cu or Ag enhanced recrystallization [90, 91]. These processes have been shown to produce significant changes to the crystal structure of the films and the work of Dresner and Shallcross [76] indicated that carrier mobilities approaching those of single crystal samples could be achieved. At the same time the resistivities of the films could be controlled by appropriate doping during the recrystallisation. Boer [92] has also studied this effect, and found that annealing the evaporated CdS layer at 620° to 650°C in a nitrogen atmosphere containing HCl, copper, cadmium, sulphur and traces of oxygen resulted in a significant improvement of photoelectric properties.

In an effort to increase the grain size from an initial 2 - 5 μm to greater than 30 μm some CdS films have been heated in evacuated quartz ampoules at temperatures ranging from 55°C to 700°C for up to 96 hours

[93]. The resulting grain growth was not consistent across the films or across different samples from the same substrate, but a few large irregular grains with widths in excess of 100 μm were observed in some of the films.

Having prepared films with the required thickness and properties an etching treatment has been found to be one of the most important steps in the formation of high output frontwall CdS - Cu_2S cells. The etching is usually done just prior to formation of the Cu_2S layer, using strong HCl solution. The etching has two directly observable effects [94, 95], it textures the film surface with pyramid structures, and it forms deep etch pits. The degree of surface texturing of the CdS films has been found to vary directly with time, temperature and acid concentration, but the degree of pitting seems to be more strongly affected by the time of the etch than by the temperature and acid concentration [94]. The effect of texturing is to reduce the light reflection losses and hence to increase the photon absorption leading to a higher cell current. It has been suggested that the etching opens the grain boundaries in the CdS film thus encouraging deeper penetration of the Cu_2S layer during the subsequent barrier formation [96]. The deep etch pits have generally been considered harmful since they lower the internal shunt resistance of the cell and can cause short circuits. However Shirland [100] has suggested that the etch pits might be helpful to cell output by providing a channel for the Cu_2S layer to form laterally in the grain boundaries intersecting the walls of the deep etch pits. Also, he could not detect any opening of grain boundaries that could be attributed to the HCl etch, but Norian and Edington [83] observed that etching produced crevices at the grain boundaries sites.

2.2.4 Point Defects in CdS Thin Films

As would be expected in the case of such a technologically important

material, extensive work has been done on the characterization of localised defect and impurity states in CdS. The aim has been both to provide information about the properties of such states and to determine their origin in relation to specific physical defects in the material. Much of this work has, of course, been concerned with single crystal material but with increasing interest in the films, more attention is now being paid to the characterization of these systems. In an earlier investigation Brandhorst et al.[97] reported the existence of a number of deep levels, which were present in evaporated CdS. The identity of the various levels is not well known, but assignment of the most probable identities has been made. States of 0.05, 0.14 and 0.25 eV below the bottom of the conduction band have been found most frequently in cadmium rich samples and were assumed to be associated with sulphur vacancies, while the 0.61 eV centre was seen in sulphur-rich material. In contrast, levels lying at 0.41 and 0.82 eV below the conduction band usually occur together and are present in both sulphur-rich and cadmium-rich samples. Oualid and coworkers [98] used a deep level capacitance transient technique to determine the energy and the capture cross section for the electron traps found in their evaporated CdS layers. They confirmed the existence of traps at 0.05, 0.15 and 0.25 eV below the conduction band with the 0.15 eV level (identified with the doubly ionised sulphur vacancy) being dominant. Besomi and Wessels [99] observed eight different traps, with trap depths ranging from 0.16 to 0.96 eV while the concentration of the traps ranged from 10^{13} cm^{-3} to 10^{15} cm^{-3}. They also found the characteristic DLTS spectrum to be dependent on the grain size of the polycrystalline CdS films, but in view of the non-uniformity of grain structure across any film and the change in growth conditions required to bring about variations in the structure, it is difficult to draw definite conclusions about the

influence of grain size alone on the electrical characterisitics of the films.

2.3 The Properties of Copper Sulphide

2.3.1 Composition of Copper Sulphide

It seems that many of the durability problems which have plagued CdS - Cu_2S solar cells through their history can be traced to the departure of the stoichiometry of the copper sulphide layer towards a more sulphur-rich composition.

The properties of copper sulphide layers have been studied by a number of investigators, and much of the data has been discussed by Stanley [41], and later by Hill [42], Savelli and Bougnot [44], and very recently by Fahrenbruch and Bube [2]. A number of characterization methods have been developed based on morphology [100], cathodoluminescence [101], electron chemical analysis (ECA) [102], transient and galvanic electrochemical measurements [96] and so on. Much of this work has been concerned with copper sulphide in the role of a photovoltaic cell absorber. Copper sulphide is known to exist in a number of crystallographic phases. The phases which are known to be stable at room temperature include Cu_2S (chalcocite), $Cu_{1.96}S$ (djurleite), $Cu_{1.8}S$ (digenite), $Cu_{1.75}S$ (anilite) and CuS (covellite). However, the value of x in the Cu_xS need not be exactly equal to those just given above. For example, Cook and coworkers [103] found that at room temperature chalcocite can have values between 1.995 and 2.0, and djurleite between about 1.91 and 1.96, etc. The structure and the associated crystallographic constants of the various phases in the Cu-S system have been studied by Cook et al.[103] and others [104-106] and the

relevant data are shown in table (2-1). In addition to these forms, Russell and Woods [107] have observed a complete phase transformation at the surface of a sample which originally had the djurleite phase. The new phase had a hexagonal structure with lattice parameters a = 1.524, c = 1.32 nm, but no value of x for this phase was reported. The chalcocite phase with an orthorhombic structure at room temperature has been found to convert to hexagonal at 104°C, djurleite with an orthorhombic structure at room temperature transforms to tetragonal at 86-93°C and to cubic at 100°C, and digenite with pseudo-cubic structure at room temperature transforms to cubic at 78°C [108, 109].

In the formation of Cu_xS on CdS, two Cu atoms replace a Cd atom, with the sulphur sublattice remaining relatively unchanged [110]. Similarly, throughout the phase changes in the Cu_xS, it is thought that the sulphur sublattice again remains relatively stationary with the Cu atoms moving around it to form the various phases. In a stoichiometric crystal there are two Cu^+ ions associated with each S^{2-} ion [111]. Deviation from the composition of Cu_2S are affected by removing Cu^+ ions from the crystal and three types of atomic imperfections follow; the effectively neutral Cu vacancy generated by a Cu^{2+} ion in place of two Cu^+ ions, the effectively negatively charged vacancy generated by one missing Cu^+ ion, and an association of these two defects.

2.3.2. Optical Characteristics

The optical absorption and electrical properties of this material are extremely important in obtaining the optimum generation and collection of carriers in the solar cell in which it is employed. Since the structure

Table (2-1) Structure and lattice constants of relevant phases of Copper Sulphide.

phase		structure	Lattice Constant (nm)		
			a	b	c
Cu_2S	Chalcocite	orthorhombic	1.1848	2.733	1.3497
		Hexagonal	0.391	-	0.6722
$Cu_{1.96}S$	Djurleite	orthorhombic	1.571	1.356	2.684
$Cu_{1.8}S$	Digenite	Pseudo-Cubic	0.556	-	-
$Cu_{1.75}S$	Anilite	orthorhombic	0.789	0.784	1.101
CuS	Covellite	Hexagonal	0.3794	-	1.633

and crystalline parameters of the different copper sulphide phases vary with composition, it is expected that there will be corresponding variations in the band gap, absorption coefficient and the resultant spectral response of the completed device.

Chalcocite (Cu_2S) possesses a high absorptivity in the visible region of the solar spectrum, and high transmission in the infrared. However, the published optical and other properties of Cu_2S show extremely wide variations. For example, there have been widely different values reported for the band gap at room temperature. Although two optical absorption thresholds are observed in several studies, it is not clear whether both of them coexist in the same phase. Mulder [112] studied the optical absorption spectra of various copper sulphide phases, and has inferred that chalcocite phase has an indirect transition at about 1.2 eV and what is most probably a direct transition in the range of 2-2.5 eV. On the other hand, cathodoluminescence studies of Cu_2S have indicated that a luminescence peak at about 1.2 eV, which appears to be associated with chalcocite phase [113], has a shape like that which one would expect for band-to-band transitions in a direct band gap material [101]. Similarly Rothwarf and Windawi [114] calculated the relation between the absorption coefficient and sheet resistance for degenerate Cu_2S, and compared the results with existing experimental data on material prepared in the same way as for solar cells. They found good agreement between the experimental data and their calculations assuming that Cu_2S is acting as a direct band gap semiconductor. However the non-ideal structure of copper sulphide films creates uncertainty in the numerically deduced values and therefore makes the assignment of the direct or indirect nature of the absorption edge correspondingly uncertain. In spite of this uncertainty, there is no doubt that there is an absorption edge at about 1.2 eV at room

temperature, and this agrees with the cut-off observed at this energy in the spectral response of $CdS-Cu_2S$ solar cells.

2.3.3. Electrical Properties

Copper sulphide is a p-type material because Cu vacancies act as acceptors and their density determines the majority carrier concentration and hence the position of the Fermi level. Acting as the absorber layer in a front-wall photovoltaic cell, the two electrical properties of a copper sulphide layer which play particularly important roles are the sheet resistance and the diffusion length of the minority carriers which are created by absorption of the incident radiation as discussed in the previous section.

The minority carrier diffusion length in copper sulphide was measured by Gill et al.[115] using a light microprobe to scan the bevelled junction region of $CdS - Cu_xS$ solar cells. The value of the diffusion length was found to be between 0.1 to 0.4 µm for Cu_2S (chalcocite), while for djurleite and digenide the value was found to be much less [116] (~ 50Å). Subsequent measurements made using the Electron Beam Induced Current (EBIC) technique [117] were found to be in agreement with these observations.

The electrical properties of copper sulphide have been measured by a number of workers. The Cu_2S phase has the lowest electrical conductivity in the Cu-S system by virtue of being the least defective. This is clearly shown by the resistivity data of Guastavino et al.[118]. The high conductivity of digenite is due to the increasing concentration of neutral vacancies, which allow the formation of a large number of negatively charged vacancies and free holes. Measurements of resistivity, Hall mobility and carrier concentration have been listed by Stanley [41] and

also by Savelli et al.[44].

The electrical resistivity of Cu_2S films which show optimum photovoltaic performance lies in the range between about 10^{-2} to 10^{-1} Ω cm. This value corresponds to a carrier density greater than 10^{20} cm^{-3}, with mobility measurements indicating values between 1 to 10 $cm^2/V.s$ [118]. The mobility has been found to be less dependant on the stoichiometry of the copper sulphide [119] than the other electrical parameters. Windawi [120] has measured the carrier concentration of chalcocite phase (Cu_2S) and found a value of 10^{21} cm^{-3}, which accords with copper sulphide being degenerate with the fermi level 0.2 eV inside the valence band. As the properties of a heterojunction are dependent on the electron affinity difference between the constituent materials, a direct measure of the electron affinity for copper sulphide is clearly desired. Indirect measurements have lead to some disagreement. Schewchun et al.[121] suggested a value close to that of silicon (4.05 eV), this suggestion has been inferred on the similarity between CdS-Si and CdS-Cu_2S solar cells [122]. Pfisterer et al.[123] indicated a value of 4.2 eV, and Duchemin et al.[124] gave an electronic affinity value of 4.4 eV. Unfortunately, direct measurement based on photoemission edge studies are difficult in the case of copper sulphide because it cannot be cleaved.

2.3.4 Film Fabrication Processes

It is clear from what has been said before, that the chalcocite phase is needed in order to achieve high efficiency cells, and a well-controlled method of film preparation is therefore required in order to produce Cu_2S layers with reproducible characteristics. Several methods for copper sulphide film fabrication have been investigated, including the chemiplating process (the so-called wet process), vacuum deposition, the

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solid state reaction (the dry process), various spraying techniques, and sulphurisation of Cu films. For the purposes of $CdS-Cu_2S$ solar cell fabrication, it is the dipping process which has been the most frequently adopted method and it is this process which has produced cells with the highest efficiency [6, 49]. In this method the Cu_xS layer is formed by dipping the pre-etched film of CdS into a hot solution of CuCl. A topotaxial layer of Cu_xS is formed by chemical displacement of Cd from the lattice of CdS crystallites by Cu^+ ions. Salkalachen et al.[125] found that the pH of the CuCl solution plays an active role in controlling the Cu_xS growth processes. With a pH value of 4.6 the film thickness was observed to increase with time parabolically while in solutions of lower pH (about 3.4) a fast linear growth mechanism was dominant. Other factors which influence the Cu_xS layer growth process are the grain size and morphology of the CdS parent surface and the relative concentrations of cadmium and sulphur atoms at this surface [126].

A disadvantage of the wet method is that it requires a CdS film with a thickness of about 25µm or more. This is due to the fact that the Cu_xS penetrates deep into the grain boundaries of the CdS [83, 127, 128] and can thus cause shorting paths to the substrate on thin CdS films.

In considering the thickness of the chemically converted layer it is important to realise that care must be exercised in interpreting empirical data. Due to the textured surface structure of CdS substrate and deep protrusions of copper sulphide into the grain boundaries, there is considerable non-uniformity in the thickness of the copper sulphide layer. It follows that the mid-grain thickness is much less than the average equivalent flat surface thickness. In cells exhibiting good conversion efficiencies, Cu_xS thickness in the range of 0.1 - 0.4µm have been reported [6, 47, 52, 129]. It is usually found that deviation from stoichiometric

composition occurs during the formation processes. However, this thesis describes an attempt to investigate the copper sulphide stoichiometry during the formation processes and subsequent annealing treatment, (section 5.1.2).

2.4 Properties of CdS - Cu_2S Solar Cells

2.4.1. Cell Structure and Stability

Although photovoltaic devices based on thin film CdS - Cu_2S heterojunctions with solar energy conversion efficiencies of up to 10% have already been demonstrated [10], problems relating to reproducibility and long-term stability of these devices still remain to be solved before their full potential can be realized. It is clear that changes in the properties of any component part of a cell during operation can contribute to a reduction in its efficiency but, in front-wall CdS - Cu_2S cells, it is the very thin Cu_2S layer, (<0.5 μm thick), in which the majority of photocarriers are generated, and the adjacent regions of the CdS layer in the vicinity of the heterojunction which are crucial in determining both the initial efficiency and the subsequent operational stability. Both the active layers, and the junction itself, are strongly influenced by the post-fabrication annealing which is an important step in most cell manufacturing procedures. In general, the effects of a short annealing treatment are a reduction in the dark current of the device, and an increase in the light-generated open-circut voltage, short circuit current and fill-factor, with a consequent increase in the overall conversion efficiency. However, the annealing conditions required to optimise the cell characteristics have been the subject of some uncertainty. For

example, reports indicating the benefits of a short bake in air [130, 131] have been followed by others [132, 133] attributing detrimental effects to the presence of oxygen. Such uncertainty is not surprising in view of the combination of effects which occur during heat treatment. These effects include the desired diffusion of copper from the Cu_2S into the CdS in order to broaden the space charge barrier in the CdS layer at the interface. This effect can be accompanied by diffusion of copper along grain boundaries with the possibility of shorting paths being generated between the Cu_2S layer and the back contact to the CdS (in front-wall cells). Furthermore any loss of copper from the Cu_2S layer via this mechanism or via interaction with the atmosphere degrades the stoichiometry of Cu_2S and thereby reduces its photon absorption coefficient and, consequently, the light-generated current in the device [47]

Two different techniques have been employed with a view to preventing a loss of copper from the front surface during post fabrication heat treatment. One method is to carry out the annealing in a reducing atmosphere such as carbon monoxide [134] or hydrogen [135, 136] in order not only to avoid copper oxide formation but also to reduce any previously formed copper oxides to the metal and thereby increase the Cu/S ratio towards its optimal value of close to 2 [137]. The second technique for avoiding loss of copper from the Cu_2S during post-fabrication is to deposit a thin film of copper onto the Cu_2S layer before annealing in air or oxygen [138]. This treatment results in a much improved operational stability but, although the processes giving rise to the observed changes in electrical characteristics during the oxygen/air annealing treatment are reasonably well understood [139, 201], an explanation for the stability acquired by cells as a result of this treatment has not progressed beyond the proposition that the process leads to the formation of a protective

copper oxide film over the device. This matter has formed one component of the present study and is considered again in later sections of this thesis.

While diffusion processes occurring at the heterojunction interface and within the grain boundaries are obviously of great importance in relation to the stability of thin film solar cells, the complex non-planar morphology of the CdS - Cu_2S system has severely hampered the development of a satisfactory analysis of these processes. It has previously been mentioned that diffusion of copper into the CdS substrate layer is a desired feature of post fabrication annealing. Diffusion of copper from metal layers into single-crystal CdS has been studied by a variety of techniques such as radiotracer methods [140], optical transmission [141], and electrical capacitance [142]. The radiotracer technique was similarly used [143] to study copper diffusion from a thick Cu_2S layer into single-crystal CdS. Diffusion profiles for polycrystalline CdS layers are expected to be drastically different from single-crystal profiles owing to the presence of the complex grain structure, and this has been clearly demonstrated by recent, mainly qualitative, studies using transmission and scanning electron microscopy [83], electrochemical analysis (ECA) [125, 133], atomic absorption spectroscopy [144], x-ray photoelectron spectroscopy [145] and Auger electron spectroscopy (AES) [144 — 149]. For such data to yield quantitative information concerning the grain and the grain boundary diffusion parameters, some assumptions need to be made concerning the physical structure of the cells, as discussed in chapter 3.

2.4.2. CdS - Cu_2S Junction Models

Since the discovery of the photovoltaic effects in copper/cadmium

sulphide many models have been proposed to explain the conduction characteristics both in the light and in the dark. These models have been summarized by Van Aerschodt et al.[31] and Stanley [41] and later by Hill [42] and Savelli et al.[44].

The concept of the CdS - Cu_2S heterojunction was first proposed by Cusano [36] and supported by Keating [150]. Before that Woods and Champion [151] and Grimmeiss and Memming [152] had suggested that the cells operated as p-n homojunctions, while Williams and Bube [153] suggested that the observed phenomena were associated with some kind of metal-semiconductor junction. The evidence from the Clevite Group [154] confirmed that the device was indeed a p-n heterojunction. In the Clevite model the cells were essentially considered to have a p-i-n structure, with a nearly degenerate p-type layer of cuprous sulphide, an approximately intrinsic layer of cadmium sulphide (~1μm) compensated by copper introduced during a post-fabrication heat treatment at 200°C and an n-type layer of CdS as shown in figure (2-1). The experimental observations made by the Clevite Group were explained in terms of the behaviour of the intrinsic layer in the cadmium sulphide. This layer, being photoconductive, was assumed to introduce an illumination dependent series resistance. A similar model was proposed by Mytton [155], but Van Aershodt et al.[31] criticised the Clevite model in view of the lack of evidence for a high series resistance in the observed forward bias I-V characteristics taken in the dark. As an alternative Van Aershodt [31] suggested that the experimental observations could be explained in terms of a model in which the barrier height and the occupancy of interface states changed under illumination.

In the early model proposed by the Stanford Group [130, 156], it was considered that the heterojunction had a conduction band spike and that

tunnelling through this spike played the major role in determining the cross-junction current. A conduction band spike was similarly postulated by Te Velde [131] who considered that the height of the spike was dependent on the quantity of oxygen which penetrated the Cu_2S layer during post-fabrication heat treatment to form electron traps at the CdS - Cu_2S interface. According to the Stanford model, however, it was the width of the spike which was influenced by heat-treatment as a result of copper diffusing into the CdS space charge region and generating deep states within the band gap. As the occupancy of these states would change with illumination, the width of the conduction band spike and, hence, the electron tunnelling probability would, similarly, be influenced by the incident radiation. Figure (2-2a) shows the early model of the Stanford Group. In the dark, the occupied, deep acceptor states partially compensate the ionised donors and widen the space charge layer while, under illumination, the effects of hole trapping by the acceptors causes the space charge layer width to be significantly narrowed.

In the light of further experimental data, this model was modified to incorporate a negative conduction band discontinuity thus eliminating the conduction band spike to produce the interface structure shown in figure (2-2b). The general principles of this model have since been supported by others including the Delaware Group [47, 157] and by Martinuzzi and coworkers [158] although there is still some dispute concerning quantitative details such as the magnitude of the conduction band discontinuity ΔE_c for which values between 0.14 eV and 0.35 eV have been quoted. Other details such as the location of the Fermi energy and the space charge layer width clearly depend on the cell fabrication conditions.

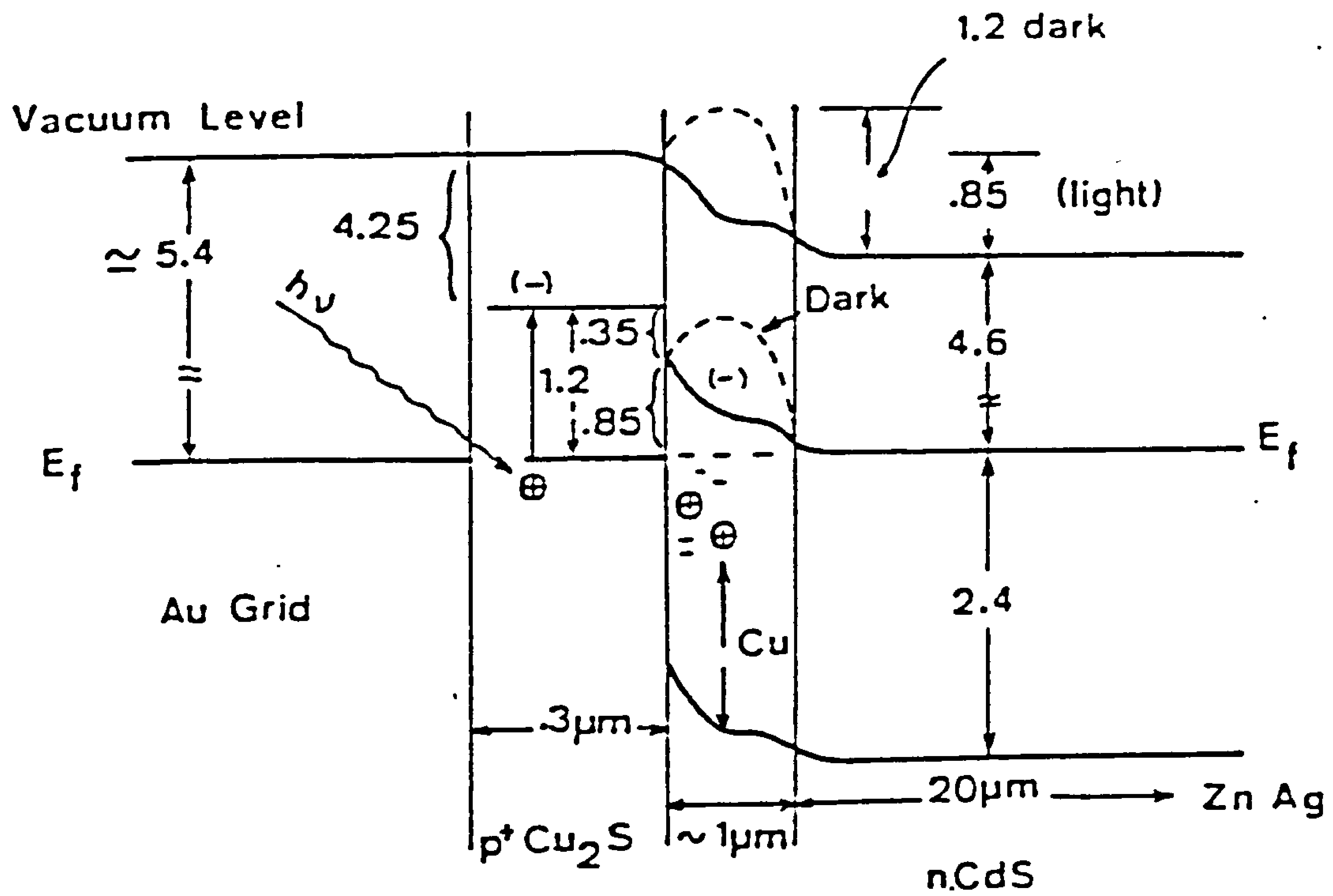
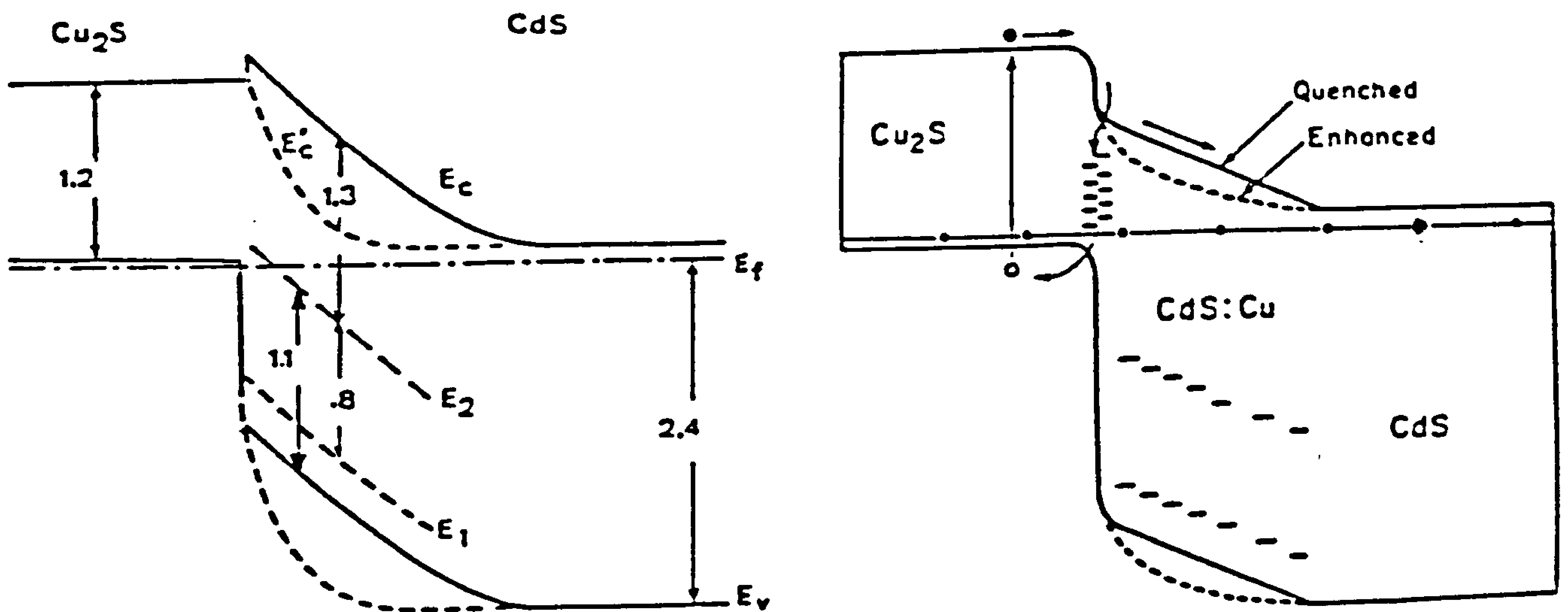


Figure (2-1) Clevite model (ref. 154)
(Energy in eV)



(a) The early model (ref. 130).

(b) The recent model (ref.32)

Figure (2-2) Stanford model (Energy in eV).
The solid lines show equilibrium band profile and the dashed lines show the steady band profile under illumination.

2.4.3. Photovoltaic Properties of CdS - Cu_2S Solar Cells

As mentioned above, the electrical characteristics of a practical cell depend very much on the fabrication process and post-fabrication treatments. However, the junction model shown in figure (2-3) has evolved as a result of a variety of different types of investigation and can be used to account for the majority of basic operational features and anomolous effects which have been observed.

The fundamental cross-junction charge transport processes which can occur in heterojunctions are discussed in chapter 3. In the case of CdS - Cu_2S cells, it has been found that more than one transport mechanism is generally in operation [159]. As might be expected, it is often found that the dominant mechanism is dependent on the temperature. At temperatures below 0^oC, Martinuzzi and coworkers [158, 160] obtained I-V characteristics which were consistent with a multi-step tunnelling process as proposed by Riben and Fencht [161] while, at higher temperatures, the current became progressively more thermionic in nature. This is in accord with the observations at the Delaware Institute of Energy Conversion [47] where the room temperature I-V characteristics for cells which had been given some post-fabrication heat-treatment were found to fit the relationship:

$$J = e A_J N_{c2} S_I \exp\left(-\frac{\phi}{kT}\right) \left[\exp\left(\frac{e (V - J R_s A_\perp)}{n kT}\right) - 1 \right] - \frac{V}{R_{sh} A_\perp} - J_L \quad (2\text{-}1)$$

where A_J is the junction area, $A_\perp$ the planar area, N_{C2} the effective density of states at the band edge of the CdS, S_I the interface recombination velocity, ϕ the barrier height at the junction, e the electron charge, n the diode ideality factor and J_L is the light-generated current. On cells which had been freshly made, the I-V data

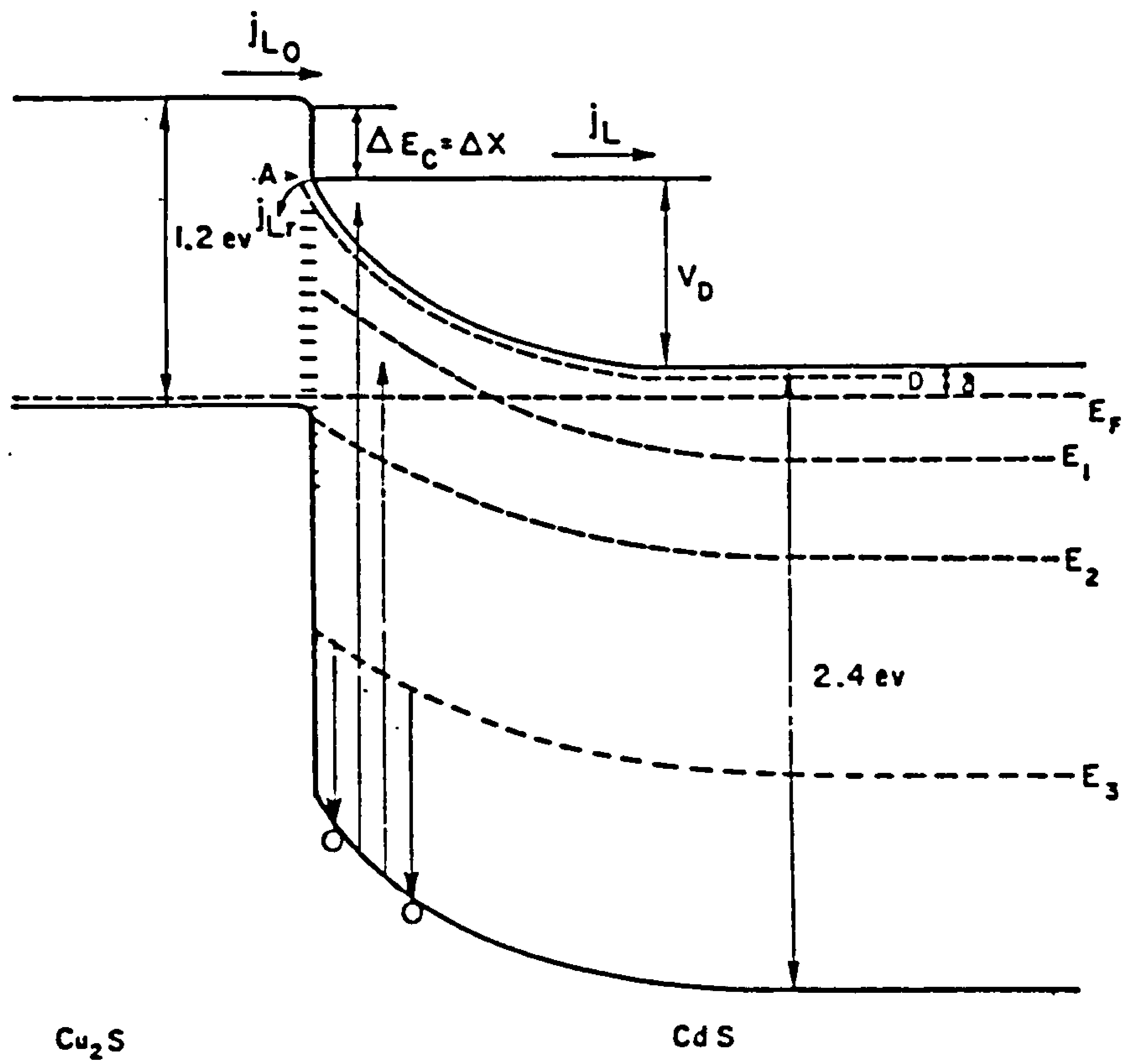


Figure (2-3) Energy band-diagram proposed by Delaware group (ref. 47).

could be explained in terms of electrons tunnelling through the barrier. It seems that the effect of copper diffusion during the post-fabrication heat-treatment was to broaden the barrier sufficiently to make the tunnelling mechanism less probable than thermionic excitation over the barrier with subsequent recombination of carriers via interface states.

Setting J = o in equation (2-1) the open circuit voltage can be expressed as

$$e V_{oc} = E_{g1} - \Delta\chi + kT \ln J_{sc} - kT \ln e N_{c2} S_I - kT \ln \left(\frac{A_J}{A_\perp}\right) \quad (2\text{-}2)$$

For $eV_{OC} \gg kT$ where Eg_1 is the energy gap of Cu_2S, J_{SC} is the short-circuit current ($\approx J_L$), and $\Delta X = \Delta E_C$ the electron affinity difference between the Cu_2S and the CdS. Experimental values for the open circuit voltage up to 0.53 V have been reported but it can be seen from equation (2-2) that the parameters ΔX, S_I and $A_J/A_\perp$ are all important in maximising the open circuit voltage. ΔX and S_I are directly related to fundamental material properties, and can only be changed significantly by changing materials. An improvement has been accomplished by the use of $Zn_x Cd_{1-x}S$ in place of CdS, with the result that open-circuit voltages of the order of 0.7 V have been reached [162]. It seems that the optimum value for x in $Zn_x Cd_{1-x}S$ will be about 0.15 - 0.2, but while improving the open circuit voltage, the use of this alloy has, so far, always been accompanied by a reduced cell current. In the best CdS - Cu_2S cells, AM1 (or Air Mass 1 represents the solar spectrum at the earth's surface when the sun is at the zenith, the incident power is about 100 mW cm^{-1}) currents of 25-26 mA cm^{-2} have been achieved, but due to recombination at the interface, the light-generated current flowing in the external circuit is not the full current generated in the absorber layer. It follows that the short-circuit current density J_{SC} (when V = o) can be expressed as a function of

the maximum generated current [47] thus

$$J_{sc} \simeq J_L = J_{L_o} \frac{\mu F}{S_I + \mu F} \tag{2-3}$$

where J_{Lo} is the currnt density generated in the Cu_2S such that $J_L = J_{Lo} - J_{LR}$, J_{LR} being that part which is lost by recombination via interface states. J_{Lo} is itself a function of the incident photon flux and the opto-electronic characteristics of the absorber material (Cu_2S), The fraction of J_{Lo} which flows across the junction depends on the electron mobility in the CdS and F the electric field at the interface as well as on the interface recombination velocity.

The field in the CdS space charge region at the junction is a very important parameter in determining the short circuit current. For an ordinary space charge region dominated by shallow donors, under short-circuit conditions, this field can be written as [47]

$$F\ (V = 0) = \frac{2\ V_D}{W} = \frac{e\ N_D^{*}\ W}{\varepsilon \varepsilon_o} = \left(\frac{2\ e\ V_D\ N_D^{*}}{\varepsilon \varepsilon_o} \right)^{1/2} \tag{2-4}$$

and for finite voltages

$$F\ (V) = \left[\frac{2\ e\ N_D^{*}\ (V_D - V)}{\varepsilon \varepsilon_o} \right]^{1/2} \tag{2-5}$$

where V_D is the diffusion voltage, W is the width of the space charge region. The electric field F is dependent on the net ionized donor density N_D^* in the space charge region or on the net positive space charge near the junction. An increase in the effective value of N_D^*, narrows the space charge region and increases the value of F. When light reaches the CdS space charge region and causes an increase in N_D^*, there is a corresponding increase in F (equation 2.5) and, therefore, an increase in

J_L (equation 2.3). Since 1976 the interface recombination model shown in figure (2-3) has been found to account for most of the well documented phenomena observed in CdS - Cu_2S cells including : the increase in the capacitance of the cell with light [47, 162, 163], the cross over between dark and light I-V characteristics, the enhancement of the short-circuit current by short wavelength light and quenching by long wavelength light, and the time-dependent phenomena all of which stem from the trapping of carriers in deep levels in the compensated region of the CdS layer near the junction.

Chapter 3

Theoretical Consideration

3.1 The photovoltaic effect

When a photon of energy equal to the energy band-gap of a semiconductor is absorbed, an electron is excited from the valence band to the conduction band. Absorption of such photons thus produces an increase in the density of electrons in the conduction band and an exactly equal increase in the density of holes in the valence band. Photons having less energy than the band gap will not be absorbed, and therefore cannot contribute to the generation of free charge carriers, while photons having an energy greater than the band gap will be absorbed and will generate free charge carriers, but for each quantum absorbed, the excess over the band gap energy value will be wasted as heat.

In order to produce a photovoltaic effect, two requirements must be met, one the generation of free charge carriers (electrons and holes) due to the incident light and the other, the presence of a built-in field to separate the positive and negative charges and drive them to their respective collecting electrodes without any substantial loss. The photovoltaic efficiency thus depends essentially on the ability of the solar radiation to generate free charge carriers and that of the built-in-field to separate them. The ability of solar radiation to generate charge carriers is determined by the band gap of the material involved and the spectral dependence of the photon absorption coefficient. The ability of the built-in-field to drive the charge carriers to their respective electrodes for collection without any appreciable loss depends upon the mobility of the charge carriers, the carrier diffusion and recombination

parameters and the junction characteristics of the system providing the internal field (e.g. p-n homojunction, heterojunction, schottky barrier). One can see that the electrical and the structural properties of materials constituting solar cells are critically important in determining the overall photovoltaic efficiency.

3.2 The P-N Junction Photovoltaic Converter

3.2.1 The ideal case

To derive the ideal conversion efficiency for a photovoltaic device, we shall first consider the energy-band diagram for an ideal p-n junction under solar radiation as shown in Fig. (3-1).

When the solar radiation is incident normally on one face of the semiconductor, the number of photons absorbed per unit time per unit volume is equal to $P_{in}\,\alpha/h\nu$, where P_{in} is the radiation density, α the optical absorption coefficient, and $h\nu$ the energy of incident photon. The absorption of these photons causes the electron and hole concentration to increase at a rate R_G as [42]

$$R_G = P_{in}\,\alpha\,Q\,/\,h\nu \tag{3-1}$$

where Q is the quantum efficiency.

In equilibrium, the rate of generation of electron-hole pairs is equal to their rate of recombination, which can be written as $\Delta n/\tau_e$ in p-type semiconductors and $\Delta p/\tau_h$ in n-type semiconductors, where τ_e and τ_h are the recombination lifetimes of excess minority electrons and holes. Thus

$$\begin{aligned} \Delta P &= P_{in}\,\alpha\,Q\,\tau_h\,/\,h\nu \\ \Delta n &= P_{in}\,\alpha\,Q\,\tau_e\,/\,h\nu \end{aligned} \tag{3-2}$$

The equivalent circuit for an ideal p-n junction is shown in Fig.

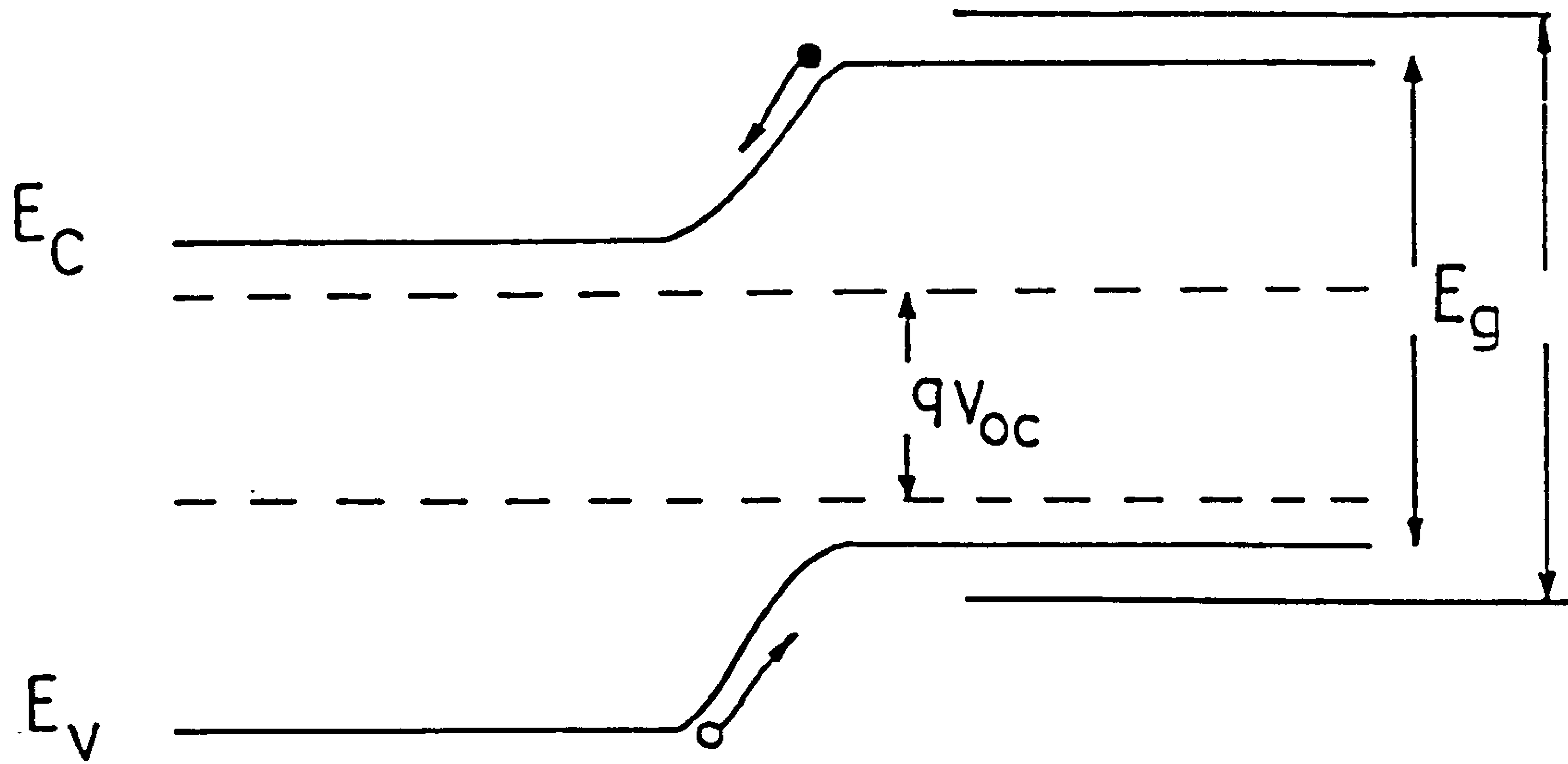


Figure (3-1) Energy-band diagram of a p-n junction solar cell under solar irradiation.

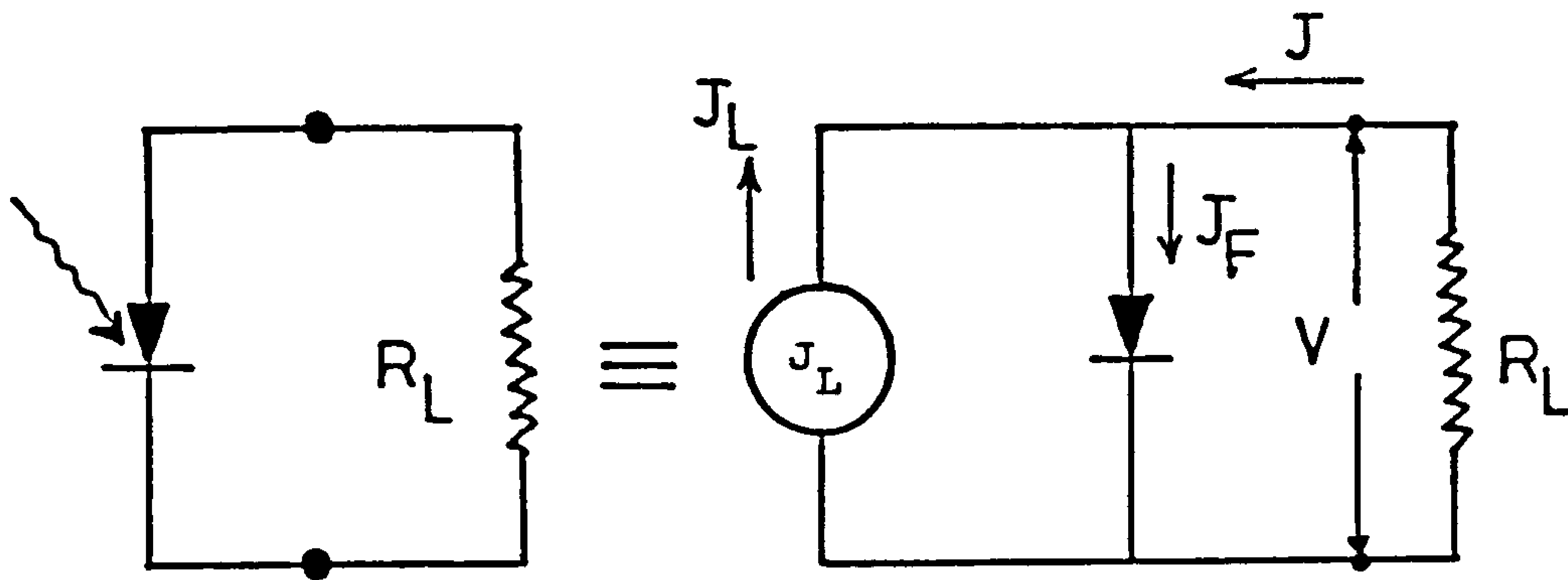


Figure (3-2) Idealized equivalent circuit of a solar cell.

(3-2) where the photogenerated current is represented by the constant current source, J_L, in parallel with the junction. The forward current density, J_f, in the dark, due to the forward voltage V across the junction is given by

$$J_F = J_s\,(e^{eV/kT} - 1) = J_s\,(e^{\beta V} - 1) \qquad (3\text{-}3)$$

where $\beta = \frac{e}{kT}$, and J_s is the reverse saturation current density, which results from the thermal generation of minority carriers within the semiconductor.

The J-V characteristics of such a system can be obtained using Kirchhoff's laws, from which it can be seen that the current through the external load, R_L is given by

$$J = J_F - J_L = J_s\,(e^{\beta V} - 1) - J_L \qquad (3\text{-}4)$$

As the forward voltage across the diode increases, the forward current must increase until at open-circuit voltage, the forward current is equal to the reverse photogenerated current and the current through the load, R_L, is zero. Then from eq. (3-4) we obtain

$$J_L = J_s\,(e^{\beta V_{oc}} - 1) \qquad (3\text{-}5)$$

and

$$V_{oc} = \frac{1}{\beta}\ln\left(\frac{J_L}{J_s} + 1\right) \qquad (3\text{-}6)$$

since $J_L >> J_s \Rightarrow \frac{J_L}{J_s} >> 1$, then eq. (3-6) becomes

$$V_{oc} = \frac{1}{\beta}\ln\left(\frac{J_L}{J_s}\right) \qquad (3\text{-}7)$$

The current J_L in eq. (3-5), (3-6) and (3-7) shifts the J-V characteristics along the current axis by an amount $-J_{SC}$, where J_{SC} is the short-circuit density and is nearly independent of voltage. Eq. (3-7) shows that for a given J_L, the open-circuit voltage increases logarithmically with decreasing reverse saturation current density J_S.

This open_circuit voltage is directly dependent on the junction potential barrier which itself is dependent on the band gap of the semiconductor.

The reverse saturation current density can be written as,(42, 164)

$$J_s = n_p \, e \frac{L_e}{\tau_e} + P_n \, e \frac{L_h}{\tau_h} \qquad (3\text{-}8)$$

where τ_e and τ_h are the electron and hole recombination times. n_p is the concentration of electrons in the p-region, p_n is the concentration of holes in the n-region, and L_e and L_h are the diffusion lengths for the electrons and holes respectively. Eq. (3-8) shows that J_s depends on the minority carrier densities and on the ratio of minority carrier diffusion length and recombination time. When the solar cell is illuminated, photons are absorbed and the carrier densities are increased from n_p to $n_p + \Delta n_p$ and from p_n to $p_n + \Delta p_n$. Then the saturation current density becomes

$$J'_s = (n_p + \Delta n_p) \, e \frac{L_e}{\tau_e} + (P_h + \Delta P_h) \, e \frac{L_h}{\tau_h} \qquad (3\text{-}9)$$

or

$$J'_s = J_s + J_L \qquad (3\text{-}10)$$

The photogenerated current J_L can thus be written as

$$J_L = \Delta p \, e \left(\frac{L_e}{\tau_e} + \frac{L_h}{\tau_h}\right) \qquad (3\text{-}11)$$

or

$$J_L = \frac{P_{in} \, \alpha \, Q}{h\nu} \, e \, (L_e + L_h) \qquad (3\text{-}12)$$

The magnitude of the factor $P_{in} \, \alpha Q/h$ depends on both the semiconductor and the solar radiation.

The condition for maximum power output for the device as indicated by the point P_m on the J-V characteristic shown in fig. (3-3), can be obtained by putting

$$\frac{d}{dV}(J\ V) = 0$$

The maximum power is delivered when the load impedance is properly matched giving

$$P_m = J_m V_m = FF \cdot J_{sc} \cdot V_{oc} \qquad (3.13)$$

where FF is the fill-factor, which depends upon the sharpness of the J-V characteristic curve. This factor relates the maximum power which a cell can deliver to the short-circuit current J_{sc} and open-circuit voltage V_{oc}, and is given by

$$FF = \frac{J_m V_m}{J_{sc} V_{ov}} \qquad (3\text{-}14)$$

The power conversion efficiency is defined as a ratio of power output per unit cell area and input power density. Thus, the efficiency is given by

$$\eta = \frac{J_m V_m}{P_{in}} \times 100 = \frac{FF\ J_{sc} V_{oc}}{P_{in}} \times 100\ \% \qquad (3\text{-}15)$$

where P_{in} is the input power density, which is equal to the radiation density.

No account has yet been taken of the spectral distribution of the incident radiation, and consideration must obviously be given to this if estimates are to be made for the conversion efficiency of practical cells. The radiation intensity P_{in} in e.q. (3-1) must be replaced by a spectral distribution function $G(\nu)$, and it must be remembered that the absorption coefficient α and the quantum efficiency Q are both functions of photon energy. The rate of generation of electron hole pairs is then [42]

$$R_G = \int_0^{\infty} \frac{G(\nu)\ \alpha(\nu)\ Q(\nu)}{h\nu}\, d\nu \qquad (3\text{-}16)$$

This equation can be used to calculate the theoretical efficiency of cells fabricated from various semiconductor compounds, as shown in Fig. (1-1).

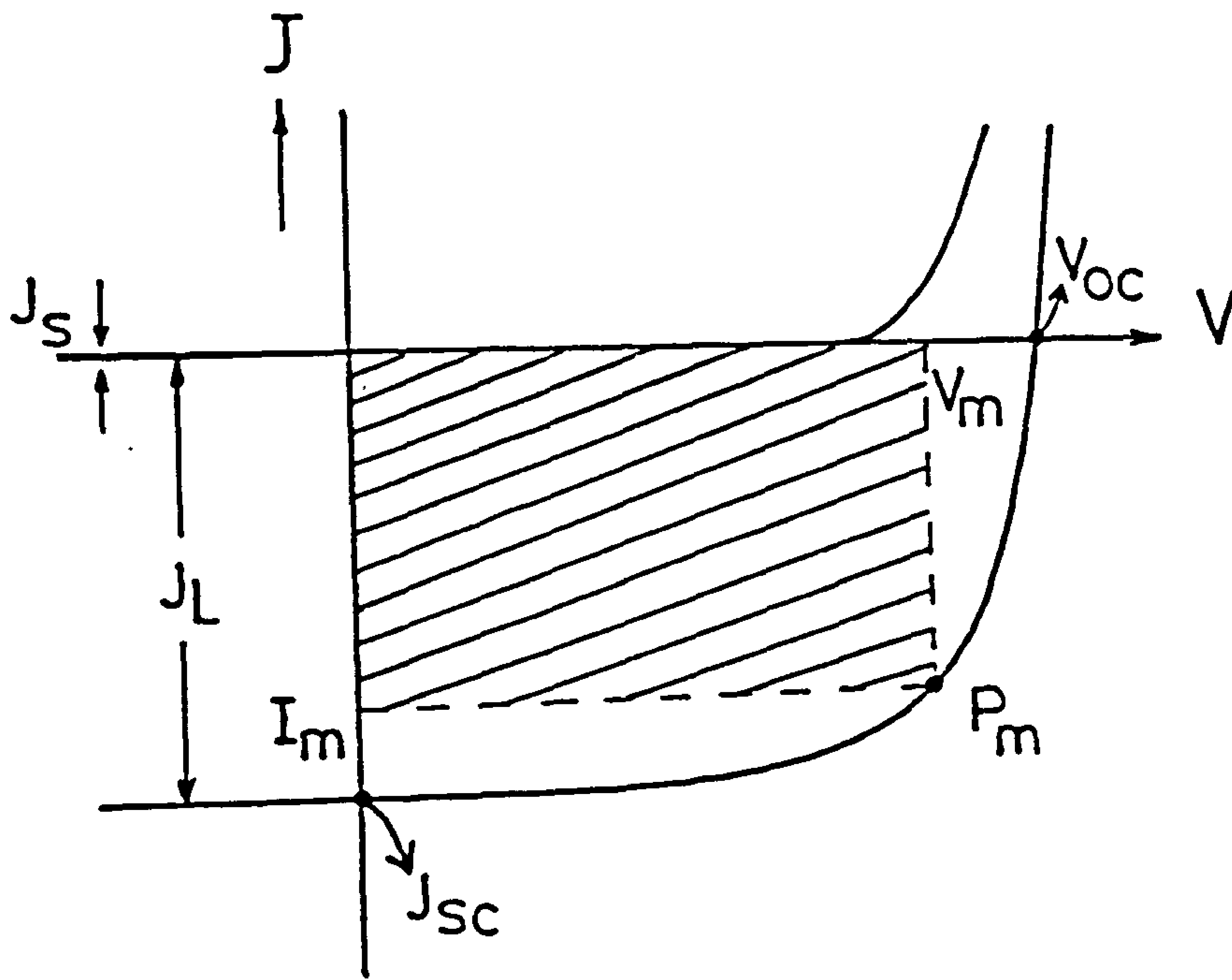


Figure (3-3) Current-Voltage characteristics of an ideal solar cell

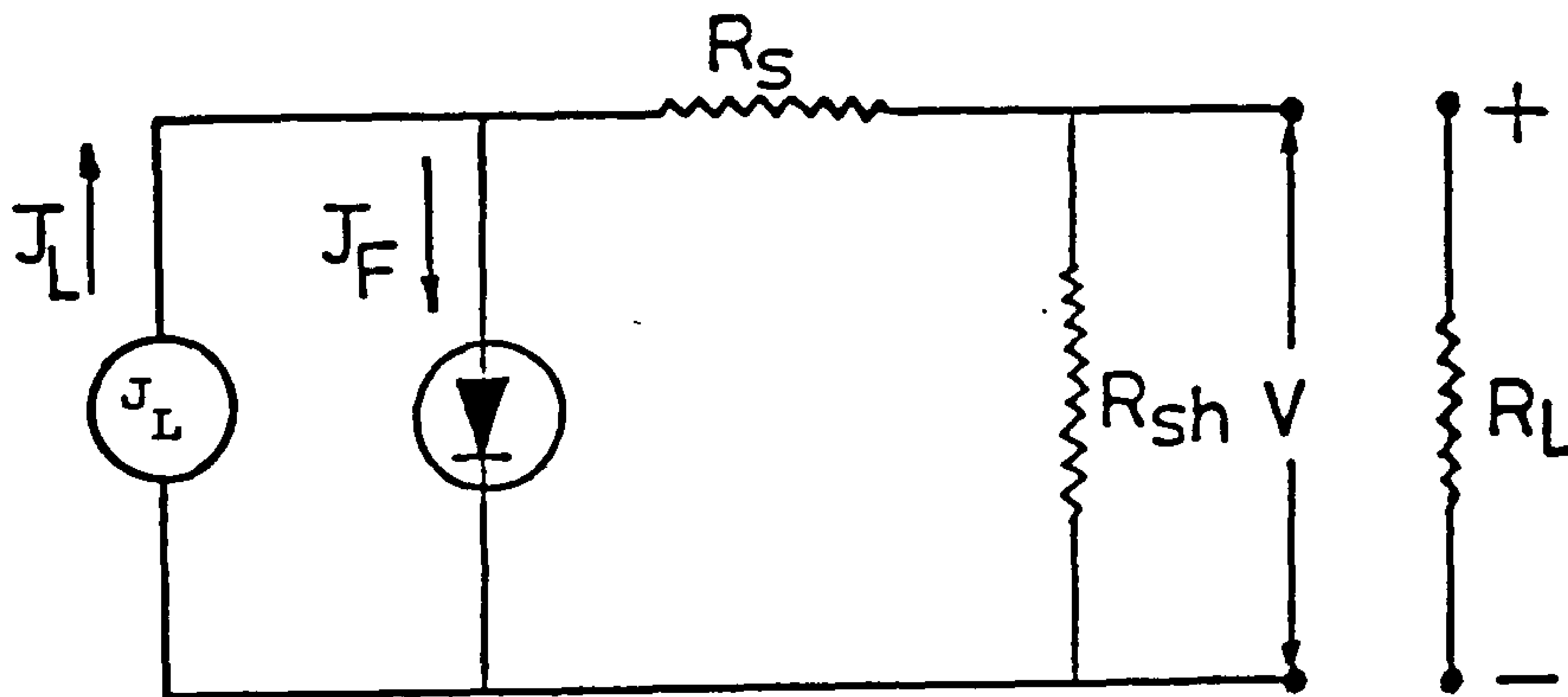


Figure (3-4) Equivalent circuit of a solar cell including series resistance R_s and shunt resistance R_{sh}.

The actual spectral distribution of solar radiation incident on the Earth's surface depends on the location, the time of year and time of day, and on atmospheric conditions.

3.2.2 The Practical Case

For practical solar cells, the charge transport mechanism is considerably more complicated than that for the ideal case described above. In addition to electron and hole diffusion currents, there may be quantum mechanical tunnelling through the barrier and recombination via space charge or interface states. The effect of these processes on the J-V characteristics of a device have been discussed previously [2, 42, 45, 157]. In these circumstances the forward current tends to follow an exponential dependence on the forward voltage expressed by exp (eV/nkT) where n is called the ideality factor, and has a value dependent on the dominant charge transport mechanism in operation. The conversion efficiency usually decreases with increasing values of n for the device.

The equivalent circuit for a practical cell can be represented as in Fig. (3-4) and the J-V relationships must be modified to include the effect of the series resistance R_s and the shunt resistance R_{sh}. Hence the current drawn from a device, under illumination can be expressed as [157]

$$J = \sum_i J_{si} \left| \exp\left(\frac{e\,(V-JR_s)}{n_i\,kT}\right) - 1 \right| + \frac{V - JR_s}{R_{sh}} - J_L \qquad (3\text{-}17)$$

where J_L is the light generated current density (roughly equal to the short circuit current density J_{sc}), J_{si} the saturation current density for the ith current mechanism and n_i is the corresponding diode ideality factor.

For a front-wall cell with the structure shown in Fig. (4-1), the

series resistance R_s has a number of components, one of which is a resistance arising from the bulk of the base material (the collector). This resistance is given by

$$R_{s2} = \rho_2 \; d_2 \; / \; A \qquad (3\text{-}18)$$

where ρ_2 is the resistivity and d_2 is the thickness of the layer, and A is the surface area of the base material. The back contact can introduce an additional resistance, but the major contribution to R_s is due to the sheet resistance of the upper layer (the absorber). This resistance is due to the need to make the absorber as thin as possible in order to ensure that the photogenerated carriers are close to the junction region. The contributing resistance is given by

$$R_{s1} \sim \rho_1 \; / \; d_1 \; m^2 \qquad (3\text{-}19)$$

where m is the number of grid lines, and ρ_1 and d_1 are respectively the resistivity and thickness of the upper layer.

The shunt resistance, R_{sh}, arises because of current leakage paths within the solar cell due to surface leakage along the edges of the cell, and also to diffusion spikes along dislocations, grain boundaries or microcracks. In thin film devices the possibilities for current leakage are greater than in single crystal systems due to the microcrystalline structure of the films, surface damage, and the possible presence of pin-holes in the films.

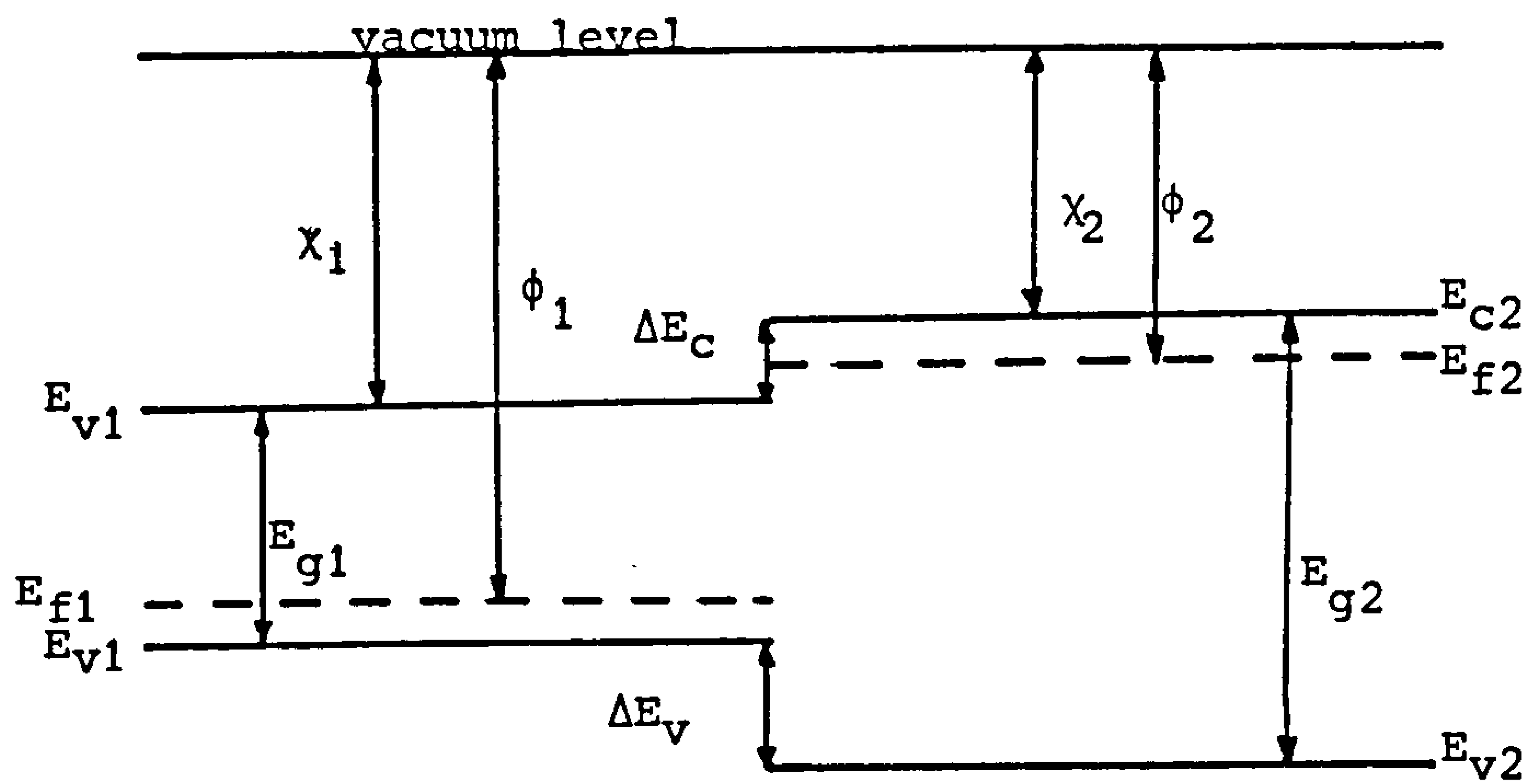
3.3 The p-n Heterojunction

A heterojunction is a junction formed between two dissimilar semiconductors. When the two semiconductors have the same type of conductivity, the junction is called an isotype heterojunction. Alternatively, when the conductivity types are different an anisotype

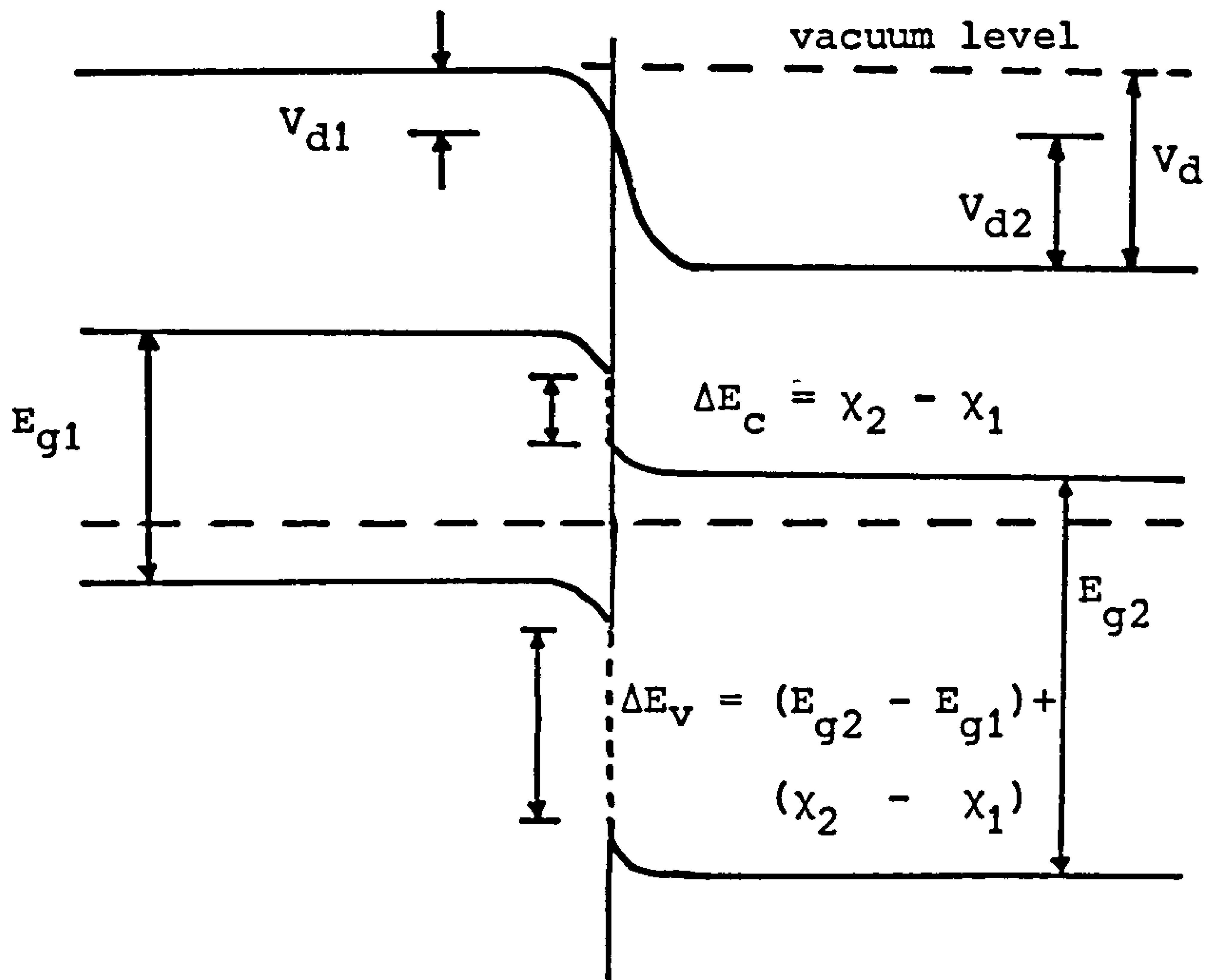
heterojunction is formed. The properties of heterojunctions have been reviewed by Milnes and Feucht (165), Sharma and Purohit (166), Casey and Panish (167), Hill (42) and more recently by Fonash (168), Shaw (169) and Fahrenbruch and Bube (2).

The energy model of an ideal abrupt heterojunction was first proposed by Anderson(170). This model forms the basic starting point for most subsequent heterojunction theories. Fig. (3-5) shows the energy-band diagram of the anisotype heterojunction formed from two different semiconductors having band gaps E_{g1} & E_{g2}, permittivities ϵ_1 & ϵ_2, work function ϕ_1 & ϕ_2 and electron affinities χ_1 & χ_2. When these two semiconductor materials are brought into contact, electrons flow from n-region to p-region, and holes flow from p-region to n-region until equilibrium is established between p- and n-regions. This results in the formation of an uncompensated positive space charge of ionized donors in the n-layer of width W_n, and an uncompensated negative space charge of ionized acceptors in the p-layer of width W_p. As the Fermi level must be uniform throughout the system under conditions of thermal equilibrium and the vacuum level is everywhere parallel to the band edges and is continuous, the discontinuity in conduction-band edges ΔE_c and valence-band edges ΔE_v is invariant with doping provided that Eg and χ are not functions of doping. Figure (3-5b) shows a possible configuration for a solar cell p-n heterojunction, where $E_{g2} > E_{g1}$.

Depending on the relative magnitudes of χ_1 and χ_2, it is clear that ΔE_c may be positive or negative. When $\Delta E_c < o$ the effect is merely to reduce V_d and ultimately to reduce V_{oc}. On the other hand, $\Delta E_c > o$ implies a conduction band spike which tends to impede photogenerated current transport and at the same time may change the dark J-V characteristics considerably. Anderson (170) derived the current voltage characteristics



(a)



(b)

Figure (3-5) Energy band-diagram of Anderson heterojunction (a) before Contact, and (b) after Contact, where $E_{g1} < E_{g2}$, $\Delta E_c > o$ and $\Delta E_v > o$.

of the heterojunction, whicn is shown in Fig. (3-5), and showed that tne forward current density is given by

$$J = e X N_{d2} \left(\frac{D_{n1}}{\tau_{n1}}\right)^{\frac{1}{2}} \exp\left(-\frac{e V_{d2}}{kT}\right) \left[\exp\left(\frac{eV_2}{kT}\right) - \exp\left(-\frac{eV_1}{kT}\right)\right] \qquad (3\text{-}20)$$

where V_1 and V_2 are the parts of the applied voltage ($V = V_1 + V_2$) dropped across the p and n regions of the junction. N_{d2} is the donor concentration in the n-region, D_{n1} and τ_{n1} are the electron diffusion coefficient and lifetime in the p-region and X is the transmission coefficient for the electrons crossing the junction. Although Anderson's simple model satisfactorily accounts for many properties of heterojunctions, it fails to explain the behaviour observed for C-V and J-V characteristics as a function of temperature due to the fact that it ignors the states which invariably occur at the interface and which give rise to recombination and tunnelling current.

The model proposed by Dolega [171] considers the junction as the interface between the two surfaces each having its own distribution of surface states. The trapped cnarges, normally associated with surfaces can recombine because of the overlap of the surface state distributions. Thus fast recombination occurs at the interface of those electrons and holes which reach the recombination centres by thermal emission over their respective barriers.

The forward current density according to Dolega's model has been rewritten by van Opdorp [172] in the form

$$J = B \exp\left(-\frac{eV_d}{kT}\right) \left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \qquad (3\text{-}21)$$

where n is the diode ideality factor. B is a weakly temperature dependent factor. Since this model implies thermal excitation over the barriers, it cannot explain the temperature independence observed in many heterojunctions for the slopes of Ln J vs V curves. Such observations

suggest that the tunnelling processes are more important. For example, where a conduction band spike exists, electrons may tunnel through it from the n-region into the conduction band of the p-region and subsequently recombine either close to the interface or after thermal excitation [173]. Newman [174] found that the tunnelling current in a heterojunction can be written as

$$J = J_{so} \exp\left(\frac{T}{T_o}\right) \exp\left(\frac{V}{V_o}\right) \qquad (3\text{-}22)$$

where J_{so}, T_o, V_o are constants. However, in many practical heterojunctions the current seems to be due to a mixture of tunnelling and recombination processes. Fig. (3-6) shows the various possibilities for current paths across an anisotype heterojunction. In this figure the electron and hole paths e_1 and h_1 represent the diffusion processes as previously discussed for the ideal p-n junction. The second possibility for the electron and hole paths e_2 and h_2 show an emission and recombination situation in which the carriers are thermally excited into opposite ends of interface states with a subsequent recombination. Such a mechanism would be expected to show a temperature dependence. The third possibility of the paths indicated by e_3 and h_3 are tunnelling processes in which either the electrons can tunnel from the conduction band in the n-region of the wide band-gap material into empty interface states and then recombine with holes, or holes can tunnel from the valence band of the narrow band-gap material and then recombine with electrons. If tunnelling originates from the bottom of the conduction band or the top of valence band, then the forward current density is of the form [175]

$$J = B \exp \left| -\alpha_T \, (V_d - V) \right| \qquad (3\text{-}23)$$

where

$$\alpha_T = \frac{4}{3\hbar} \left(\frac{m^* e \, \varepsilon_2}{N_{d2}} \right)^{\frac{1}{2}} \qquad (3\text{-}24)$$

This expression for α_T assumes a single step process of tunnelling and a linear barrier.

More satisfactory agreement with experimental results is obtained (160, 161) if a multi-step tunnelling process is considered. A simple form of the appropriate equation is of the form

$$J = c_f \ \exp(\beta T) \ \exp(\varphi V) \qquad (3\text{-}25)$$

where c_f is constant and the coefficients φ and β are practically independent of the applied voltage and the temperature respectively. The slope of ln J versus V for the above equation is almost temperature independent with the small remaining temperature dependence arising from the variation with temperature of the widths of the band gaps. The weak temperature dependence of the current-voltage characteristics for the tunnelling recombination process, allows this mechanism to be easily distinguished from thermally-assisted processes.

3.4 The Schottky Barrier

According to Schottky's theory of metal-semiconductor junctions, the shape of the potential barrier in the surface region of a semiconductor is determined by a uniform space charge. However, a variety of surface and interface space charge barrier systems are now often referred to as Schottky barriers and contacts which have intentional rectifying properties as Schottky diodes.

In a similar way to that for a p-n junction, a barrier arises at the junction between a metal and semiconductor because of the difference in work functions between the metal and the semiconductor. Mott [176] showed that the diffusion potential should be equal to the difference between the

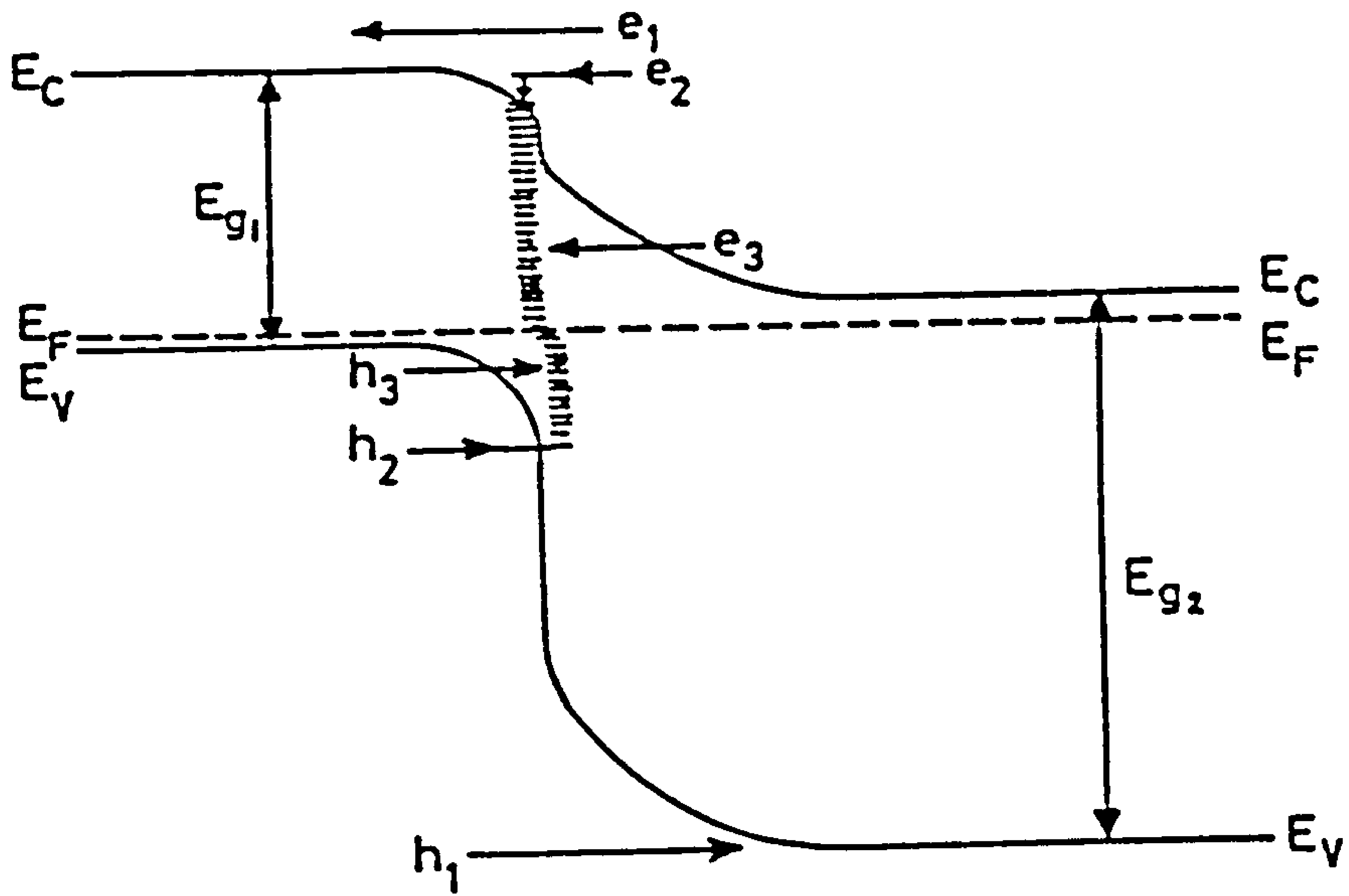


Figure (3-6) Possible interface transport mechanism in p-n heterojunction.

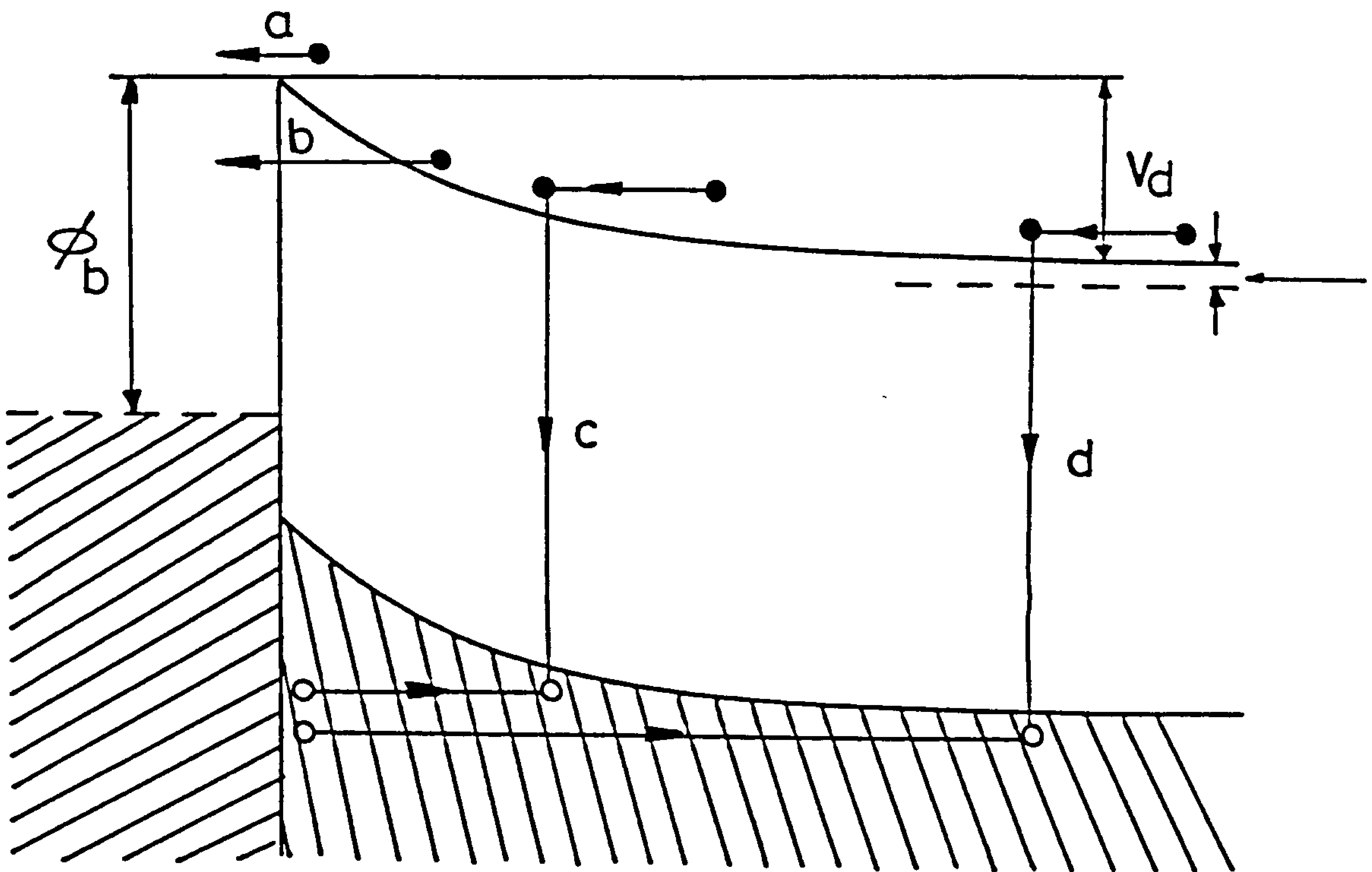


Figure (3-7). Transport processes in a forward-biased Schottky barrier.

work functions of the metal and the semiconductor, and the barrier height should be given by the difference between the metal work function ϕ_b and the electron affinity of the semiconductor χ_s. Bardeen [177] assumed the existence of a thin insulating layer between the metal and the semiconductor and explained that the barrier height is often almost independent of the choice of metal, due to the existence of surface states on the semiconductor.

The current transport in metal-semiconductor contacts is mainly due to the majority carriers, in contrast to p-n junctions, where the minority carrier transport processes are important. Fig. (3-7) shows four basic transport processes under the forward bias (the inverse processes occur under reverse bias) for an n-type semiconductor. These processes are [178] (a) emission of electrons from the semiconductor over the top of the barrier into the metal, (b) quantum-mechanical tunnelling through the barrier, (c) recombination in the space-charge region, and (d) recombination in the neutral region (hole injection).

For many practical cases, process (d) can be neglected, but processes (b) & (c) cause departures from the ideal behaviour (process a) in much the same way as discussed for p-n junctions.

Assuming that mechanism (a) is dominant, the forward bias dark current of a Schottky barrier diode can be written as

$$J = A^* T^2 \exp\left(-\frac{e\,\phi_b}{kT}\right) \left| \exp\left(\frac{eV}{kT}\right) - 1 \right| \qquad (3\text{-}26)$$

where ϕ_b is the Schottky barrier height, while A^* is the modified Richardson constant and it is given by

$$A = 4\,\pi\,e\,m^*\,k^2/h^3 = 120\,\frac{m^*}{m_o} \quad A/cm^2\,K^2 \qquad (3\text{-}27)$$

where m^* is the effective mass of the carriers, m_o is the free electron mass, and h is Planck's constant. However due to effects of tunnelling

and recombination processes, the J-V characteristics for practical devices do not follow exactly the form of eq. (3-26), but can be fitted to an equation of the form

$$J = J_s \left| \exp\left(\frac{eV}{nkT}\right) - 1 \right| \qquad (3\text{-}28)$$

or

$$J \simeq J_s \exp\left(\frac{eV}{nkT}\right) \quad \text{for} \quad eV >> kT$$

where J_s is the reverse saturation current density, and n is known as the ideality factor as in the similar case for p-n junctions. This factor can be obtained from the slope of the ln J versus V curve.

$$n = \frac{e}{kT} \left(\frac{\partial V}{\partial \, \ell n \, J} \right) \qquad (3\text{-}29)$$

Schottky barriers have been studied by many workers and a detailed treatment can be found in various books such as those by Rhoderick [178] and by SZe [164], while Townsend [50] and Hovel [39] have reviewed Schottky barrier solar cells. Ideal Schottky cells have also been discussed by McQuat and Pulfrey.[179] One of the main advantages of Schottky barrier cells is their response to short wavelength light, and high short circuit currents which can be obtained provided that anti-reflective coatings are added to minimise the normally high reflection from the surface of the metal. To form high efficiency Schottky barrier solar cells, it is necessary, as in the case of p-n junction cells, to provide as large a barrier height as possible to reduce J_s and hence increase the open circuit voltage V_{oc}. The non-ideal Schottky barriers with a very thin insulating layer between the metal and the semiconductor (MIS) can produce a junction with a higher open circuit voltage and higher efficiency than that achieved [180-182] with the simpler M-S structure. A general analysis of MIS junctions has been made by Fonash [183, 184] for semiconductors with different oxide layer thickness and different metal work functions.

3.5 The Space Charge Region and Capacitance-Voltage Studies for Solar Cells

It has been seen in the previous sections that the performance of a semiconductor solar cell (whether in the form of a homojunction, a heterojunction or a Schottky barrier) is very sensitive to the nature of the space charge barrier at the interface and particularly to its influence on the carrier transport mechanisms across it. Studies intended to obtain information about the space charge region can thus be very profitable in building an improved understanding of the behaviour of a cell. In particular capacitance measurements can be used to obtain information about the charge distribution, the space charge layer width, the diffusion voltage and the carrier concentration of the semiconductor.

In this section, in order to provide a treatment which would be applicable to a number of different practical situations, a p^+-n junction with a three-region space charge distribution will be considered, following the analysis of Hall and Singh [185]. The three regions (all within the n-type semiconductor) are shown in Fig. (3-8) and include : (a) a high space charge density from $x = o$ to $x = d_1$, (b) from $x = d_1$ to d_2 a lower charge density in a partially compensated layer of the system, and (c) from $x = d_2$ to W a higher space charge density contributed by the more highly conductive bulk of the semiconductor. Clearly W is the total space charge layer width.

The electrostatic potential Ψ is related to the space charge density ρ by Poission's equation which must be solved making use of the following boundary conditions:

$$\frac{d\Psi}{dx} = o \qquad \text{at} \qquad x = W$$

$$\Psi = o \qquad \text{at} \qquad x = o \qquad (3\text{-}30)$$

$$\Psi = V_D + V \quad \text{at} \quad x = W$$

where V_D is the diffusion voltage and V is the applied voltage.

The space-charge density for such a distribution as is shown in Fig. (3-8) can be expressed in the following terms:

$$\rho = e \left[\frac{N_1}{1 + \exp\left[a\,(x-d_1)\right]} + N_2 + N_3 \left(1 - \frac{1}{1 + \exp\left[b\,(x-d_2)\right]}\right)\right] \text{for } 0 \leqslant x \leqslant w$$

$$\rho = 0 \quad \text{for} \quad x > w \qquad (3\text{-}31)$$

where the space charge density at the high space-charge density surface is $e\,(N_1 + N_2)$, the space-charge density in the compensated layer is eN_2, and the space charge density for the bulk is $e(N_2 + N_3)$. The parameters a and b are required to describe the spatial variations of charge within the transition layers between one space-charge region and the next. The Poisson equation may be written in one-dimensional form as

$$\frac{d_2\Psi}{dx^2} = -\frac{e}{\varepsilon}\left[\frac{N_1}{1 + \exp\left[a\,(x-d_1)\right]} + N_2 + N_3\left(1 - \frac{1}{1 + \exp\left[b\,(x-d_2)\right]}\right)\right] \qquad (3\text{-}32)$$

and this can be integrated to yield Ψ as a function of xby making use of appropriate boundary conditions including those expressed in equations (3-30) together with the requirement that no discontinuities in Ψ should exist at the boundary between the three regions. Then for the case where $a = b = \infty$ the expression for the potential Ψ in each of the three regions are:

$$\Psi_{x \leqslant d_1} = -\left(\frac{e}{\varepsilon}\right)\left[(N_1 + N_2)\tfrac{1}{2}x^2 - (N_2 + N_3)\,wx - (N_1 d_1 - N_3 d_2)\,x\right] \qquad (3\text{-}33)$$

$$\Psi_{d_1 \leqslant x \leqslant d_2} = -\left(\frac{e}{\varepsilon}\right)\left[N_2\tfrac{1}{2}x^2 - N_1\tfrac{1}{2}d_1^2 - (N_2 + N_3)\,wx + N_3 d_2\,x\right] \qquad (3\text{-}34)$$

$$\Psi_{x \geq d_2} = -\left(\frac{e}{\varepsilon}\right)\left[(N_2 + N_3)\tfrac{1}{2}x^2 - (N_2 + N_3)\,wx + \tfrac{1}{2}N_2 d_1^2 - \tfrac{1}{2}N_1 d_1^2\right] \qquad (3\text{-}35)$$

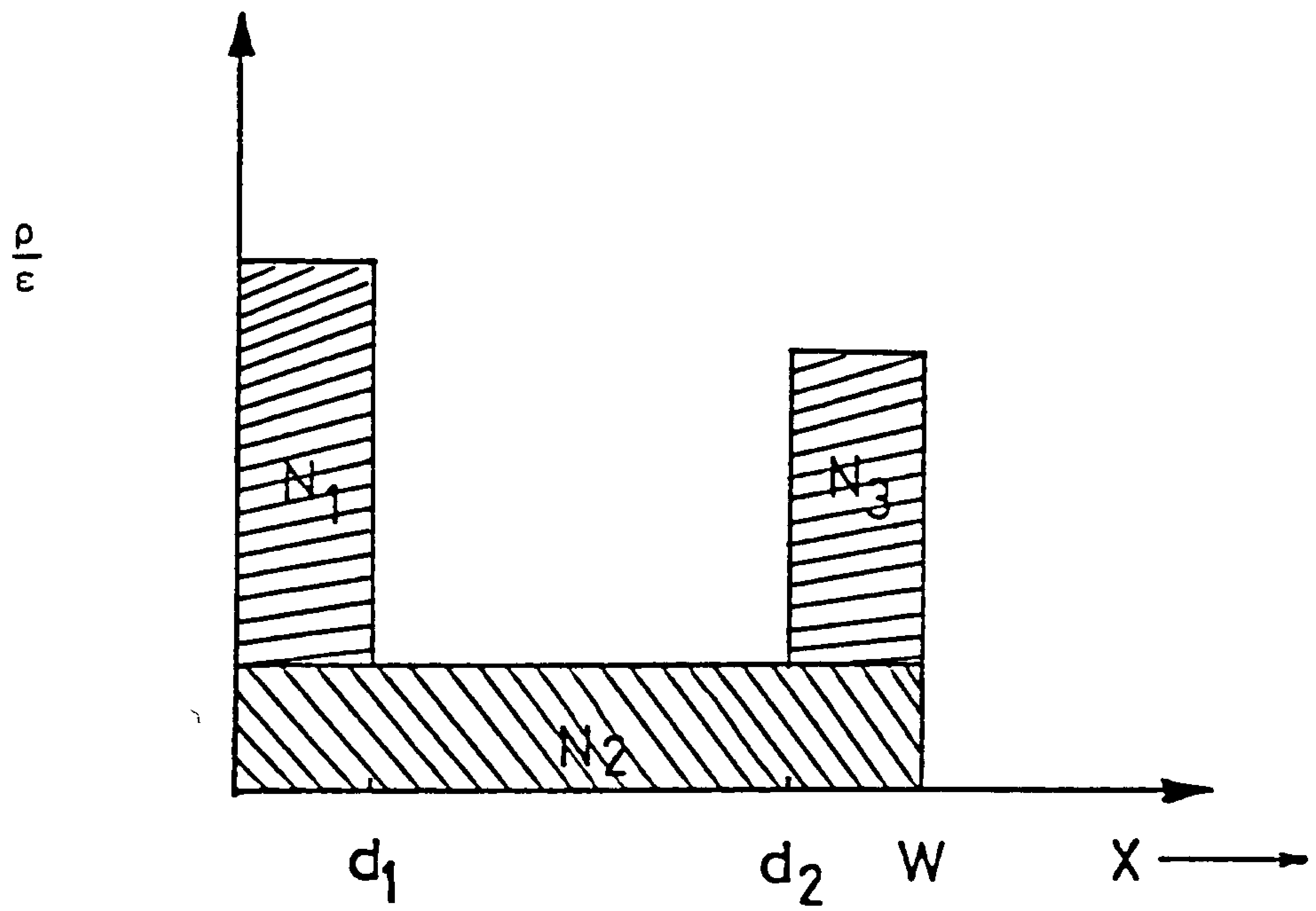


Figure (3-8) One-dimensional spatial variation of space-charge density from the heterojunction interface at x = 0.

It follows from eq. (3-35) and (3-30) that the space-charge width W can be written as

$$W = \left(\frac{2\,\varepsilon (V + V_D)}{e\,(N_2 + N_3)} + \frac{N_3\, d_2^2}{N_2 + N_3} - \frac{N_1\, d_1^2}{N_2 + N_3} \right)^{\frac{1}{2}} \tag{3-36}$$

The junction capacitance C is related to the charge Q by:

$$C = \frac{dQ}{dV} \tag{3-37}$$

where $Q = A\,e\,\left[N_1\, d_1 + N_2\, W + N_3\,(W - d_2)\right]$

$$= A\,e\,\left[N_1\, d_1 - N_3\, d_2 + (N_2 + N_3)\, W\right] \tag{3-38}$$

and where A is the area of the junction.

If we assume that d_1, d_2, N_1, N_2 and N_3 are not functions of voltage V, then

$$\frac{dQ}{dV} = A\,e\,(N_2 + N_3)\,\frac{dW}{dV} \tag{3-39}$$

Using e.q. (3-36) and (3-39), it is seen that the capacitance-voltage relationship can be written as:

$$\left(\frac{1}{C}\right)^2 = \left(\frac{2}{A^2\,\varepsilon\, e\,(N_2 + N_3)}\right) V + \left(\frac{2}{A^2\,\varepsilon\, e\,(N_2 + N_3)}\right) \left[V_D + \frac{e}{2\varepsilon}\,(N_3\, d_2^2 - N_1\, d_1^2)\right] \tag{3-40}$$

and from e.q. (3-36) and (3-40) we have

$$C = \frac{\varepsilon A}{W} \tag{3-41}$$

as in the case of a simple single region space charge barrier.

Three special cases of particular relevance to the CdS-Cu_2S system can be considered.

Case I. When $N_1 = N_3 = o$, then eqs. (3-36) and (3-40) can be written as follows:

$$W = \left(\frac{2\,\varepsilon\,(V + V_D)}{e\, N_2}\right)^{\frac{1}{2}} \tag{3-42}$$

$$\left(\frac{1}{C}\right)^2 = \left(\frac{2}{A^2\,\varepsilon\, e\, N_2}\right)(V + V_D) \tag{3-43}$$

This situation applies to the simplest form of p^+-n junction or the ideal

metal-semiconductor device (Schottky barrier). According to eq. (3-43), a graph of C^{-2} against the reverse bias voltage V allows N_2 to be determined from the slope and the diffusion voltage V_D to be obtained from the intercept on the voltage axis.

Case II. When we have a conductive interface layer for which $N_1 > N_2$ and $N_3 = o$, the eq. (3-36) and (3-40) become

$$W = \left(\frac{2 \varepsilon (V + V_D)}{e N_2} - \frac{N_1}{N_2} d_1^2 \right)^{\frac{1}{2}} \qquad (3\text{-}44)$$

and

$$\left(\frac{1}{C}\right)^2 = \left(\frac{2}{A^2 \varepsilon e N_2}\right) V + \left(\frac{2}{A^2 \varepsilon e N_2}\right) \left(V_D - \frac{e}{2\varepsilon} N_1 d_1^2\right) \qquad (3\text{-}45)$$

In this case, the extrapolated interface with voltage axis for plot of C^{-2} - vs - V is no longer equal to the diffusion voltage V_d, but rather $V_D - (\frac{e}{\varepsilon}) N_1 d_1^2$, while the slope of the plot still determines N_2 (the bulk ionized impurity concentration). As the thickness of the conducting surface layer is increased, the space-charge layer thickness decreases and an effective barrier-reduction effect can occur as a result of electron tunnelling.

Case III. The third case of interest is related to a situation in which an insulating region lies close to the interface, possibly as a result of impurity compensation. In this case $N_3 > N_2$, $N_1 = o$ and e.q. (3-36) and (3-40) can be written as:

$$W = \left(\frac{2 \varepsilon (V + V_D)}{e (N_2 + N_3)} + \frac{N_3 d_2^2}{N_2 + N_3}\right)^{\frac{1}{2}} \qquad (3\text{-}46)$$

and

$$\left(\frac{1}{C}\right)^2 = \frac{2}{A^2 \varepsilon e (N_2 + N_3)} V + \frac{2}{A^2 \varepsilon e (N_2 + N_3)} \left(V_D + \frac{e}{2\varepsilon} N_1 d_1^2\right) \qquad (3\text{-}47)$$

Once again the slope of the plot of C^{-2} against V allows the bulk semiconductor electron concentration $(N_2 + N_3)$ to be determined while the

voltage-axis intercept now occurs at

$$V_D^* = V_D + \left(\frac{e}{2\varepsilon}\right) N_3 \; d_2^2 \tag{3-48}$$

For many practical situations, N_3 and d_2 are such that the second term is dominant and then

$$V_D^* \approx \frac{e}{2\varepsilon} \; N_3 \; d_2^2 \tag{3-49}$$

Accordingly, from this result, the width of the insulating region d_2 can be obtained.

It is important to note that the C-V measurements should be carried out at large operating frequencies, when slow trapping states play only a neglible role in determining the charge densities. Capacitance values measured at high frequencies (~ 1 MHz) are determined by fast, shallow states rather than the deep-level traps [186].

With regard to the use of the above analysis in studies of CdS - Cu_2S solar cell junctions it is expected that one of the above three cases will be applicable at different stages of cell fabrication. When the cell is first formed, a junction defined by case I or case II is anticipated, depending upon the fabrication conditions, but as a result of subsequent heat-treatment during which copper diffuses from the Cu_2S into the CdS, an insulating region is generated on the CdS side of the junction leading to the situation described by case III. According to the analysis above, the resultant barrier properties are very sensitive to the width of the induced insulating layer which is, of course, dependent on the temperature and the time of the diffusion process.

3.6 Diffusion Processes in Thin Film

As we shall see in chapter 5 in this thesis , the diffusion of copper from the Cu_2S layer to the CdS is a very important step in CdS-Cu_2S solar cell fabrication processes. The diffusion of copper results in an increase in magnitude of the space charge barrier on the CdS side of the junction, but it could also have a deleterious effect on the long term operational stability of the cells.

The diffusion of impurities in thin films can take place in the grains and in the grain boundaries. There is no doubt that the resultant diffusion profile in such a film is very complicated and some gross assumptions have to be made in order to estimate the respective diffusion coefficients (D_g in the grain and D_{gb} in the grain boundary) from the observed profiles.

In applying simple diffusion theory the following assumptions are made, (a) one species of impurity will diffuse independently of any other, (b) the diffusion rate is independent of the concentration, and (c) the amount of material diffusing per unit time is proportional to the concentration gradient. For the simple one-dimensional case with propagation in the y direction, Fick's [187] equation can be written as

$$\frac{\partial C(y,t)}{\partial t} = D \frac{\partial^2 C(y,t)}{\partial y^2} \qquad (3\text{-}50)$$

where C is the impurity concentration, and D is the diffusion coefficient According to Fick's law, for impurity diffusion from a limited supply at the surface (y = o), the concentration at a depth y should be given by (188, 189)

$$C(y,t) = C_o \exp\left(-\frac{y^2}{4Dt}\right) \qquad (3\text{-}51)$$

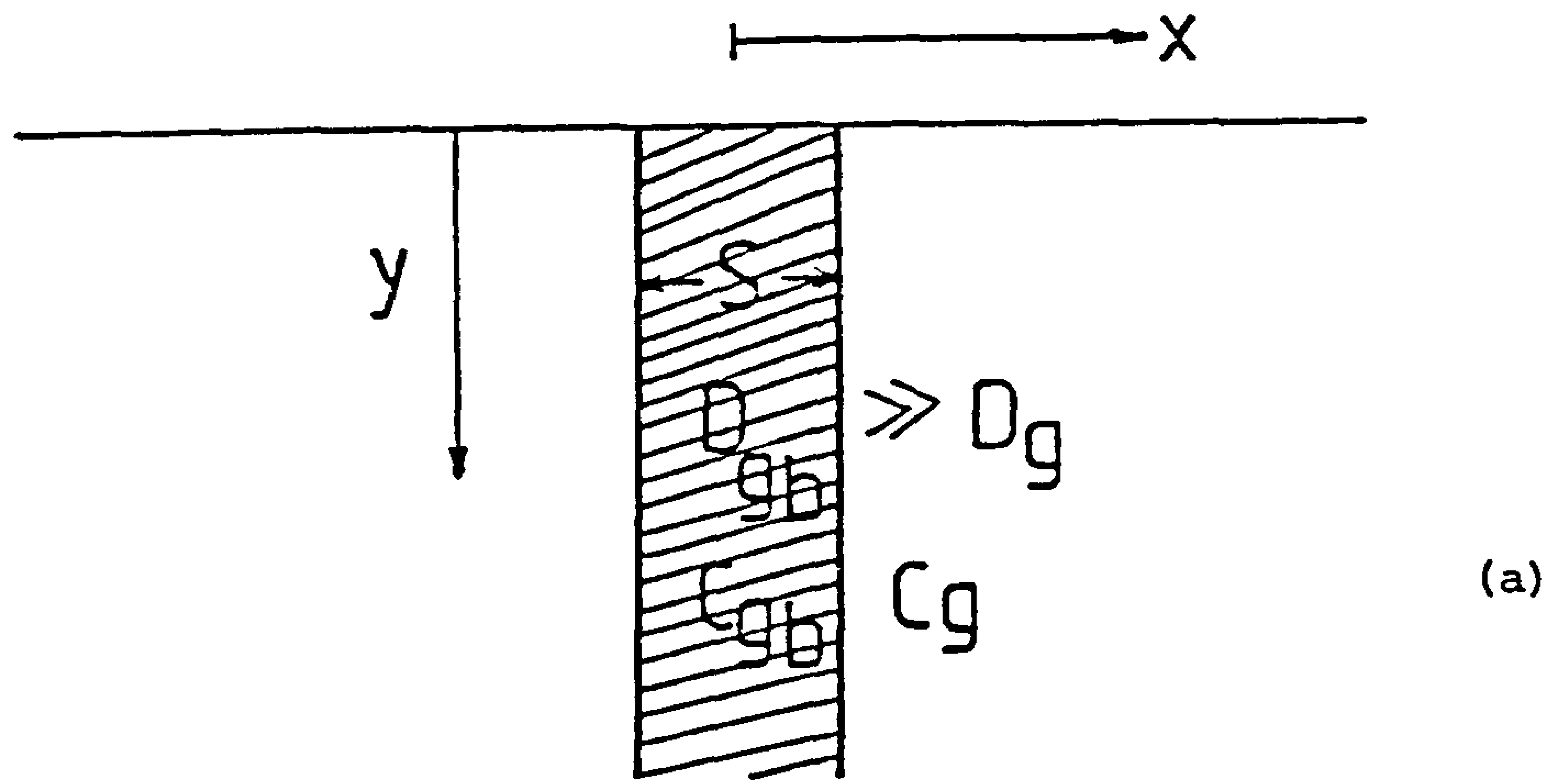
where C_o is dependent on the initial surface concentration of the impurities, and on the time of diffusion t.

In this work, the CdS thin film is in the form of a polycrystalline layer with columnar grains and grain boundaries perpendicular to the substrate. During the heat-treatment process or during cell operation, one could expect that the diffusion of copper from the Cu_2S to the CdS would take place both in the grains and between the grains of the film. For bulk diffusion into the grains, equation (3-51) becomes:

$$C_g (y, t) = C_o \exp (- \frac{y^2}{4 D_g t}) \qquad (3\text{-}52)$$

where D_g is the diffusion coefficient in the grain. In the absence of any other diffusion mechanism, D_g could be obtained from a plot of ln Cg against y^2. However, in addition to the grain diffusion, there will be a further process associated with the grain boundaries. The grain boundary diffusion problem has been mathematically analysed [190, 191] using an idealised model in which grain boundaries lie normal to the free surface of an other wise homogeneous section of material and that each grain boundary is an isotropic slab of material of width S in which the diffusion is characterised by the coefficient D_{gb}. With this model (illustrated in Fig. 3-9a) and with $D_{gb} >> D_g$ the grain boundary constant concentration contours are expected to follow the form shown in Fig. (3-9b). Using this model, a polycrystalline film could be considered to be formed from a random array of slabs of width S lying normal to the free surface of the thin film with each slab sandwiched between two flat grains. Assuming the boundary conditions $C_g = C_{gb}$ and $D_g \frac{\partial C_g}{\partial x} = D_{gb} \frac{\partial C_{gb}}{\partial x}$ at the grain-grain boundaries interface, where C_g is the concentration in the grain (outside the slab) and C_{gb} is the concentration in the grain boundary (within the slab), Le Claire [192] has shown that

$$D_{gb} S = \left(\frac{\partial \operatorname{Log} C_{gb}}{\partial y^{6/5}} \right)^{-5/3} \left(\frac{4 D_g}{t} \right)^{1/2} \left(\frac{\partial \operatorname{Log} C_{gb}}{\partial (\eta \beta^{-\frac{1}{2}})^{6/5}} \right) \qquad (3\text{-}53)$$



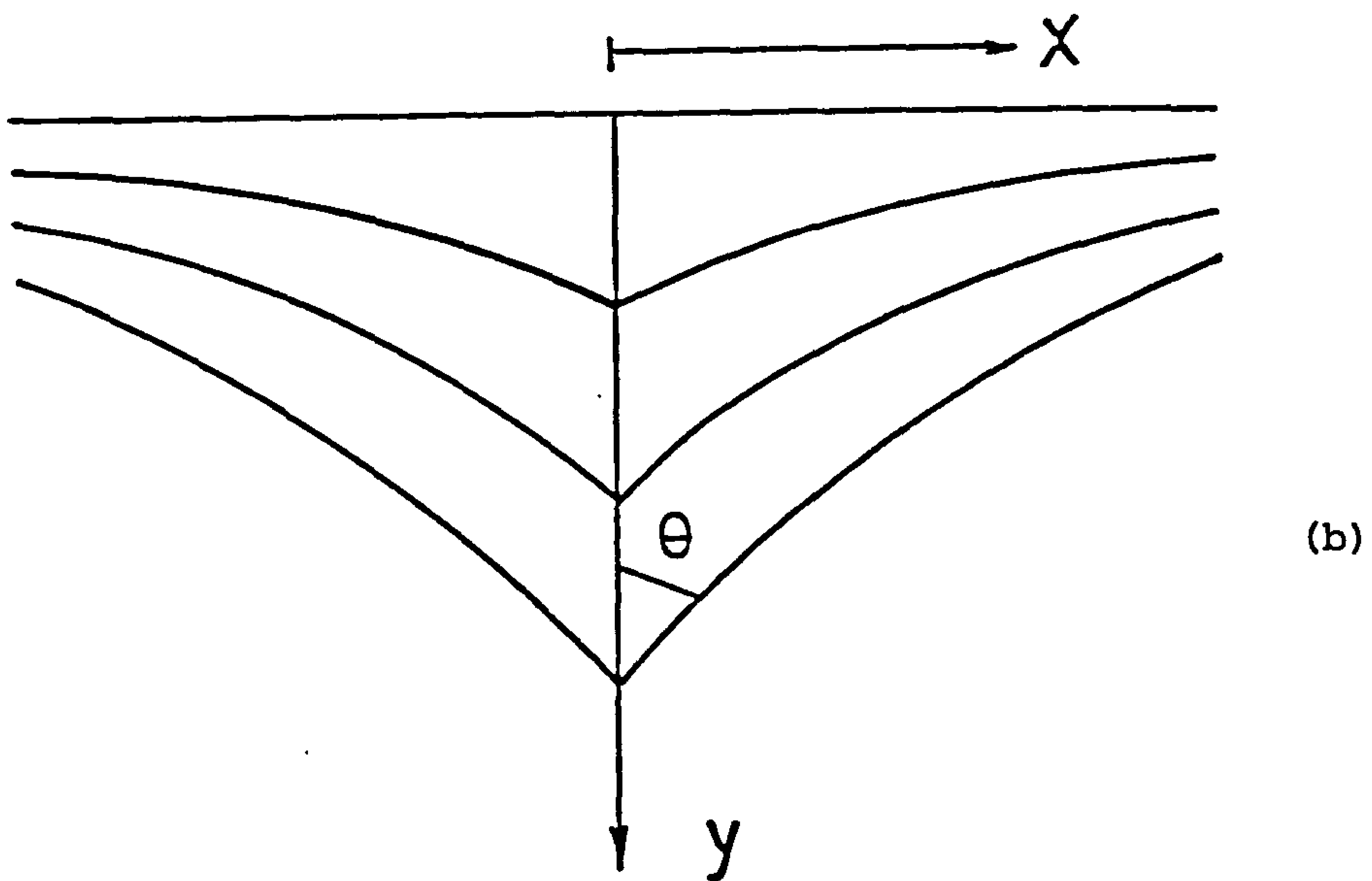


Figure (3-9) The typical grain boundary concentration contours and the model for the grain boundary diffusion in sectioning experiment.

where η and β are dimensionless parameters introduced by Whipple [193]. Numerical evaluation of the last term has provided a value of 0.78 [192, 194], practically independent of concentration, position and temperature. Thus, provided that s, t and D_g are known, D_{gb} can be found by determining the slope of a graph of log C_{gb} against $y^{6/5}$.

Chapter 4

Experimental Procedures

4.1 Introduction

Figure (4-1) shows the cross-sectional structure of a typical cell. The fabrication of such a cell can be divided into five main stages: Preparation of the substrate, deposition of the cadmium sulphide, formation of the copper sulphide, cell annealing, production of the front contact and encapsulation.

Each of these stages of fabrication has an important influence on the properties of the completed cells and therefore it was necessary to control very carefully the fabrication procedures in order to obtain reproducible results.

The experimental details concerning each of the process steps are given in the following sections together with information on the characterization procedures used at different stages of cell fabrication and for determining the behaviour of the completed cells.

4.2 Preparation of the Substrate

A wide variety of substrates was used, including zinc-coated copper, Molybdenum (Mo), zinc coated Mo, Pb, Sn, Zn and various metallic thin films evaporated on glass sheets. The most successful results were obtained with zinc coated copper which makes a good low resistance ohmic contact and provides good adhesion with the CdS thin film. A brief fabrication procedure is as follows:

4.2.(a) Copper Substrate Copper sheets of the required size (5 cm x 4.5 cm) were washed in tap water and detergent to remove any contamination on

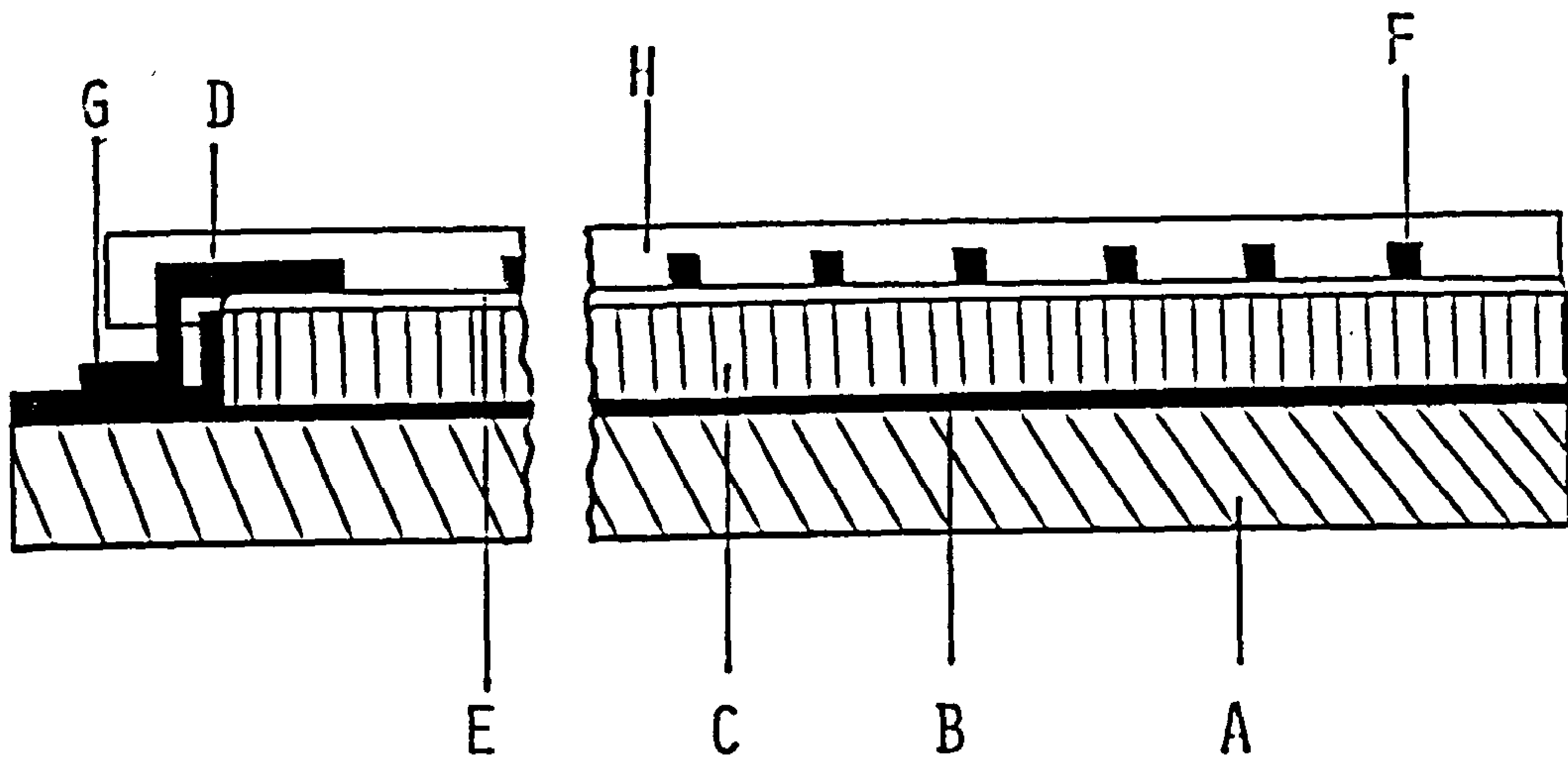


Figure (4-1) Diagramatic cross-section of $CdS-Cu_2S$ Solar Cell .

A	Substrate	B	Thin coating layer
C	CdS	D	Non-Conducting epoxy
E	Cu_2S	F	Metallic grid
G	Grid tap	H	Clear encapsulant

the surface. They were etched in nitric acid (30%) until all the top surface was removed. The sheet was rinsed thoroughly in distilled water and in methanol and finally it was dried in a nitrogen stream.

4.2.(b) Molybdenum Substrate The sheets of Mo were cut to the required size (5 cm x 4.5 cm) and detergent was used for initial cleaning, as in the case of copper. These sheets were then dipped for 10-20 seconds into a beaker containing 50/50 fuming nitric acid and distilled water until the surface had been oxidized to a dark brown colour. This brown oxide layer was removed by soaking the sheets in concentrated hydrochloric acid for about 20-30 seconds, leaving the surface clean and bright. Finally the Mo sheet was rinsed well in distilled water and dried in a nitrogen stream.

4.2.(c) Glass Substrate Sheets of glass of the required size (1.2 cm x 1.2 cm) were used. The thickness of the glass sheet was ~0.1 cm. The glass sheets were kept in a beaker containing 5% concentrated lipsol liquid for a few days. Everything was then heated to about 70°C for 1 hour, before rinsing in hot water and transferring the glass sheets to a beaker containing 2% concentrated lipsol liquid and placing them in an ultrasonic cleaner for 5 minutes. The required number of glass sheets were rinsed thoroughly in warm distilled water until all the lipsol liquid was removed and finally the glass sheets were rinsed in methanol and dried in a nitrogen stream.

4.2.(d) Coating the Substrate The vacuum evaporation technique was used to make a thin coating layer on both metallic and glass substrates. A 12" vacuum coating unit was used. Molybdenum and tungsten boats were

degassed in a vacuum before the metal deposition took place and high purity metals were evaporated using a suitable boat. The substrate was placed about 14 cm vertically above the boat. The thickness was measured using a film thickness monitor. For zinc layers the thickness was determined by a simple method of measuring the weight of the substrate before and after deposition. From the weight difference, density of Zn, and the area of Zn deposited on the substrate the thickness can easily be calculated.

For glass substrates, a thin film of chromium was evaporated first, in order to provide a good adhesion between the glass, and the required metal layer was deposited immediately afterwards without breaking the vacuum.

4.3 Deposition of the Cadmium Sulphide Layer

When CdS powder is heated in a vacuum, it decomposes and the constituent elements travel until they reach a cooler surface or substrate where they recombine to grow in the form of a polycrystalline CdS film. The Wurtzite hexagonal phase always predominates in CdS evaporated films at substrate temperatures greater than 150°C [42,49,65]. If there is a preferred growth direction in the crystallites then, as the growth continues, those crystallites which initially were oriented with their growth direction nearly perpendicular to the substrate begin to predominate. Thus thicker films are covered by highly oriented grains. Apparently the growth rate of the CdS crystallites is substantially greater in the + c direction than in others. However, the orientation of the hexagonal (0001) plane is not perfect and it often assumes a range of angles with respect to the substrate. By arranging the substrate at a suitably large distance from the source the crystallites can almost be

aligned with (0001) direction perpendicular to the substrate. Further, by increasing the thickness of the CdS film, the degree of preferred orientation can be increased. This type of oriented growth yields the columnar structure as shown in Fig. (4-2). The substrate surface texture and temperature , and the evaporation rate, determine the number of nucleations and statistical distribution of their orientation, and hence the grain size of the final CdS film [43].

The process of the evaporation has generally four main steps [195]. The first step is the dissociation of the bulk CdS to cadmium and sulphur on the surface

$$CdS\ (solid) \rightleftharpoons Cd_{(surface)} + S_{\ (surface)} \qquad (4\text{-}1)$$

The loosely bound cadmium atoms on the surface can evaporate directly.

$$Cd_{\ (surface)} \rightleftharpoons Cd_{\ (gas)} \qquad (4\text{-}2)$$

but a single sulphur atom is more likely to associate with another one before the evaporation

$$2\ S_{\ (surface)} \rightleftharpoons S_2\ (surface) \qquad (4\text{-}3)$$

and then the sulphur on the surface can evaporate directly

$$S_2\ (surface) \rightleftharpoons S_2\ (gas) \qquad (4\text{-}4)$$

The cadmium and sulphur vapours recombine on the heated substrate. Since the sulphur vapour pressure is slightly higher than cadmium vapour pressure, the deposits will have an excess of Cd. The lower the substrate temperature the greater the amount of excess cadmium in the film and hence the lower the resistivity. If the temperature of the substrate is very high, cadmium atoms may re-evaporate before recombining with sulphur, thus the stoichiometry of the CdS thin film depends not only on the stoichiometry of the CdS materials in the crucible but also on the substrate temperature and the evaporation rate [42, 65].

The system used for CdS film deposition during this project is shown

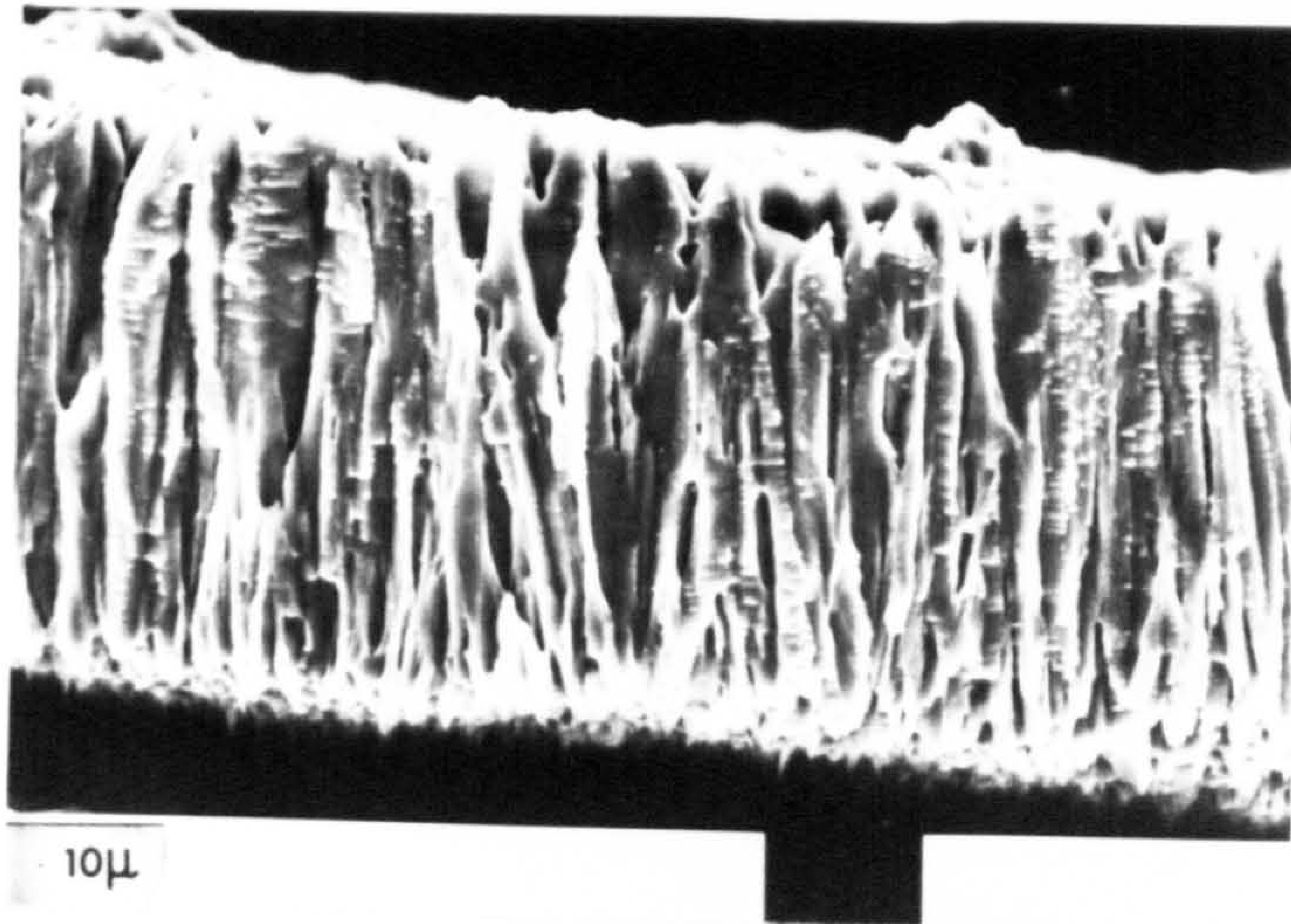


Figure (4-2) SEM micrograph of an acid etched CdS film showing the columnar structure of CdS grains.

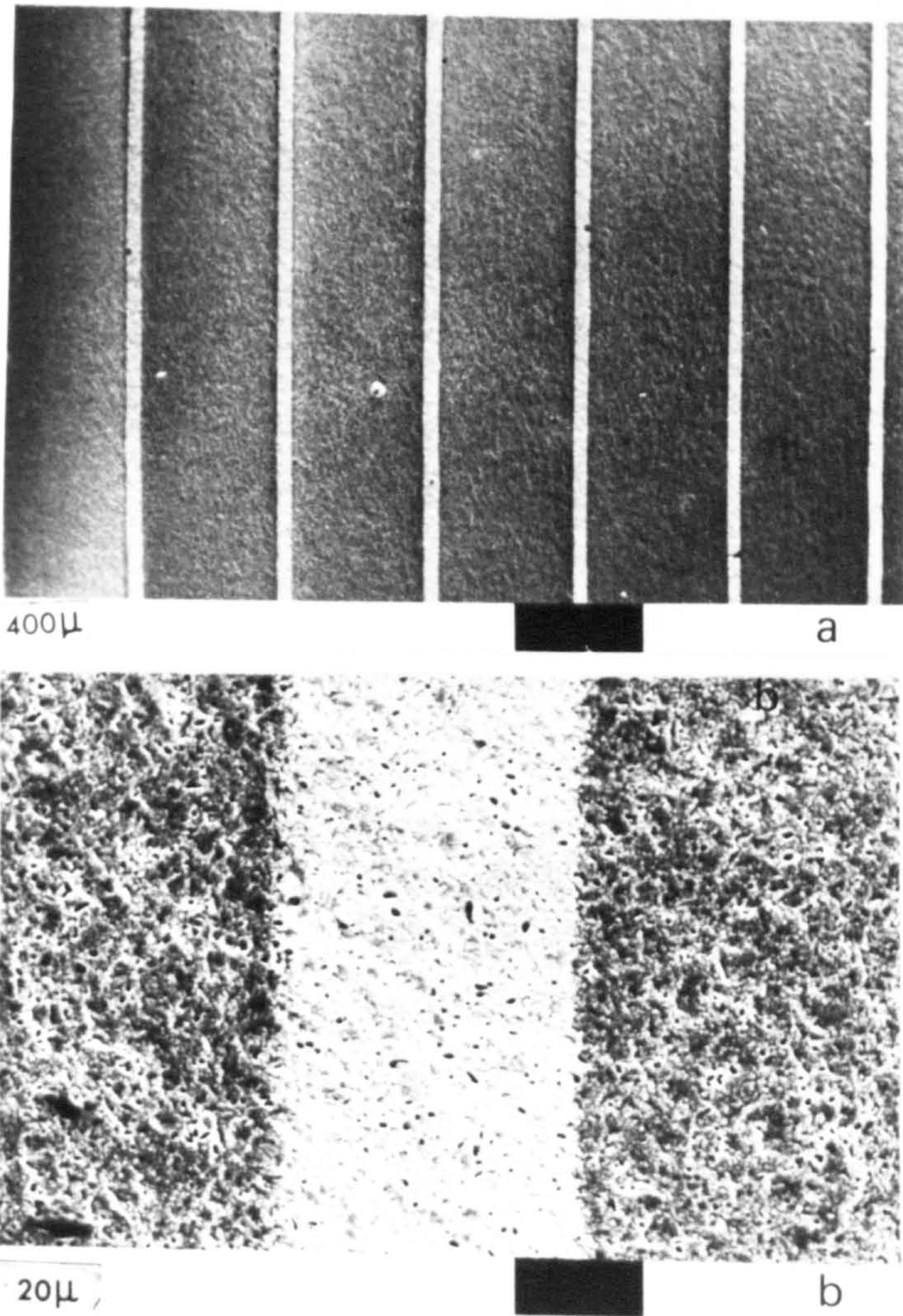


Figure (4-3) SEM micrograph of evaporated gold grids for, (a) number of grids and (b) magnified view of one grid.

schematically in Fig. (4-4) and consists of an evaporation system capable of attaining vacuum better than 10^{-5} torr. The substrate holder consisted of a hollow stainless steel block containing a heater element insulated from it by two thin sheets of mica. Power was supplied from a transformer rated at 15 V, 60 A. The substrate was placed between the heater block and a mask, which was designed to allow a simultaneous fabrication of 18 (1 cm x 1 cm) cells arranged in a 3 x 6 matrix. An extra 1 cm square hole had been cut to clamp a chromel-alumel thermocouple to monitor the substrate temperature. The thermocouple was spot-welded on a metal foil which was placed in contact with the substrate between the substrate heating block and the mask. The substrate holder including the substrate, the mask, and the thermocouple were then suspended above the quartz crucible by the use of two threaded rods, so that its height could be varied.

The CdS charge was contained in a double-walled cylindrical quartz crucible which was heated by means of a molybdenum heating element wrapped around a quartz former as shown in Fig. (4-5). The outer shield was a cylinder of stainless steel covered with a quartz tube. It is difficult to heat the CdS to its sublimation temperature without particles being projected directly onto the substrate. This splattering can be avoided by putting a quartz wool plug on the top of the CdS. Power was supplied from a transformer rated at 15 V, 60 A. A platinum-platinum/rhodium thermocouple could be placed within the quartz crucible to monitor the temperature of the CdS during the evaporation.

The hot-wall consisted of a pyrex cylinder with a heating element wrapped around it. The length and the diameter of this pyrex cylinder were 22.5 cm and 14.0 cm respectively. Power was supplied from a transformer rated at 35 V, 10 A.

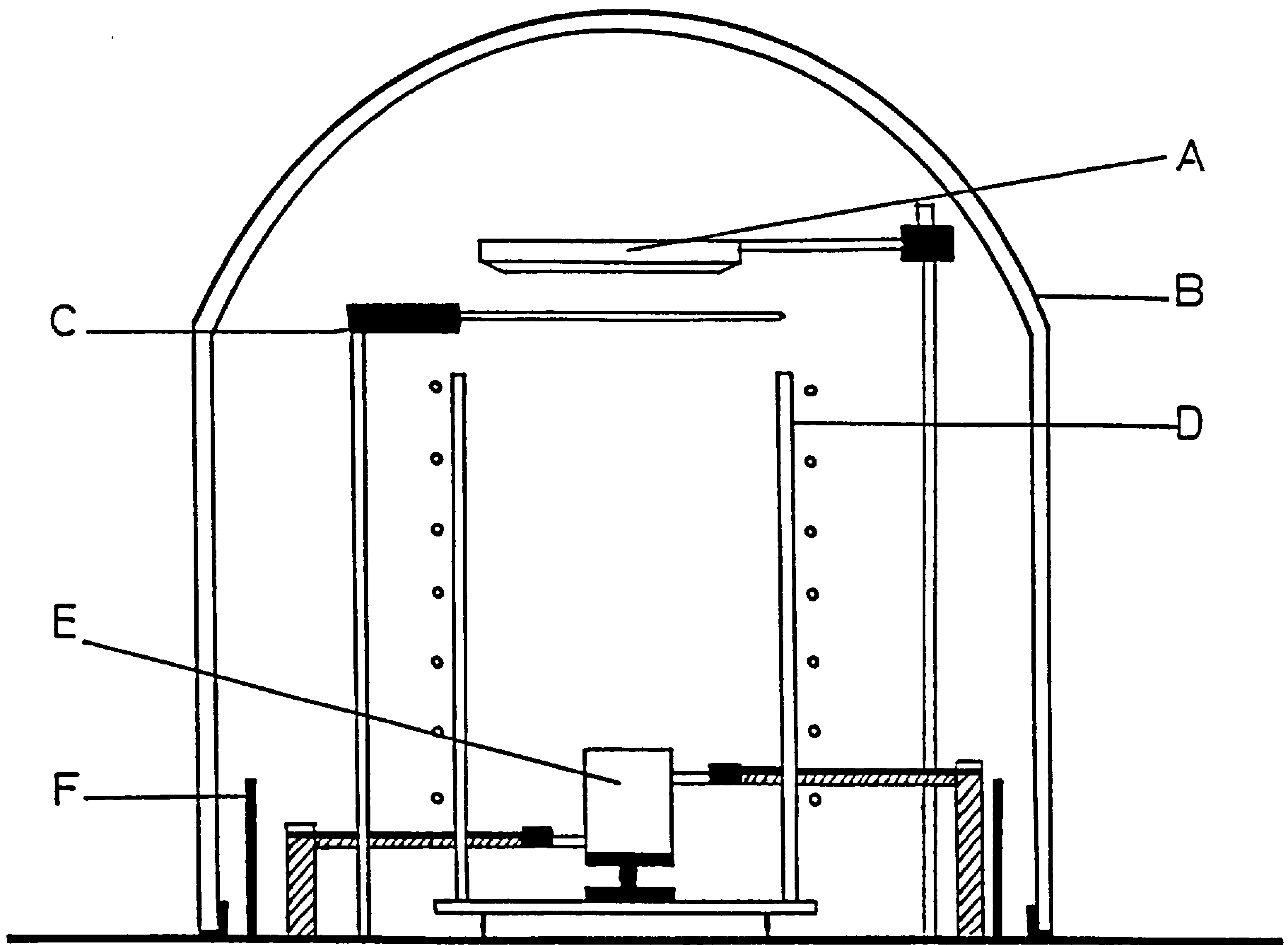


Figure (4-4) Apparatus for the deposition of CdS.

A	Substrate heater	B	Bell jar
C	Shutter	D	Hot-wall
E	Source container and heater	F	Aluminium foil

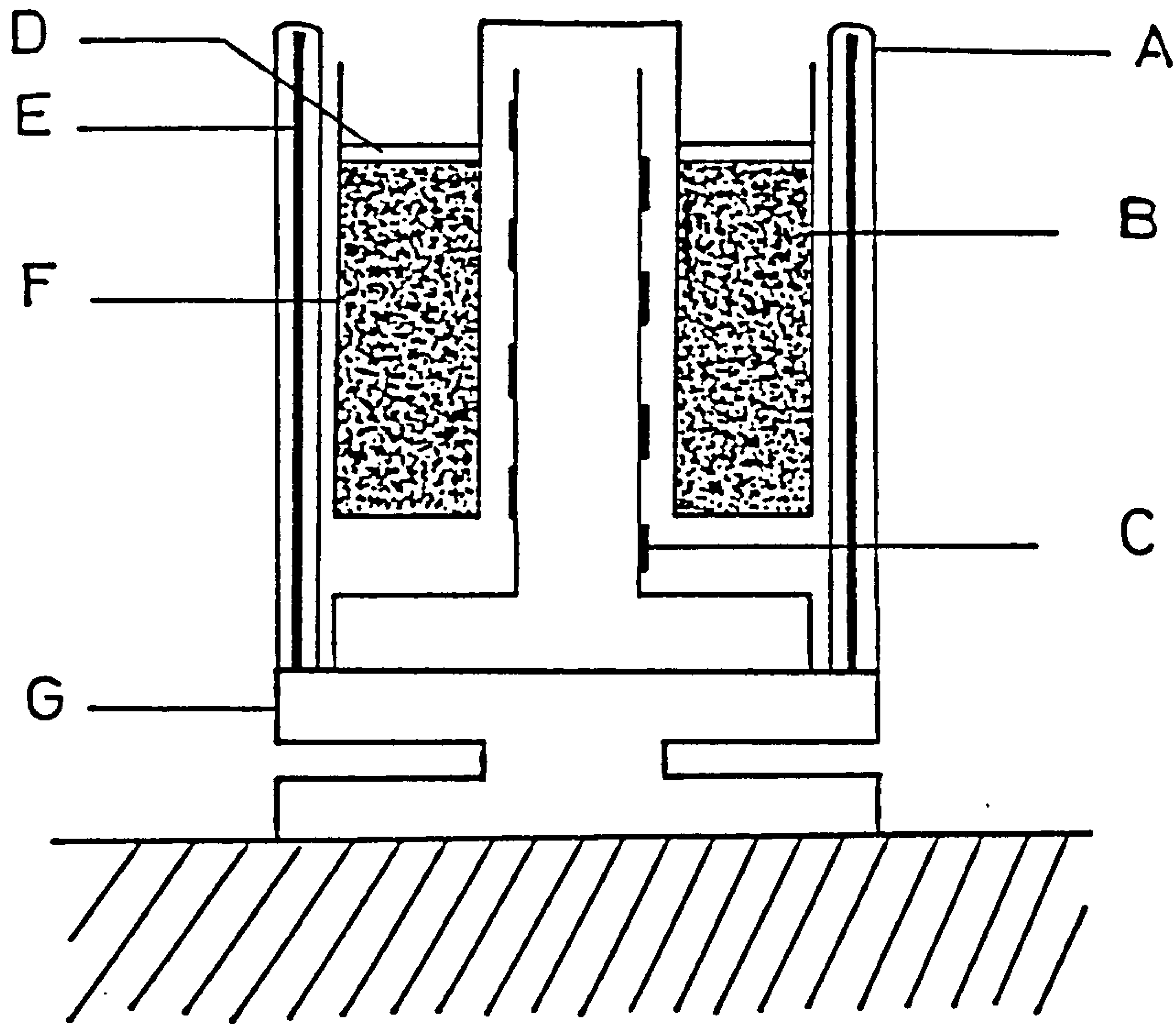


Figure (4-5) Source Container and heater.

A Quartz tube
B Quartz crucible
C Molybdenum heating element
D Quartz wool
E Stainless steel shield
F CdS powder
G Stand (pyrofolite)

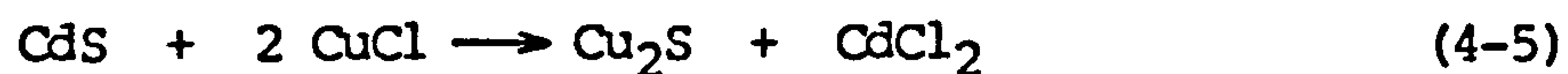
At the start of each evaporation cycle, a shutter was placed in position between the CdS source crucible and the substrate.

After pumping down to obtain vacuum less than 10^{-5} torr. The substrate was heated until outgassing was completed. To improve the quality and the reproducibility of the CdS thin film the substrate was heated to 300°C, and then dropped to the required temperature before starting the deposition. Gradually the quartz crucible and the hot-wall were heated, bringing the hot-wall to 200°C and the quartz crucible to 700-750°C, when the sublimation of CdS begins to be noticable. With the temperature of the substrate, the hot-wall and the quartz crucible adjusted to their required values, the rate of evaporation was allowed to attain a steady-state before the shutter was moved aside. Some immediate adjustment is then required to the substrate temperature which starts to rise due to the radiation heating from the high temperature source assembly. The temperature of the substrate could be controlled at any temperature between 200°C and 350°C, while the quartz crucible could be heated to temperatures up to 1100°C.

At the end of the evaporation, the substrate was once again covered by the shutter, and all the heaters were switched off. The system was cooled down to room temperature with care being taken to ensure that the substrate cooled slowly in order to retain good adhesion to the CdS film.

4.4 Formation of Copper Sulphide Layer

The formation of a p-n heterojunction is accomplished by converting the top layer of the CdS surface to copper sulphide via a chemical reaction with a solution of cuprous chloride in water and hydrochloric acid for short periods at about 95°C. The reaction follows as



$$CdS + 2\,CuCl \longrightarrow Cu_2S + CdCl_2 \qquad (4\text{-}5)$$

where a mutual exchange of two Cu^+ ions for every Cd^{++} ion from the CdS results in a topotaxial copper sulphide layer on the surface. The free-energy change for this reaction is $- 5.22 \times 10^4$ J $mole^{-1}$ (-1.4 eV $molecule^{-1}$) (42) and the forward reaction is thus highly favoured, particularly as the $CdCl_2$ is removed from the reaction area by going into the solution.

In order to improve the quality and the reproducibility of the copper sulphide layer, cuprous chloride powder was purified to remove the unwanted cupric ions, which may be present in the chemiplating solution. The cuprous chloride powder was first purified by dissolving in concentrated hydrochloric acid, which was decanted and precipitated in a large volume of deionised water. The pale green colour due to cupric ions (which are present in the powder as cupric chloride together with the cuprous chloride) in the solution is removed and fresh deionised water added to the deposit which is again allowed to settle. This was repeated several times until all traces of acid (containing soluble cupric ions) were washed away. This was indicated by the clear solution and a pure white deposit. Finally the CuCl was rinsed in alcohol and dried under vacuum.

The chemiplating solution was prepared using deionised water which was first boiled while nitrogen gas was bubbled through in order to remove the oxygen. The deionised water was cooled to about 60°C and 11 ml of hydrozine was added to 75 ml of the water. After adding 13 ml of concentrated HCl acid, the temperature of the solution rises to 70-80°C. Finally a known weight of purified CuCl powder was added (usually 0.5 gm) and the solution was stirred well while nitrogen gas was bubbled through. After heating to the required temperature (usually 95°C) the pH was adjusted to the required value (pH = 4 was usually used).

Prior to dipping the CdS layer into the Cu Cl solution, the edges of the CdS films were protected using a varnish which could withstand a temperature up to 200°C. The CdS films could be cut out as 1 cm square cells to be dipped singularly, or they could be left as a combined unit of up to 9 1cm square cells and dipped together.

In the actual chemiplating process, the CdS films were first chemically etched in concentrated HCl at room temperature for 5-10 seconds. The films were then cleaned in deionised water and thermally stabilized in a deionised water bath at about 80°C for a few seconds and then chemiplated in a CuCl solution as prepared above. Finally the films were rinsed thoroughly in deionised water and dried in nitrogen gas.

4.5 Cell Annealing

After the formation of the copper sulphide layer, the next step is the "forming" of the junction by means of heat-treatment. If performed in a suitable atmosphere the role of this treatment can be to form the junction and also to improve the stoichiometry of the copper sulphide layer. The best results in this programme were obtained when the cells were heated in flowing hydrogen at temperatures in the range of 150-200°C for a few hours. Heat-treatment in vacuum and in air were also investigated and it was shown that, for short annealing times, a vacuum gives similar effects to hydrogen, while air was found to be markedly different. Alternatively, for some cells, a thin layer of Cu (about 100 Å) was evaporated onto the copper sulphide layer, and the cells then heat-treated in air. The effect of the heat-treatment on the copper sulphide stoichiometry (in different ambient atmospheres) and on the electrical properties of the cells are shown and discussed in chapters (5) and (6).

4.6 Formation of the Front Contacts

Although it is possible to make a simple front contact by painting lines of silver paste (using a fine brush) on the top surface of the copper sulphide layer, much better results and much greater reproducibility are obtained by evaporating a linear array of gold grid lines through a mask. The mask made for this purpose was designed to produce grid lines of 20 μm width and optical transmission higher than 90%. A negative print was taken of a large scale drawing of the grid design and a photo etch technique used to make the mask using copper foil. The Cu foil was polished until it had a bright finish. A good finish could be obtained by polishing the Cu foil with Brasso which was then removed using trichloroethylene (C H Cl-C Cl_2). The foil was then transferred to a beaker containing 2% of concentrated lipsol liquid and washed in an ultrasonic cleaner for 5 minutes. The foil was then rinsed thoroughly in warm distilled water (until all the lipsol liquid was removed), and finally rinsed in methanol before being dried in a nitrogen stream.

A layer of positive (Shipley AZ-1350) photoresist was spread uniformly over the Cu foil and baked at 80°C for 30 minutes. The Cu foil was cooled to room temperature and the photographic negative was placed over it in front of a UV light (200 W high pressure Hg unfiltered lamp was used) and exposed for 1-2 minutes. The grid pattern was developed using Shipley AZ-351 developer diluted with distilled water (1:5) for 1 minute, then the Cu foil was baked at 80°C for a few minutes. The exposed area of the foil was then etched away using hexahydrate crystals of ferric chloride (500 g/l). The remaining photoresist was removed using acetone. The resultant masks had a grid structure with 16 lines cm^{-1}, and a grid width of the order of 40-50 μm as shown in Fig. (4-3).

In order to ensure that the grid lines had a sufficiently low resistance, a thickness of about 0.5 μm was used. Line widths of 40-50 μm were obtained consistently, yielding grid transmission of about 85% as can be seen in Fig. (4-3). The gold grids were joined up with silver paste and a fine wire of Cu was attached to complete the electrode.

4.7 The Scanning Electron Microscopy (SEM)

The SEM is a well-established research tool in many research fields [196]. It was designed to produce a magnified image of a surface. Some of the main advantages of this instrument are: the large depth of focus and high magnification, which gives considerable perspective to the image, the possibility of examining relatively large samples at low power and high magnification.

In this work a Stereoscan 600 scanning electron microscope (Cambridge Scientific Instruments Limited) was used. It has a switched magnification range between X20 and X50,000 which represents a scanned area on the sample from 6 mm x 5 mm to 2.4 μm x 2 μm. The sample holder can be positioned at any tilt angle between 0 and 90°, and the sample stub can be rotated in the holder.

The SEM was used to study the grain structure and surface texture of the CdS thin films arising from different fabrication processes, and also to determine the grain size and the thickness of the CdS films.

4.8 Auger Electron Spectroscopy (AES)

Auger electron spectroscopy was discovered in 1925 by Pierre Auger [197]. In recent years, as a result of advances in high vacuum

technology, it has become a powerful method for solid surface and thin film analysis and it is now commonly used in both industrial and research laboratories [198, 199].

The emission of Auger electrons is a secondary effect which occurs when an atom is subjected to X - irradiation or particle bombardment. Under such treatment atoms of the material become ionised, electrons in the inner orbits being ejected. This leaves the atom in an excited state and it may return to a lower state by an electron dropping from an outer orbit. This releases an amount of energy equal to the difference between the two energy levels involved. This energy may be transferred to another electron which is ejected in consequence. This is known as the 'Auger effect' and the ejected electron as an 'Auger electron'.

Although X-rays and ions can be used for the excitation, AES is best performed by using relatively low energy (usually 1-10 keV) electrons.

The principles underlying the technique are illustrated in Fig. (4-6). The basic requirement is the measurement of the kinetic energy distribution of secondary electrons. An Auger peak from an element of atomic number Z is found at an energy given approximately by

$$E_{wxy}(Z) = E_w(Z) - E_x(Z) - E_y(Z + A) - \emptyset_A \qquad (4\text{-}6)$$

where E_w, E_x E_y are the energies of individual levels relative to the Fermi level, $\emptyset_A$ is the work function of the energy analyzer material, and Δ allows for the change in the energy level since the atom is doubly ionized after Auger ejection. The experimental values for Δ have been found to be generally between 1/2 and 3/4 [197, 199].

A Vacuum Science Workshop Auger electron spectrometer (XAS 2000) was used for this work. This consists of two chambers, one for sample analysis and the other, with a differentially pumped Ar ion gun for sample processing. The system is diffusion pumped through long life cold traps

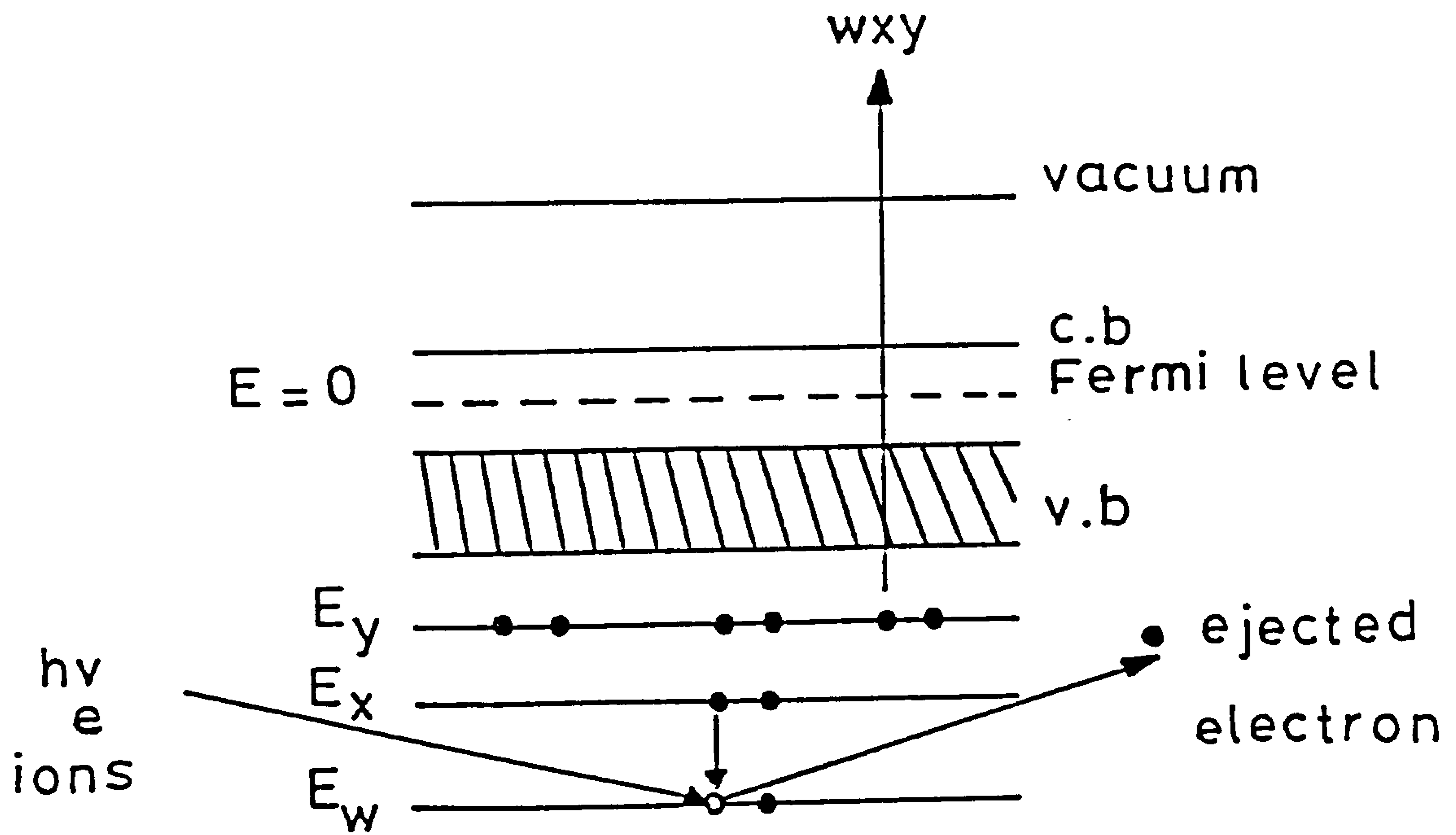


Figure (4-6) Energy level diagram of a singly-ionised atom (atomic number Z) in a solid semiconductor, illustrating the Auger process.

fitted with isolation valves. The sample transfer mechanism allows up to eight samples to be transported from the sample preparation chamber via a gate valve into the main analysis chamber. A 180° hemispherical analyser with an integral four element zoom lens was fitted in the system. Auger spectra were monitored at vacuum levels $<10^{-9}$ torr for the following elements at the indicated energy: Cu (920 eV), S (152 eV), Cd (376 eV), Cl (181 eV), O (508 eV) and C (272 eV). In order to minimize errors due to sputtering artefacts, such as surface damage, differential sputtering, etc., the Ar gun was operated at 10 μA at the low ion beam energy of 4kV. The milling rate was calibrated to be 4 nm min^{-1} using several films of known thickness. The elemental concentrations were determined from the peak heights. The peak heights are proportional to the elemental composition but they do not give the concentration of the concerned species in absolute terms.

The AES method is ideally suited for fast determination of concentration depth profiles and, in this investigation, has been used primarily for studying the interdiffusion processes associated with the degradation behaviour of the completed $CdS-Cu_xS$ thin film solar cells.

4.9 The Ion Implantation Facility

The ion implantation accelerator is shown diagrammatically in figure (4-7). The main features are the heavy ion source, constant field accelerator tube, magnetic separator, electrostatic quadrupole focus electrodes, x and y shift and scan deflector plates, first target chamber, accelerating column and second target chamber. Relative to the separator magnet the ion source could have a voltage of +100kV maximum, and the final target a voltage of -200 kV maximum giving the accelerator voltages of up

to 300 kV.

A sample of the material, containing the desired element to be implanted was ionised in the ion source. The desired ion species was separated from its isotopes and other unwanted ions in the magnetic analyser. The isotope separation is based on the principle that the accelerated ions, deflected by a uniform magnetic field, will travel along trajectories determined by their mass to charge ratio and energy.

All ions could be given equal energy (by stabilizing the pre-acceleration voltage) and thus trajectories of the particles were determined by mass to charge ratio alone. The ion beam passed through a series of equipotential planes, ending at earth potential, and then between the pole pieces of a 60° Lintott mass separator magnet. A slit placed in the path of the ion beam as it emerged from the magnet selected the required ion species from the beam and blocked the unwanted ions. The ions passing through the slit were focused by the quadrupole electrode system, and further electrodes shifted and rastered the beam. Neutral particles were removed by a neutral beam trap consisting of a set of electrodes which shifted the charged beam into a path displaced from its original path but had no effect on neutral particles. At this stage the ion beam could be used to implant a sample placed in the first target chamber, if an ion energy of 100 keV or less was required. The ions could be accelerated further by passing through another set of equipotential planes to a second target at a potential up to - 200 kV relative to earth. A further set of focus, shift and raster, and neutral beam trapping electrodes was placed between the second accelerator tube and the second target chamber. This accelerator tube consisted of nine aluminium accelerating electrodes, separated by pyrex spacers and protected on the inside by stainless steel.

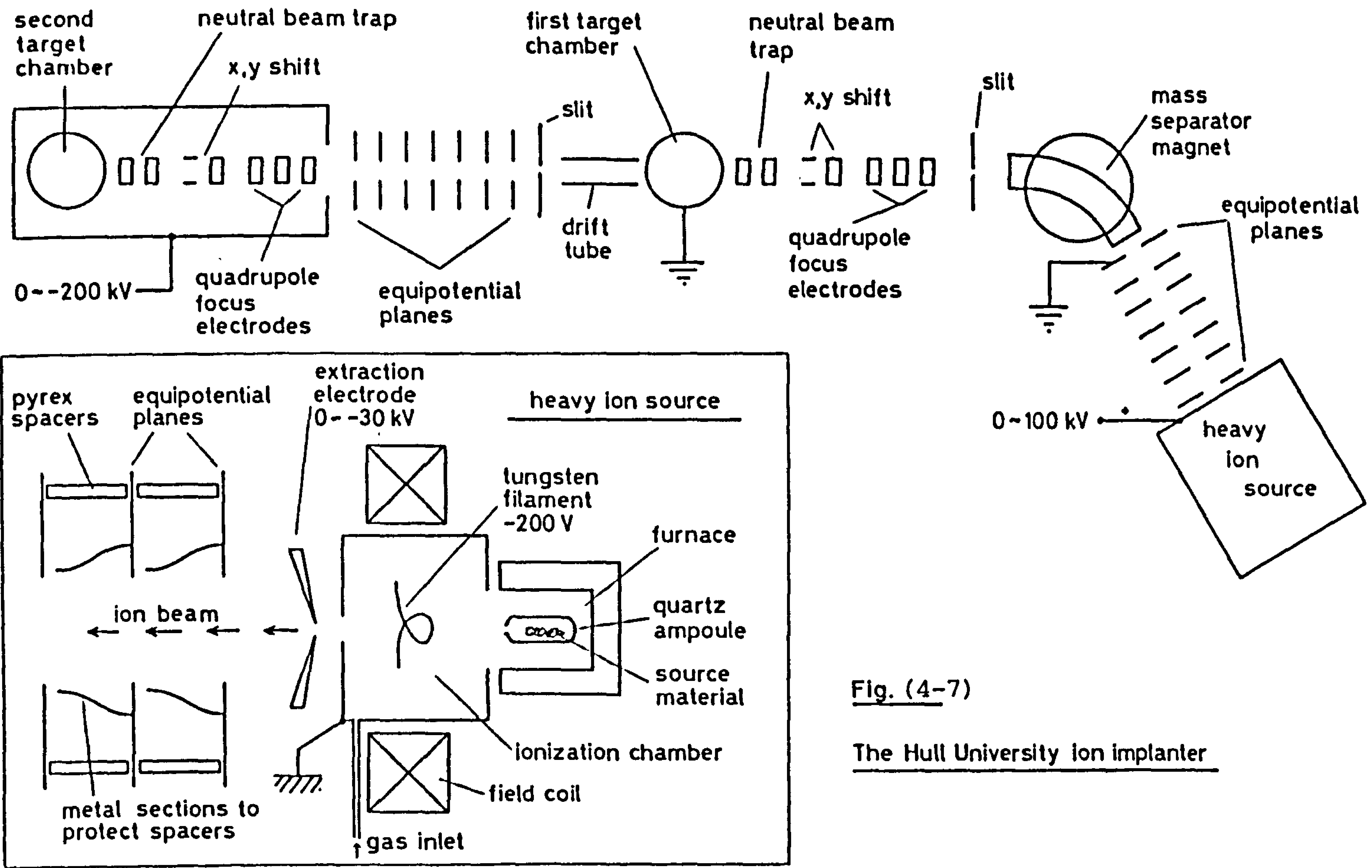


Fig. (4-7)

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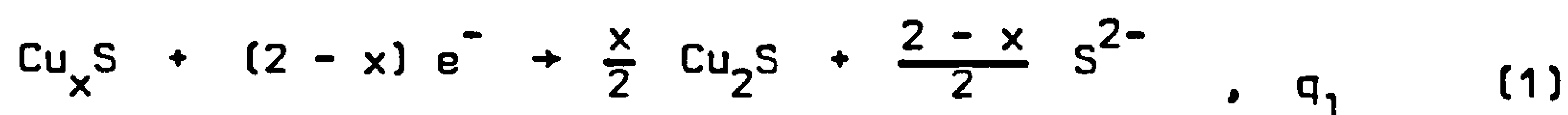
4.10 The Electrochemical Reduction Technique

The thickness and the stoichiometry of the cuprous sulphide layers were determined electrochemically by cathodic stripping. The method was essentially that employed by Castel [102], whereby measurements are made of the variations in the chemical potentials for the different Cu-S phases present in the copper sulphide layer by slow sweep chrono-potentiometry.

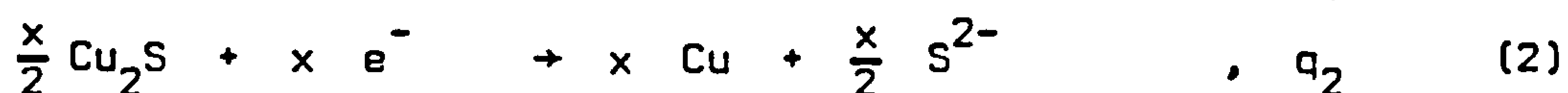
In order to measure the chemical potentials, a cell is constructed with the form

$$Pt \mid S^{2-}(aq) \mid Cu_xS \mid Pt$$

where S^{2-} represents sulphur with degree of oxidation 2, dissolved in an aqueous solution of neutral electrolyte. The chemical reduction from Djurleite to Chalcocite and further to copper takes place in two steps:



$$Cu_xS + (2 - x)\, e^- \rightarrow \frac{x}{2}\, Cu_2S + \frac{2 - x}{2}\, S^{2-} \quad , \; q_1 \qquad (1)$$



$$\frac{x}{2}\, Cu_2S + x\, e^- \rightarrow x\, Cu + \frac{x}{2}\, S^{2-} \quad , \; q_2 \qquad (2)$$

A study [102] of the variation of the normal potential in the above cell during the course of the reductions (1) and (2) has revealed that, given the basic properties of the sulphide anion, the reduction potential of copper sulphides (Cu_2S, $Cu_{1.96}S$, CuS) are a function of acidity of the electrolyte solution and the above two reactions are identified with the best separation when the electrolyte pH is equal to or greater than 8.

The experimental cell used in this investigation was similar to that employed by Castel consisting of a sodium acetate solution (0.1 M, pH 8.0), platinum anode, a reference electrode and the copper sulphide sample as cathode. The experimental arrangement for the potential measurement is shown in Figure (4-8). Prior to the measurement, pure N_2 gas was bubbled through the solution to drive off traces of dissolved oxygen. Later, during the experiment, an inert ambient (again N_2 gas was used) was formed

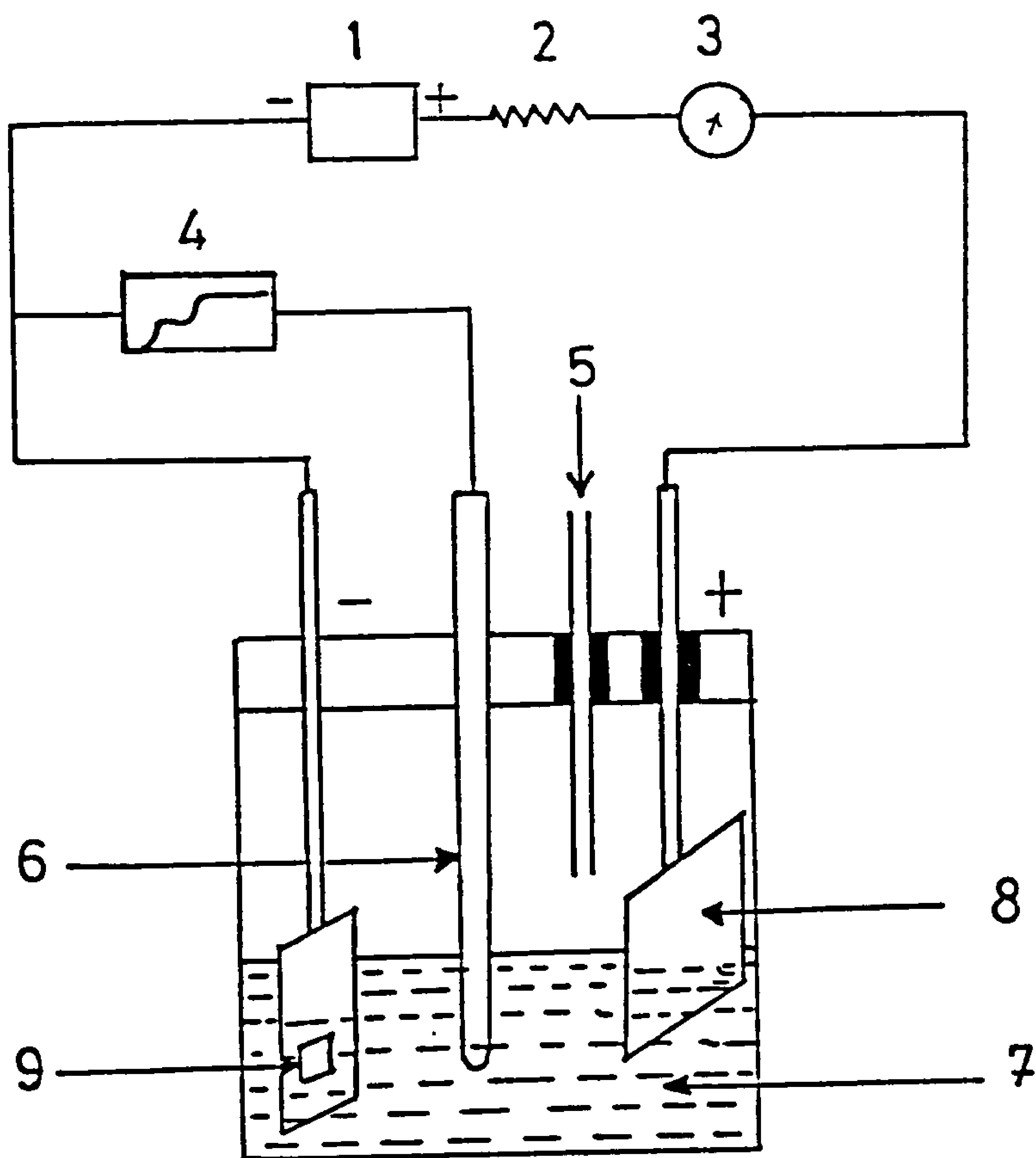


Figure (4-8) Electrochemical cell for studying the electrochemical reduction of copper sulphide films.

1 - DC voltage supply (∿ 300V)

2 - High resistance (∿ 5.75 MΩ)

3 - Keithley digital multimeter

4 - Recorder

5 - Nitrogen gas

6 - Colomel reference electrode

7 - 0.1 M Sodium acetate solution

8 - Platinum anode

9 - Exposed area of Cu_xS film (cathode)

above the solution.

While preparing the copper sulphide films for this experiment, extreme care was taken to use pin-hole free films. A non-conducting epoxy was applied to insulate all the other regions of the electrode immersed in the electrolyte except a small area (~ 0.2 cm x 0.2 cm) of the Cu_xS film itself. Low current densities in the range of 2.5×10^{-4} A cm^{-2} to 25×10^{-4} A cm^{-2} were maintained in the cell by using a high resistance in series with the power supply.

If q_1 and q_2 are the quantities of the electricity necessary to accomplish the two stages of the reduction as in (1) and (2), and, t_1 and t_2 are the respective reduction periods, then deviation from the copper sulphide stoichiometry

$$\delta = 2 - x = \frac{2\,q_1}{q_1 + q_2} = \frac{2\,t_1}{t_1 + \alpha t_2} \qquad (4\text{-}7)$$

where α in the last term is a factor by which the current is incresed to accelerate the reaction in the Cu_2S phase. The total quantity of copper formed can be deduced from

$$n_{Cu} = \frac{\alpha\, I\, t_2}{F} \qquad (4\text{-}8)$$

where F is Faraday's constant and I is the current flowing in the cell. The second step of the reduction can be used to calculate the equivalent planar thickness, $\bar{d}$, of the cuprous sulphide layer from the relation

$$\bar{d} = \frac{\alpha\, I\, t_2}{2\,F}\;\frac{M}{d}\;\frac{1}{S} \qquad (4\text{-}9)$$

where M, and d respectively are the molecular weight and the density of the copper sulphide taken to be 5.6 g cm^{-2}. S is the area of the sample. Figure (4-9) schematically illustrates the electrochemical data obtained experimentally in the form of a potential-time graph. Although the electrochemical method is a destructive technique, which yields only the

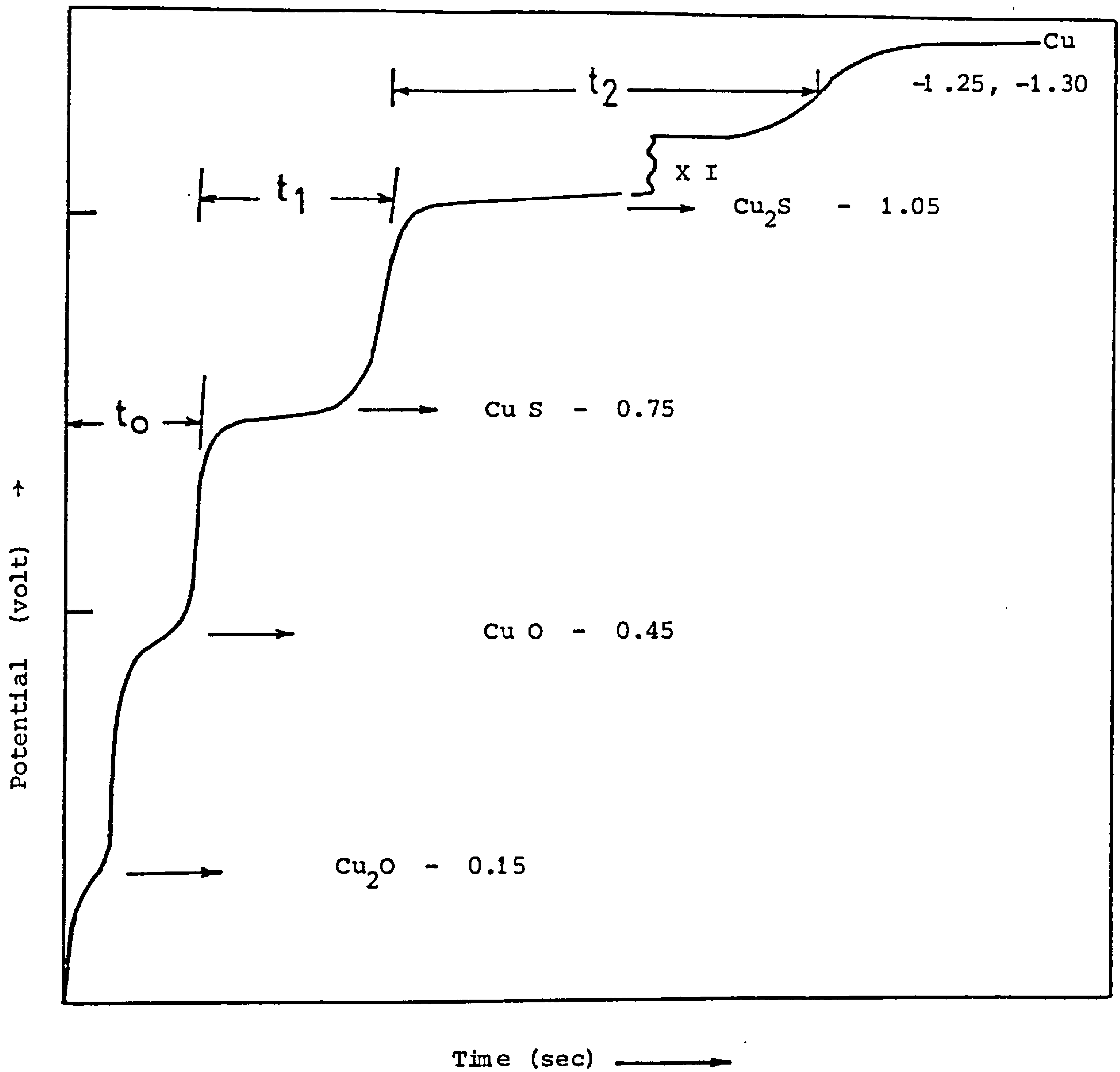


Figure (4-9) Representative potential-time graph showing respective chemical reduction of Cu-S Compounds.

average film properties, its application has been very helpful in developing an understanding of the copper sulphide film characteristics, and consequently of the heterojunction photovoltaic properties.

4.11 Sheet Resistance of the Copper Sulphide Layer

For the sheet resistance measurements, a linear four-point probe method was used. The same grid lines as shown in Fig. (4-3) were used in groups of four to make measurements of the sheet resistance. Current was passed through the outer two grids and the voltage (related to the sample resistivity) developed across the inner two grids was measured.

4.12 Resistivity and Carrier Concentration Determinations for the CdS thin films

The resistivity of the CdS layers perpendicular to the plane of the substrate (along the c-axis) was measured by the use of ohmic contacts on both faces of the CdS thin film. One of the contacts was the metal substrate itself, while the other was a circular evaporated indium dot on the front surface of the film. The resistance R between the two contacts was measured with a Keithley digital multimeter and the resistivity ρ calculated from

$$\rho = R \frac{A}{\ell} \qquad (4\text{-}10)$$

where A is the area of the indium dot and ℓ is the thickness of the CdS thin film.

The carrier concentration for the CdS thin films were obtained from capacitance-voltage measurements on Au/CdS Schottky diodes formed by evaporating circular dots of gold on to the front surface of th CdS films. The metal substrate once again provided the back ohmic contact. The diode

capacitance C was measured using a Boonton 72B capacitance meter with the reverse bias voltage V across the junction in the range between 0 and 3 volts. By plotting the data in the form C^{-2} against V, the carrier concentration was calculated from the slope of this graph using equation (3-43). This measurement could also be used to determine the space charge width and the diffusion voltage for both Au/CdS Schottky diodes and CdS/Cu_2S solar cells.

4.13 The Optical System for the Cathodoluminescence Analysis

The apparatus for studying the luminescence emission is shown diagrammatically in Figure (4-10). The cathodoluminescence was excited using 5 $\mu A\ cm^{-2}$, 10 keV electrons from an electron gun placed in the front of the sample so that the electrons struck the sample normally. The emission observed through a window in the cryostat was reflected through 45° by an adjustable mirror and mechanically chopped at 800 HZ before being passed through a Hilger Monospek monochromator which had a 1 mm grating blazed at 1 µm with slit widths of 0.25 mm. A photomultiplier was placed at the exit slit of the monochromator and the output from it was fed through a Brookdeal low noise amplifier and a Brookdeal phase sensitive detector into a potentiometric recorder.

The adjustable mirror was positioned to maximise the amount of emitted light incident on the entrance slit of the monochromator which had an electromagnetic clutch control and a synchronous motor for wavelength scanning. The electron gun focus and the x and y deflection plate voltages were adjusted to give uniform exposure of the sample as judged by observation of the visible cathodoluminescence emission from the sample.

The samples were mounted in an evacuated chamber on a rotatable metal

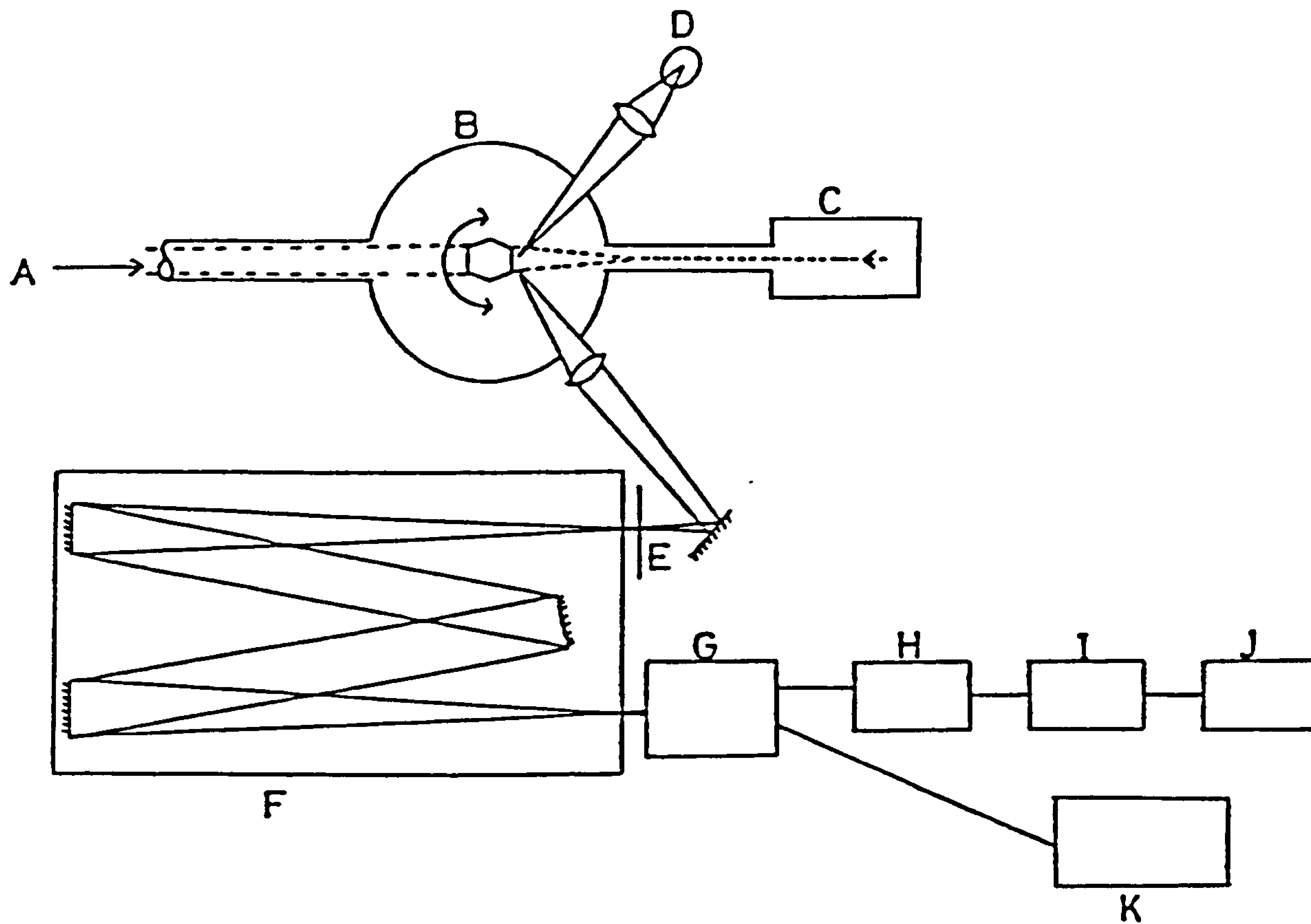


Figure (4-10) Arrangement of optical apparatus for studying luminescence emission before and after implantation.

A	Ion beam	B	Cryostat base and cold finger
C	Electron gun	D	Photoexcitation
E	Chopper	F	Hilger Monospek monochromator
G	Detector	H	Amplifier
I	Phase sensitive detector	J	Recorder
K	High Voltage Supply		

block having a hexagonal cross section, so that six different samples could be fixed on its six faces by using silver paste. The cathodoluminescence spectrum was recorded at liquid nitrogen temperature in a vacuum of $\sim 10^{-7}$ torr.

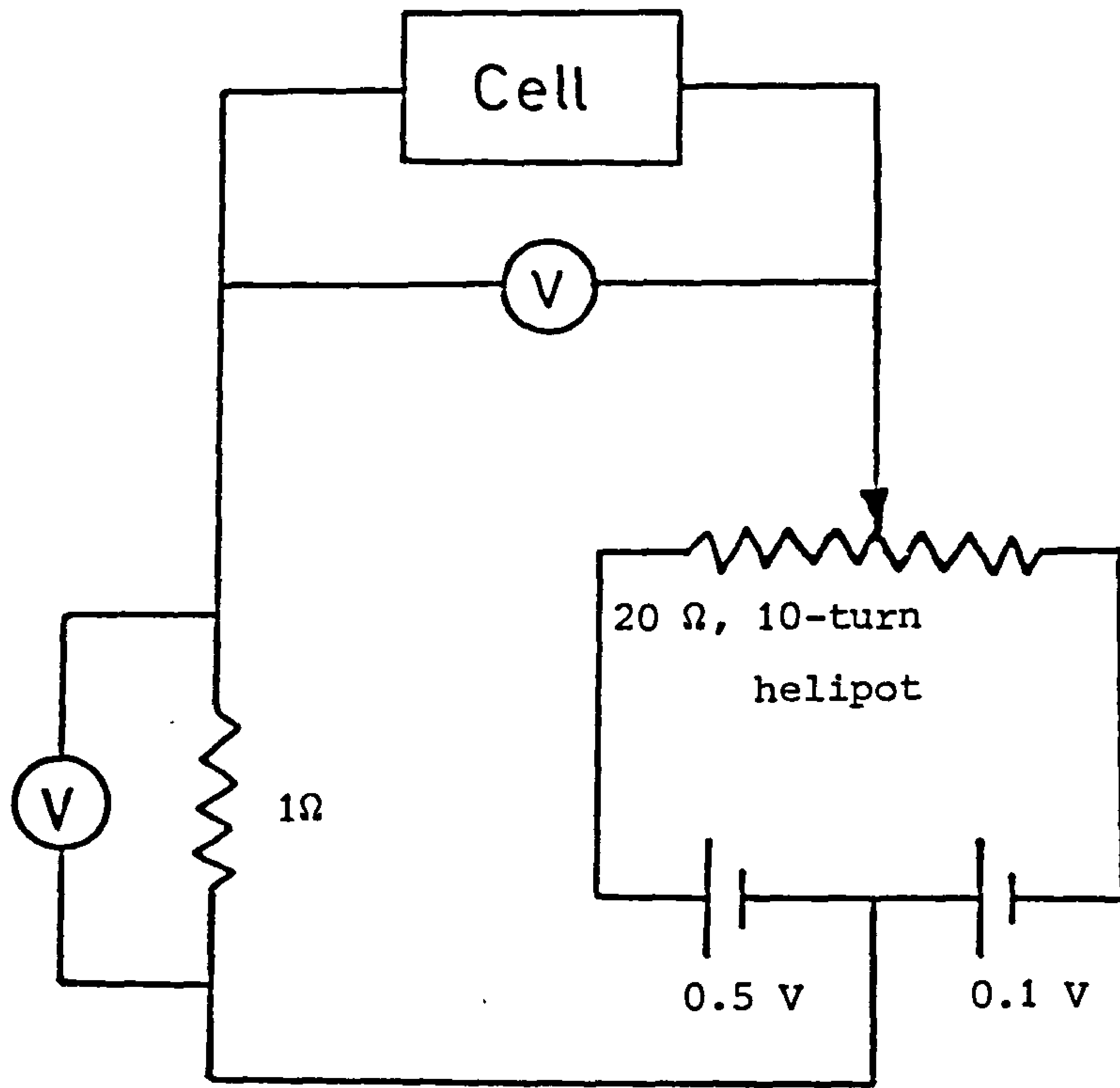
4.14 The Photovoltaic Spectral Response Measurements

The photovoltaic spectral response measurements were made at room temperature, with the cells illuminated normally using a Bausch and Lomb monochromator (grating blased at 0.3 μm), and a tungsten light source. The photovoltaic response was measured from 0.4 to 1.1 μm with a Wratten 88 A filter being used for wavelengths higher than 0.78 μm. For monitoring the spectral response of the open-circuit voltage a Keithley digital multimeter was used and the output recorded potentiometrically. Since the short-circuit current in this experiment was very small due to low intensity of incident light, great care was required to avoid stray effects due, for example, to background light in the laboratory. Therefore, for measurements of the spectral response of I_{sc}, the cell was connect ed with a Brookdeal low-noise amplifier and phase sensitive detector.

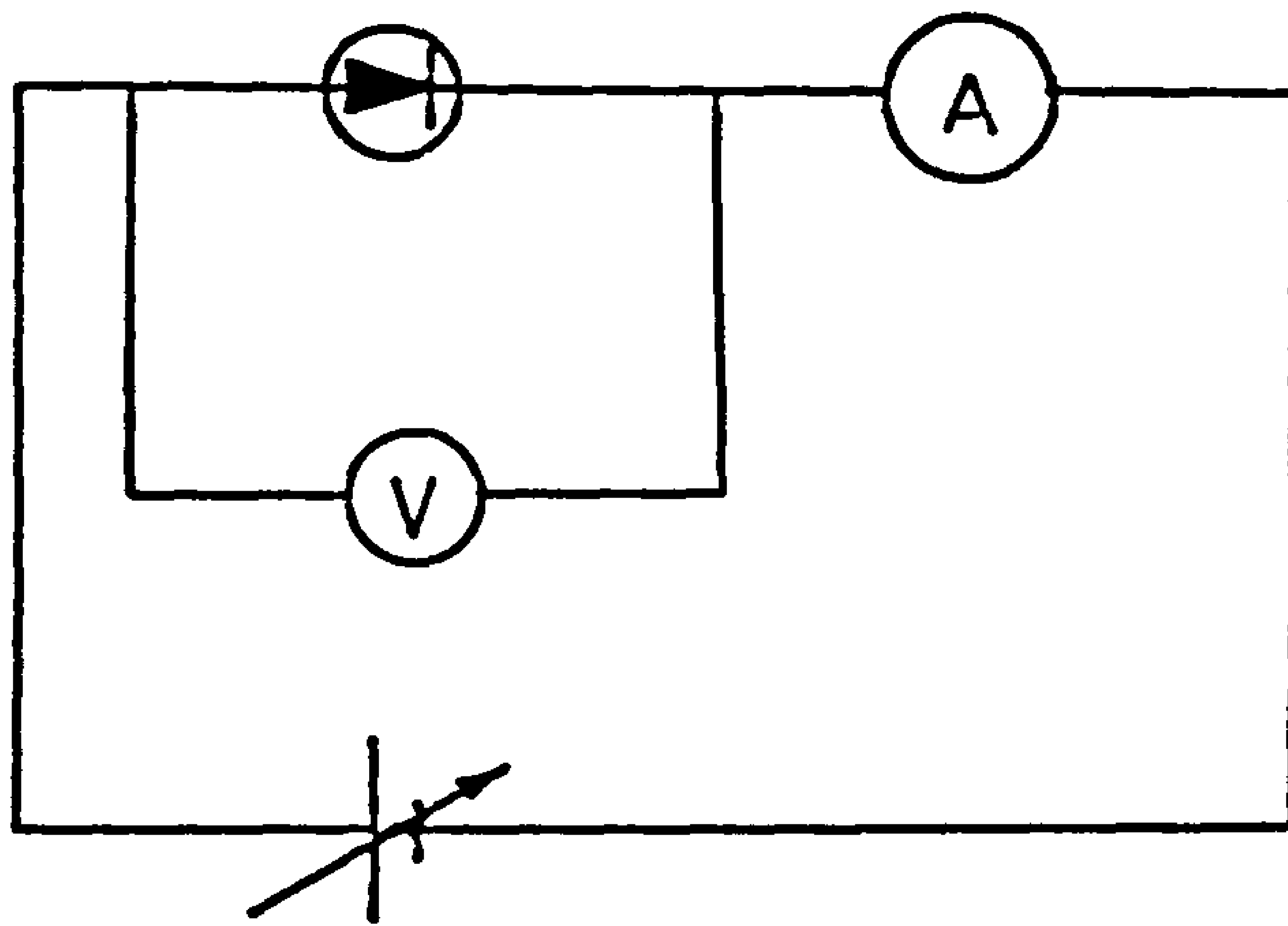
The spectral dependence of the incident light intensity was calibrated by the use of a standard PbS cell so that the spectral responses of the cells could be normalised for constant incident photon flux.

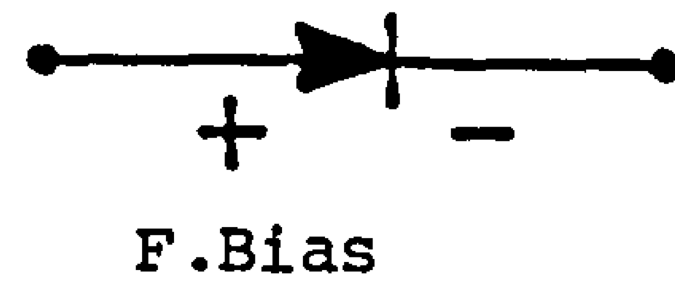
4.15 The Current-Voltage Characteristics

Figure (4-11a) shows the electrical circuit which was used to measure the current-voltage characteristics of the CdS-Cu_2S solar cells under

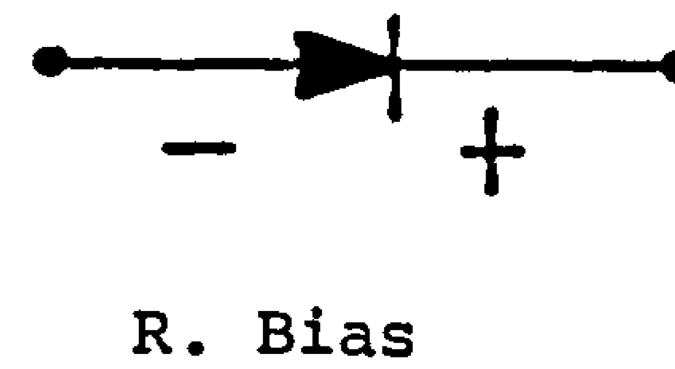


(a)





F.Bias



R. Bias

(b)

Figure (4-11) Circuits of measuring current-voltage characteristics.

various conditions. The voltage was measured directly across the cell and the current was measured by monitoring the voltage generated across a 1 ohm standard resistance. A Bryans 26000 x-y recorder was used to record the resultant characteristic as the externally applied bias was scanned manually. The light source illuminating the cells was a 1000 W tungsten lamp with a water filter to give an approximation to the solar spectrum (200). The light intensity was calibrated by use of a standard silicon solar cell which had been calibrated for AMO solar radiation (at which it gave a short-circuit current of 105.3 mA) but as the short circuit current I_{SC} of this cell is directly proportional to light intensity, the light source could be calibrated for different light intensities including AM1 which was the radiation level mostly used.

For I-V measurements at different temperatures the test cell could be mounted in a cryostat which could be evacuated to a pressure of 10^{-5} torr. A temperature control system was used to maintain steady temperatures in the range between 80 and 400 K. A copper-constantan thermocouple mounted near the sample was used to measure the temperature. Figure (4-11b) shows the basic principle of the electrical circuit which was used for these studies. Two Keithley digital multimeters were used to measure the current and the voltage under forward and reverse bias voltages which were provided from a stabilised DC power supply.

Chapter 5

Results

5.1 Development of thin film CdS-Cu_2S solar cells

5.1.1. The CdS layer

5.1.1.a. The effect of the substrate

Both the topography and thermal expansion properties of the substrate are crucial factors in determining the structural properties and defects of subsequently grown layers of CdS, but the substrate must also provide a low-resistance ohmic back contact to the CdS in order to minimize the series resistance of the completed cells. In order to determine which substrate had the best characteristics in terms of reproducibility, stability and high efficiency cell performance, a variety of possible systems were investigated. Table (5-1) summarizes some of the results, indicating the quality of the adhesion, ohmicity and back contact resistance between the substrate and the CdS films. The table shows that only zinc coated Mo, Al and Cu sheets, and Pb coated glass sheets gave both good adhesion and low back contact resistance.

In order to provide a further check, several different substrates were placed in the vacuum chamber at the same time and then the CdS deposition was carried out. Table (5-2) shows the resistance between the substrate and a 0.2 cm indium dot deposited on the top surface of CdS films. The first three substrates show a low resistance between the indium dot and the metallic substrate. Such a resistance is due to the resistivity of the CdS film itself, and these substrates provide a linear relationship between the current and the voltage. The other substrates have a high resistance due to the unsatisfactory back contact.

Fig. (5-1) shows the scanning electron micrographs for one batch

Table (5-1) Adhesion, ohmicity and back contact resistance for different substrates.

	Adhesion	Contact ohmicity	Back contact resistance
A - Metal Sheet Substrate			
Mo	Good	not always ohmic	high
Al	"	ohmic	very high
Ag	"	not always ohmic	high
Ti	"	ohmic	very high
Cu	Poor	rectify	very high
B - Thin film deposited on metal sheet substrate			
Zn on Mo	Good	ohmic	low
Zn on Al	"	"	"
Zn on Cu	"	"	"
Ti on Cu	Poor	"	"
In on Cu	"	-	-
In on Mo	"	-	-
C - Thin film deposited on glass sheet coated with Cr.			
Zn	poor	ohmic	low
Cu - Zn	poor	ohmic	low
Pb	good	ohmic	low
Sn	poor	-	-
In	poor	-	-
Ag	good	not always ohmic	high

Table (5-2). The resistance between the substrate and the CdS film.

The CdS was evaporated at a rate of 1μm min^{-1} and substrate temperature 230-240°C.

Substrate	Resistance (Ω)
Zn thin film on Cu sheet	0.5
Ti thin film on Cu sheet	0.75
Pb thin film on glass sheet	0.82
Ag thin film on glass sheet	10.8
Mo sheet	18
Ti sheet	100.8

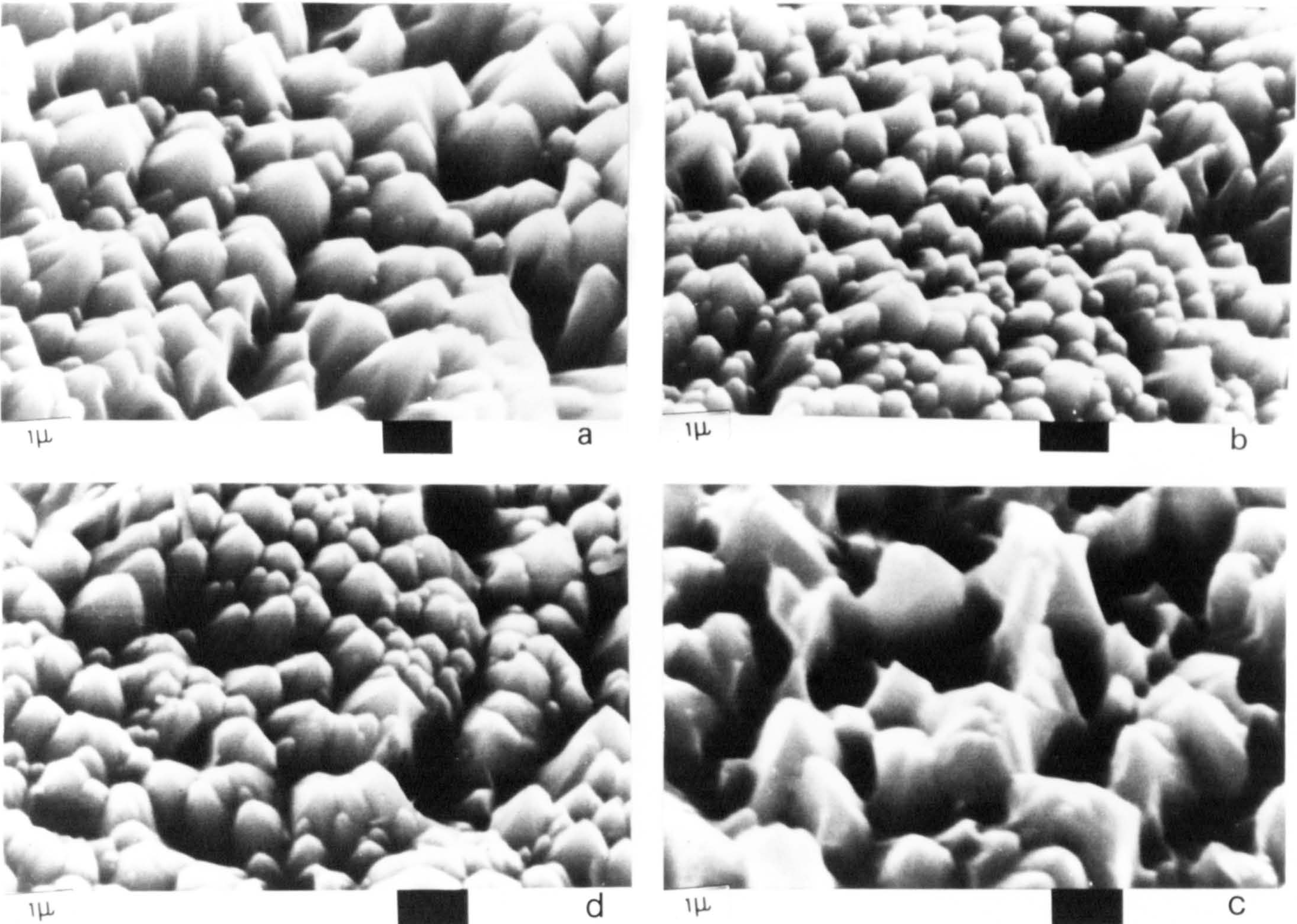


Figure (5-1) SEM micrographs for one batch of HCl acid etched CdS films grown on different substrates, (a) zinc coated copper, (b) zinc coated Mo, (c) zinc coated Al and (d) Pb coated glass viewed at tilt angle of $\sim 30^{o}$.

of CdS films grown on different substrates. The Zn coated Al substrate is shown to be associated with a low packing density and some pinholes, while CdS films grown on zinc coated Cu and Mo together with Pb coated glass substrates show a good packing density. However, the grain sizes were somewhat similar for all the CdS films.

In view of these results and the work of other investigators (see chapter 2) a special effort was devoted to developing a reliable fabrication procedure for CdS-Cu_2S cells on zinc coated copper substrates. The zinc layer is necessary to prevent the direct formation of copper sulphide by the reaction of the copper with the S_2 molecules arriving from CdS vapour. In addition, zinc serves as an effective ohmic contact to the CdS. One advantage of this substrate is due to the interdiffusion between the zinc and the copper during the substrate baking and CdS deposition. This interdiffusion leads to the formation of high reflectivity brass at the surface of the substrate. Because of the superior reflection properties of pure copper and low zinc brasses [202,203], it is desirable to keep the initial Zn layer as thin as possible. To achieve the optimum thickness of zinc, that is sufficient zinc to inhibit direct copper sulphide formation but a thin enough layer to result in maximum light reflection and good ohmic characteristics, different thicknesses of zinc layer were tried. Results indicate that a maximum in the short-circuit current is obtained when the thickness of the zinc layer is in the range between 0.2 - 0.5 μm, in agreement with the work by Bragagnolo [202]. At this thickness the adhesion for the CdS layer was good but it should be noted that some adhesion problems have been encountered for zinc layers thinner than 0.1 μm or for zinc layers evaporated under poor vacuum conditions.

The adhesion of thin films of Cu and Zn on glass substrates was

poor and the copper films peeled from the substrate at various stages of processing. The adhesion was improved when the substrate temperature was raised to ~ 300°C prior to deposition but the zinc coated copper sheet substrate was found to be much better and more reproducible.

In order to explore the effect of surface texture of the substrate, the growth of CdS on smooth and rough surfaces of zinc coated copper foil was also investigated. The unetched surface of the CdS on a smooth substrate was found to be much flatter than for a rough substrate but the adhesion of the CdS was not as good as that on the rough substrate so that difficulties in cell fabrication were encountered. Accordingly, the standard substrate used for all subsequent investigations was rough textured, zinc-coated copper foil.

5.1.1.b. The effect of CdS powder

In the early work on this project a variety of different CdS powders were investigated. The aim was to determine the relationship between the source material and the grown CdS films. Fig. (5-2) shows the cathodoluminescence emission spectrum for two different CdS powders. Curves A and C are for the "as received" CdS powders, while curves B and D are for the sintered powders. The sintering process was carried out by heating the CdS powder in vacuum (~ 10^{-5} torr) for 10 hours at 400°C, and then sealing off in vacuum the quartz tube containing the CdS powder before baking it for 2 days at 900°C.

Changes in the composition of the CdS powders are expected to occur during the sintering process. Indeed, when the Koch-light CdS powder was sintered, a thin layer of sulphur (or probably sulphur-rich CdS) was seen to be deposited on the quartz tube of the cold trap, while for

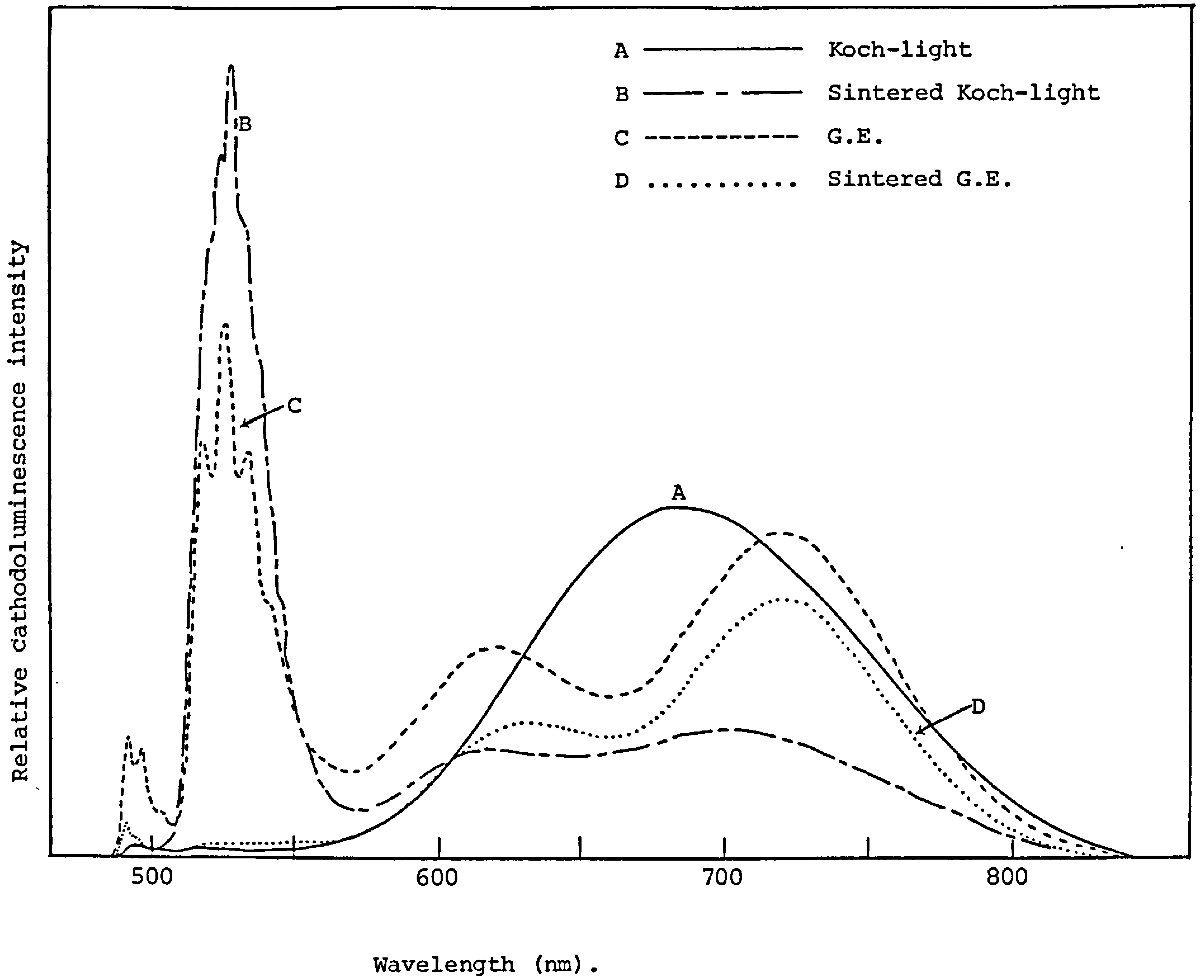


Figure (5-2) Cathodoluminescence emission spectrum of two CdS powders taken before and after sintering treatment.

General Electric powder a thin layer of cadmium was deposited. Thus, the effect of sintering is to change the stoichiometric composition of the CdS powder so that the atomic ratio of Cd/S is increased for Koch-light CdS powder, and is decreased for General Electric powder. Fig. (5-2) shows the sintering treatment to have a marked effect on the luminescence properties. For example, the intensity of the edge emission for Koch-light CdS powder increased significantly while it diminished for the General Electric powder. Similar marked variations have been found in the electrical properties of the CdS films produced using these powders. This is illustrated by the results in Table (5-3), which were obtained when the film deposition rate and the substrate temperature were 0.6 μm min^{-1} and 230-240°C respectively.

Table (5-3) Carrier concentration and resistivity values of CdS thin film obtained using different CdS source powder.

Source material	Carrier concentration (cm^{-3})	Resistivity (Ω cm)
G.E. CdS powder	5.33×10^{16}	42.7
Sintered G.E. CdS powder	8.5×10^{15}	1050
Koch-light CdS powder	2.4×10^{17}	25.0
Sintered Koch-light CdS powder	8.5×10^{17}	7.3

The structural properties of the films also depend on the chosen source powder, as can be seen in Figure (5-4) which shows the effect of the sintering treatment for films formed from Koch-light powder. It should be noted that films prepared by evaporating the "as received" Koch-light CdS

powder showed a low packing density and a large number of pinholes after acid etching. Furthermore, although quartz wool was used to plug the CdS source bottle some particles of CdS tended to be projected onto the substrate during the evaporation process. This was due to the fact that the "as received" Koch-light CdS was in the form of a very fine powder. This problem could be overcome by decreasing the rate of evaporation, but this had a further effect on the electrical properties of the CdS films, as discussed in section (5.1.1.c). The effect of the evaporation process on the resultant film properties is further demonstrated by comparing the spectra in Fig. (5-2) with those in Figure (5-3) which shows the cathodoluminescence emission spectra for the CdS films prepared using the 4 different CdS powders. (Curves A - D were obtained for the same 4 CdS films referred to in Table 5-3). The two peaks observed in the vicinity of 490 and 520 nm in the CdS powders have been extensively investigated in CdS single crystals [204]. The lower wavelength (higher energy) peak is due to an excitonic transition, while the green edge emission peak (lower energy) is attributed to the recombination of a free electron with a hole bound to a native defect, probably the cadmium vacancy, or an impurity acceptor. The longer wavelength peaks in the cathodoluminescence spectra are due to other defects in the CdS films. The large peak observed at about 690 nm for the "as received" Koch-light CdS powder is considerably diminished in the thin film (Curve A), while the edge emission peak shows a significant increase in magnitude. Other differences between the emission spectra for the powder and thin film samples can be seen but the overall emission and relative intensities of the various emission bands depend strongly on the film deposition parameters. It is interesting to note that, in general, those layers which display poor cathodoluminescence (e.g. curve D in Figure 5-3) are found to form low efficiency cells.

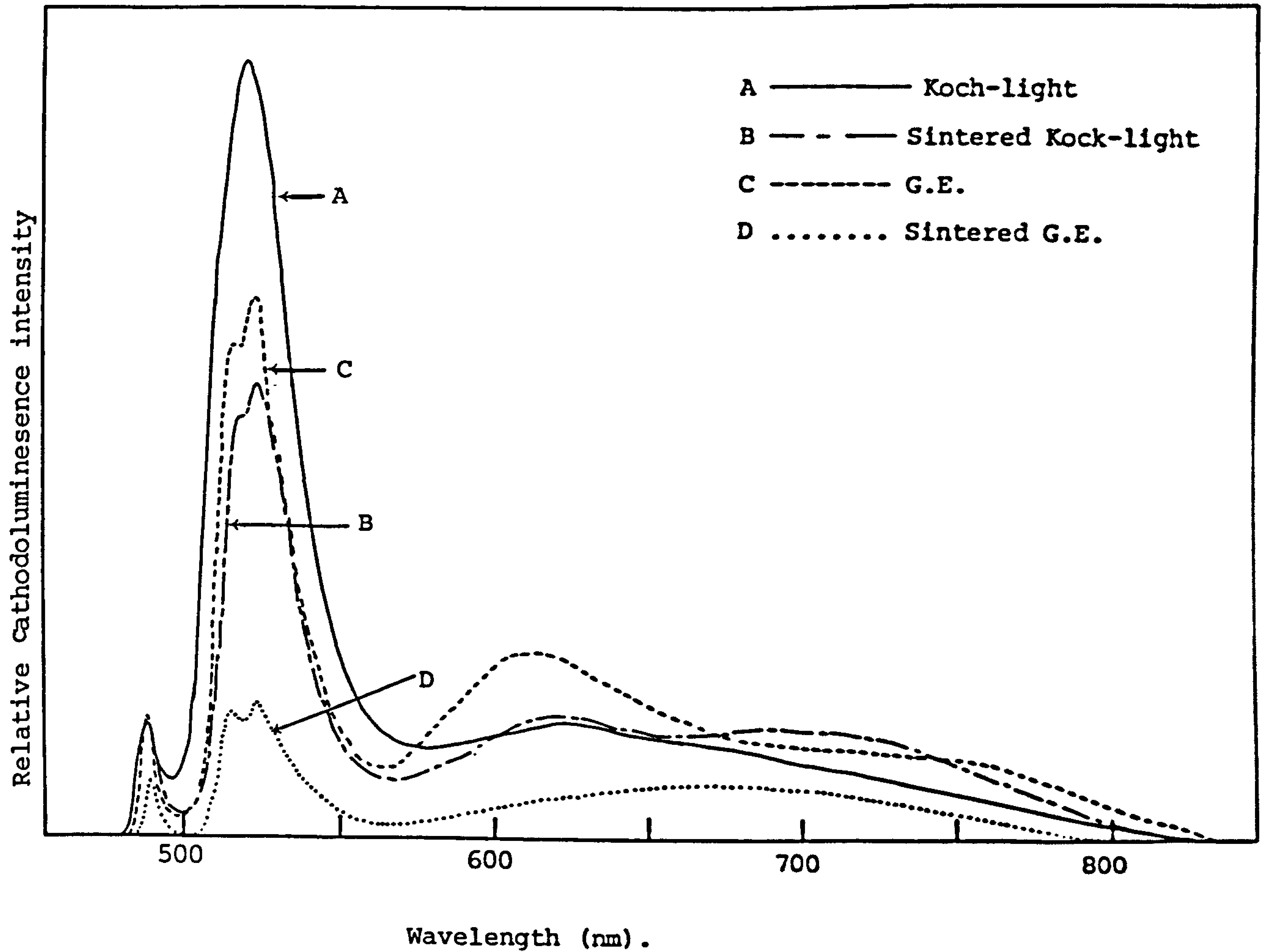


Figure (5-3) Cathodoluminescence emission spectrum of CdS thin films prepared from different CdS powders, and using substrate temperature of 230 - 240°C and deposition rate of 0.6 μm/min.

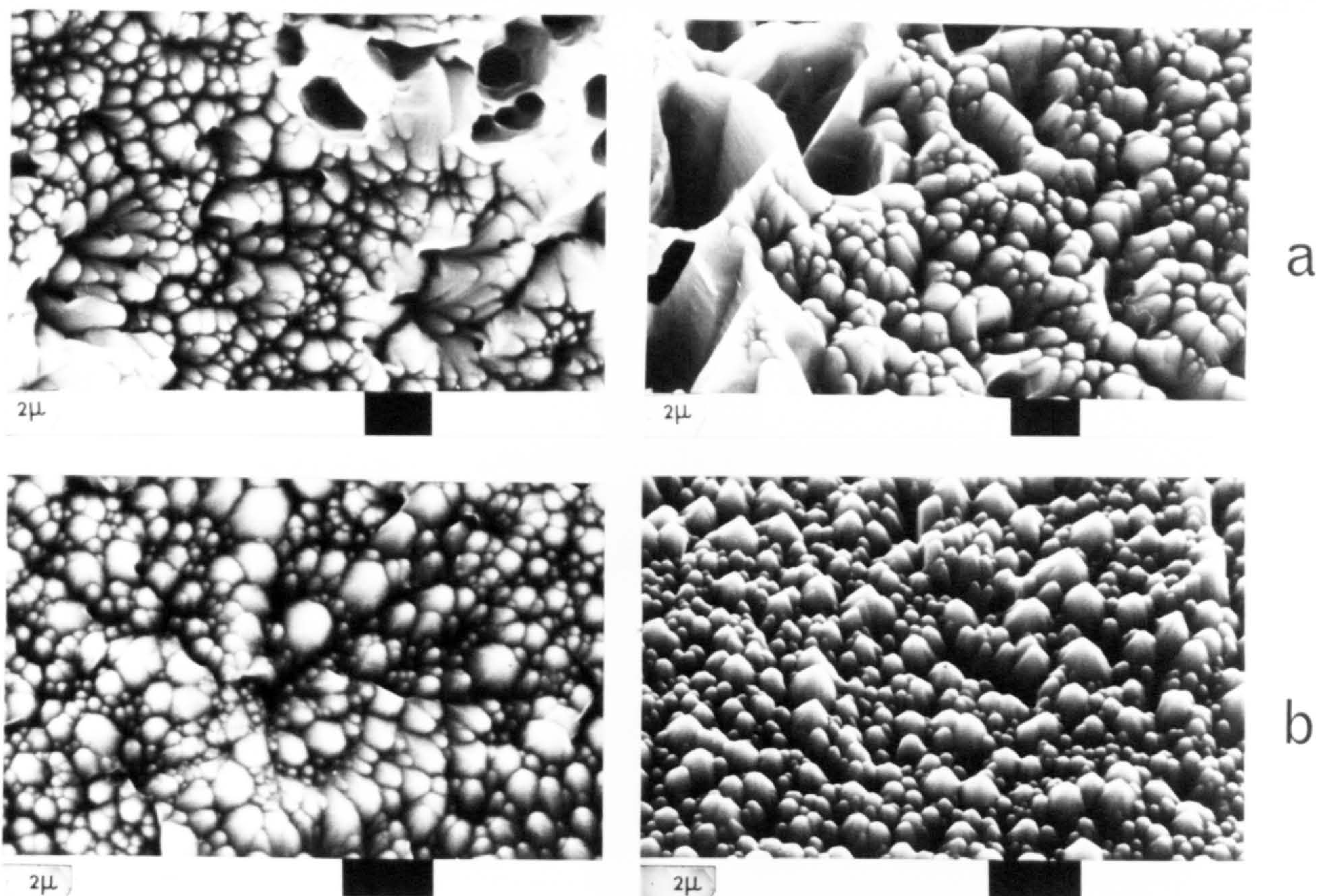


Figure (5-4) SEM micrographs of HCl etched CdS films prepared from (a) as received Koch-light CdS powder and (b) Sintered Koch-light CdS powder, viewed at normal incidence and at tilt angle of $\sim 30^{o}$.

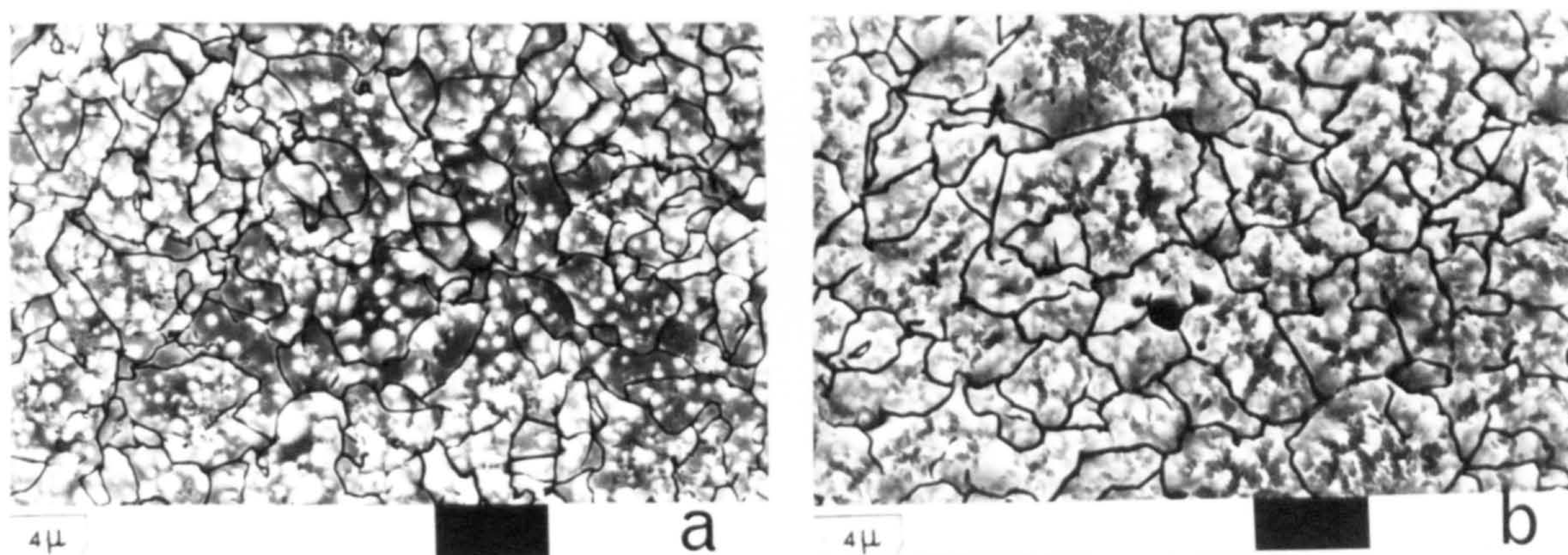


Figure (5-5) Typical SEM micrographs of two $CdS-Cu_2S$ cells after removal of the Cu_2S layer by leaching in 0.1 N KCN Solution. The cells fabricated using two CdS films prepared at two substrate temperatures, (a) 200 - 210°C and (b) 230 - 240°C.

Due to the problems of evaporating unsintered Koch-light powder (mentioned above) the reproducibility of CdS films formed from this source of CdS was poor. However, this problem did not arise when using either sintered Koch-light or General Electric CdS powder, which reliably produced good quality CdS films suitable for fabricating high efficiency solar cells providing that the growth conditions, such as the substrate temperature and deposition rate, were optimized.

5.1.1.c. Substrate temperature and deposition rate

The influence of the deposition rate and the substrate temperature on the electrical properties of the CdS films prepared using sintered Koch-light and the "as received" General Electric CdS powder is seen in the results shown in Table (5-4). It should be noted that in calculating the resistivity and carrier concentration account has been taken of the variation in film thickness which ranged from ~ 30 μm for the films prepared at the lowest substrate temperature to less than 20 μm for the films deposited at > 250°C. This is due to the fact that once the vapour molecules have condensed on the substrate surface re-evaporation can occur and the rate of re-evaporation increases with substrate temperature. The upper limit for the film deposition rate as shown in Table (5-4) was 1 μm min^{-1}, because at higher source evaporation rates spattering of the CdS powder became a problem, with powder particles being seen on the CdS films when they were examined under an optical microscope. The lower limit of the substrate temperature was 200°C, because the substrate received considerable radiation heat from the furnace. It should be noted that all films in Table (5-4) were deposited with care taken to ensure that the hot-wall temperature (200°C), the source-substrate separation, the

pressure and the CdS source degassing procedure were identical during the different evaporation cycles for these films.

The results in Table (5-4) show that the resistivity of the CdS films increases with increasing substrate temperature and decreases with the deposition rate, while the carrier concentration decreases with increasing substrate temperature and increases with increasing deposition rate. These findings are in good agreement with the work of Dimova [205]. Wilson and Woods [65] obtained similar results for the effect of the substrate temperature on the electrical resistivity of CdS films when the substrate temperature was above 150°C, but the effect of changing the evaporation rate was different to that observed here. However, a direct comparison between these results is not valid because the films examined by Wilson and Woods were much thinner than those considered here and film thickness is known to have an important influence on the properties of evaporated layers.

It is clear from Table (5-4) that, although the trend for the resistivity and carrier concentration values were in the same direction for both series of films, the absolute values of the carrier concentrations for the film prepared from sintered Koch-light CdS powder are approximately one order of magnitude higher than for the films prepared using General Electric CdS powder. Such a difference could be due to differences in the stoichiometry such that the atomic ratio of Cd/S was higher for the sintered Koch-light than for the unsintered General Electric powder. Alternatively, differences in the quantity and variety of trace impurities in the two different sources would be expected to exert an important influence on the electrical properties of the resultant films.

The effect of the deposition rate and substrate temperature on the grain size was studied by means of the scanning electron microscope.

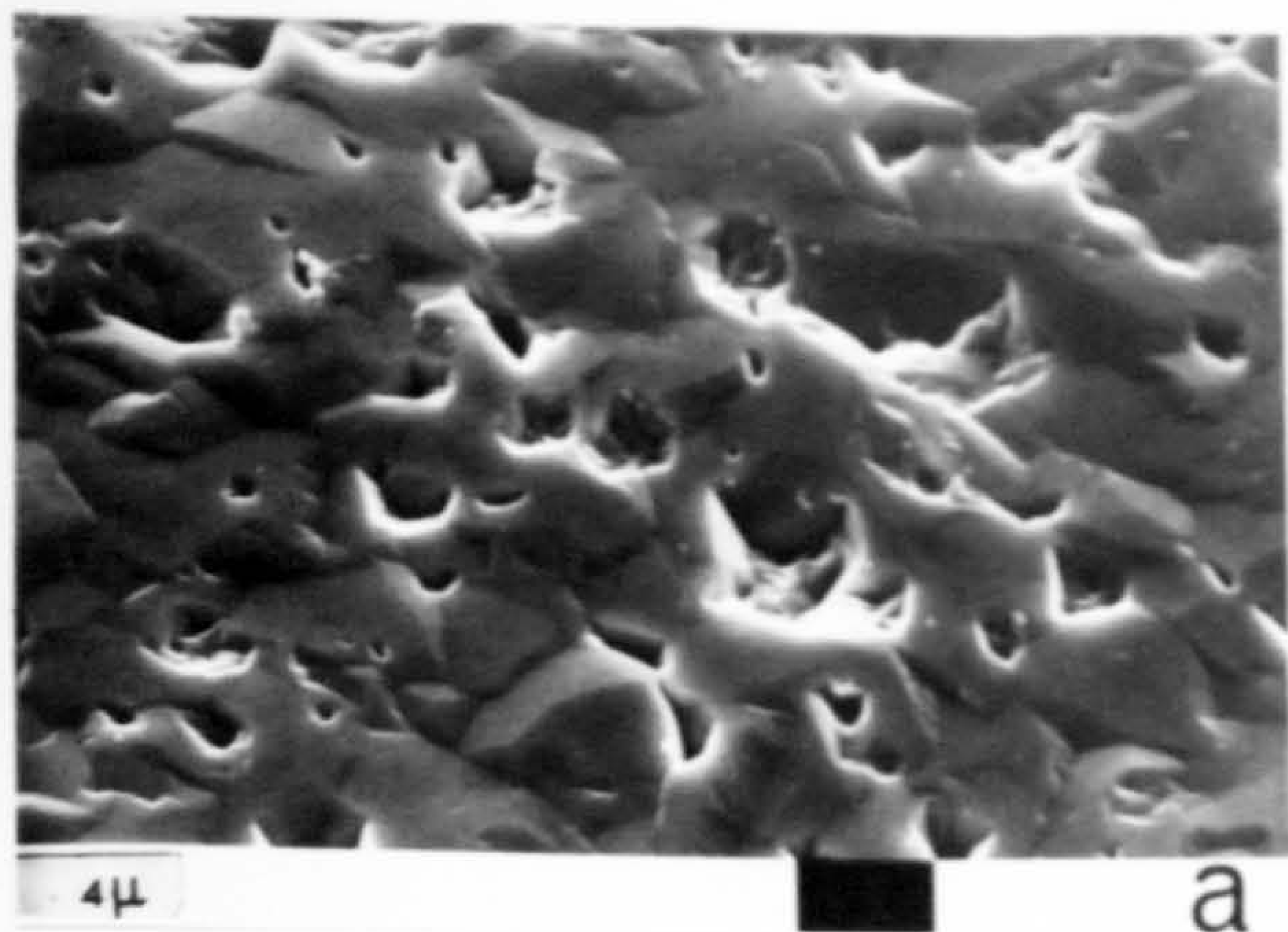
Table (5-4). Carrier concentration and electrical resistivity of CdS films prepared at different substrate temperature and deposition rate.

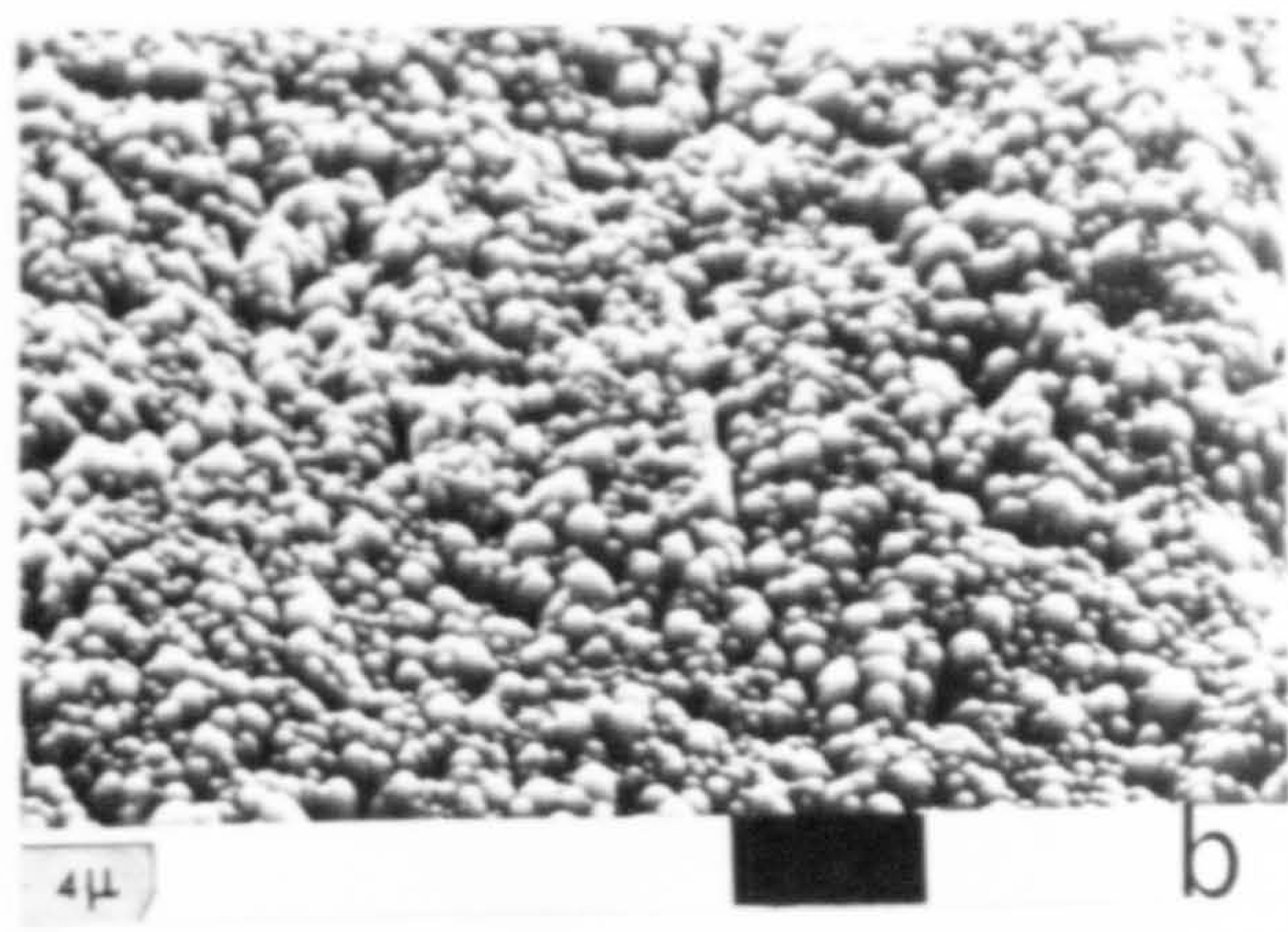
Source material	Deposition rate ($\mu m\ min^{-1}$)	Substrate temperature (^{o}C)	Carrier concentration (cm^{-3})	Resistivity (Ω cm)
"as received" G.E. CdS powder	1.0	230 - 240	2.09×10^{17}	9.5
	0.6	230 - 240	8.33×10^{16}	42.7
	0.3	230 - 240	1.5×10^{16}	187.5
	0.07	230 - 240	7.25×10^{15}	944
	1.0	200 - 210	8×10^{17}	5.1
	1.0	230 - 240	2.09×10^{17}	9.5
	1.0	260 - 270	5×10^{16}	450
	1.0	290 - 300	2.1×10^{15}	3063
Sintered Koch light CdS powder	1.0	230 - 240	1.4×10^{18}	1.0
	0.6	230 - 240	8.5×10^{17}	7.3
	0.5	230 - 240	6.2×10^{17}	9.5
	0.3	230 - 240	3.4×10^{17}	14.7
	0.5	200 - 210	1.58×10^{18}	1.19
	0.5	230 - 240	6.2×10^{17}	9.5
	0.5	260 - 270	8.9×10^{16}	340

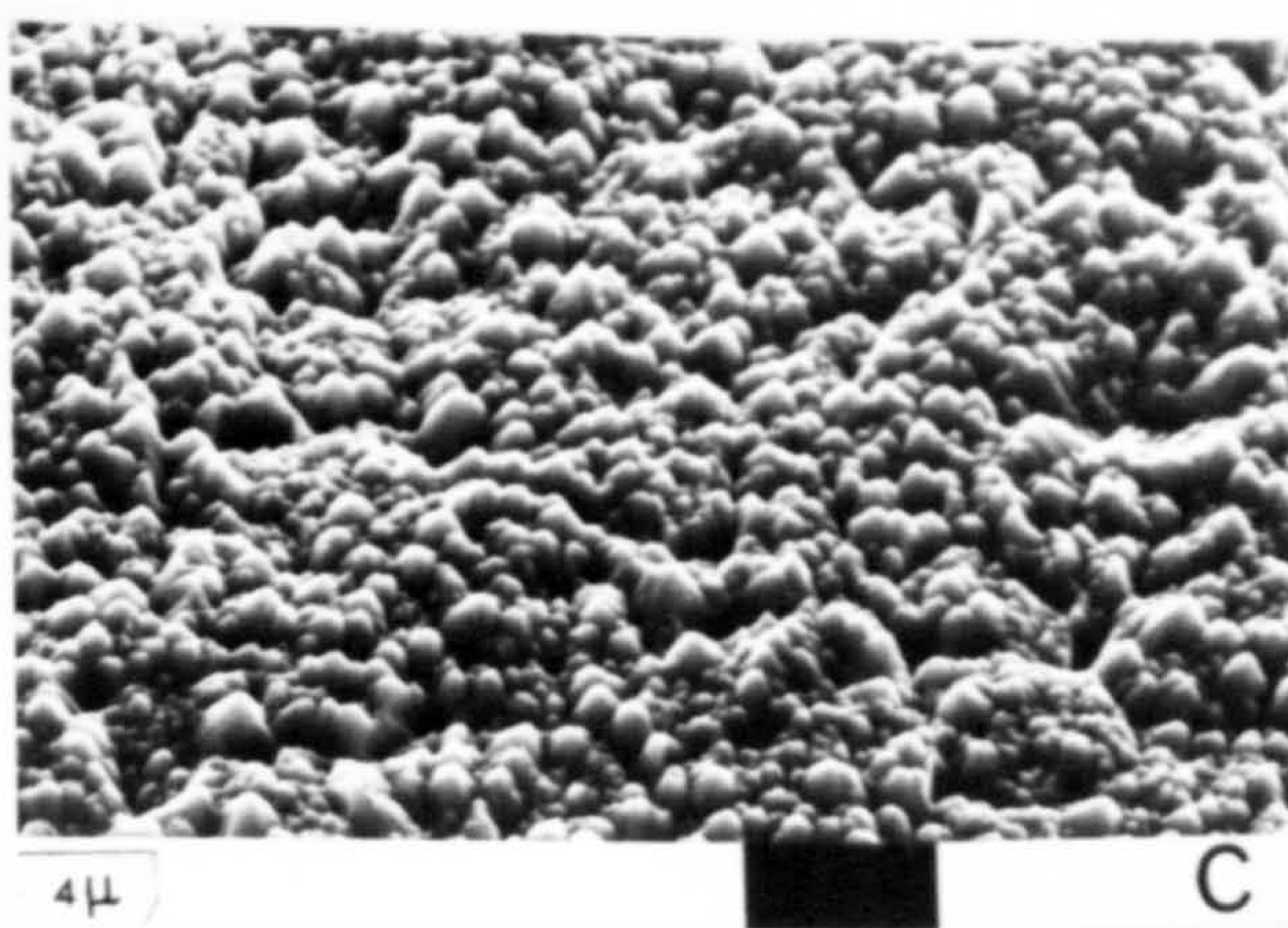
Fig. (5-5) shows some of the relevant micrographs for the top surface of CdS films prepared at two different substrate temperatures using General Electric CdS powder. The grain structure in these films has been revealed by grain boundary decoration. This boundary decoration was provided by first forming Cu_xS on the surface of the CdS film by the CuCl solution process and then removing the Cu_xS layer by dissolving it with KCN [212,219]. The removal of Cu_xS which had formed between the grains reveals the boundaries. From the resultant micrographs in Fig. (5-5) it is clear, that the grain size increases as the substrate temperature increases as has been previously observed by Shallcross [72]. Similar micrographs have been obtained for films produced with lower deposition rates.

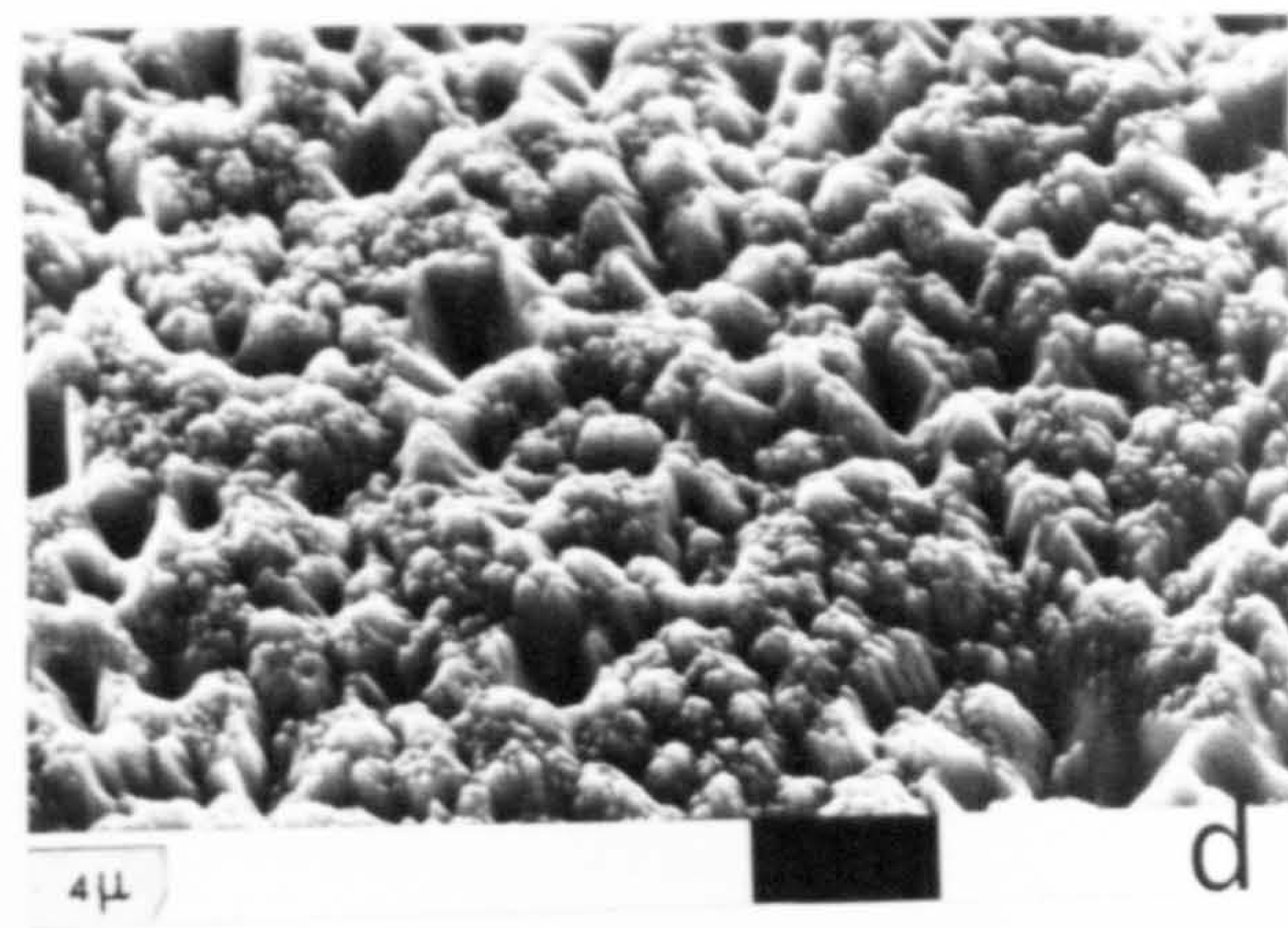
5.1.1.d. Structure and chemical etching

To obtain a highly absorbing surface for the solar cell and to remove surface contamination prior to dipping, the CdS layers are etched in concentrated HCl acid at room temperature. The textured surface which results from etching is advantageous since it acts as a light trap and makes the area of the solar cell junction significantly larger than the geometrical area of the film. Figure (5-6) shows the scanning electron micrographs for CdS films which had been etched in concentrated HCl acid for times of 0, 5, 10, 20 and 30 sec at room temperature. It is clear that as the etching time is increased up to 10 sec, the acid attacks both the grain and the grain boundary regions, yielding a pyramidal structure at the CdS surface with a number of pyramids at the top of each CdS grain. As the etching time is continued beyond 10 sec, some pinholes and etch pits start to develop and increase in width as the etch time









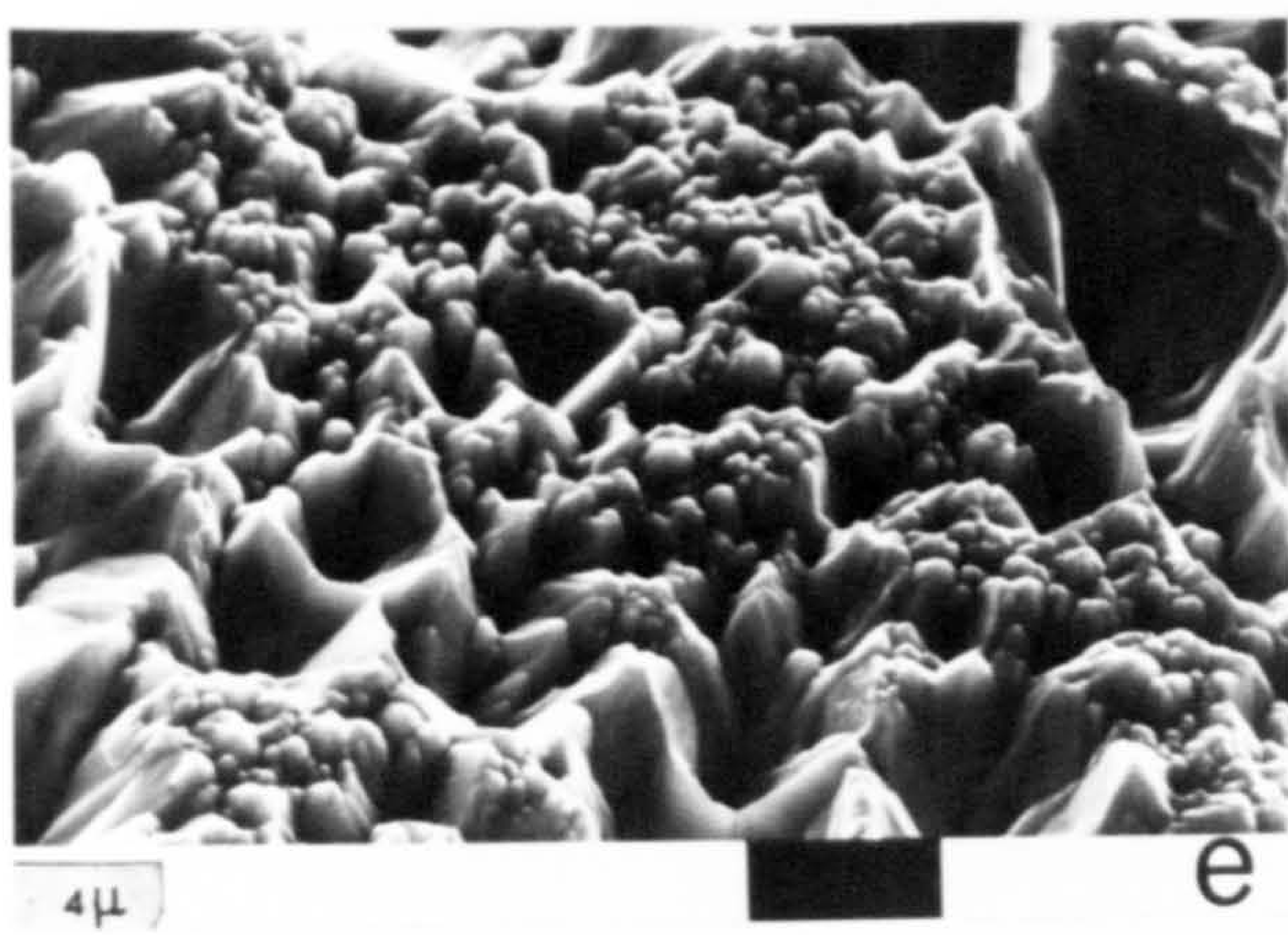


Figure (5-6) SEM micrographs of CdS film after HCl acid etching for (a) 0 sec, (b) 5 sec, (c) 10 sec, (d) 20 sec and (e) 30 sec.

increases. Subsequent studies of the properties of completed cells have indicated that the optimum etching time for high efficiency solar cells is about 5 to 10 seconds.

The effect of the different HCl acid concentrations and temperatures was investigated but such variations were found to provide no advantage over the use of the "as received" concentrated HCl at room temperatures. Brief consideration was given to an alternative method of surface preparation. In this method the CdS film was first dipped in CuCl solution and then the resultant Cu_xS layer was removed with a KCN solution. This procedure increases the effective surface area, primarily by increasing the grain boundary penetration. Although this technique did not lead to the fabrication of solar cells with improved efficiencies as compared with acid etching, it did show that the removal of the top layer of CdS is very important, since the short-circuit current was improved significantly even after a 2 sec preparatory dip. Moreover the stoichiometry of the Cu_xS was also improved, as discussed in section (5.1.2.b).

Besides increasing the effective area, providing a clean, fresh CdS surface and reducing the reflection of the solar cell after the formation of Cu_xS layer, the acid etch may also change the composition of the upper layer of the CdS film, or at least etch away any Cd-rich layer on the surface. Indeed some indication of this behaviour has been obtained from capacitance-voltage measurements. Fig. (5-7) shows the plot of C^{-2} as a function of the reverse voltage for two Schottky diodes of Au-CdS, where the gold dot Schottky contacts were evaporated onto the CdS films before and after the acid etch for 10 sec. As the area increases by a factor of 2.0 after the acid etch (see section 5.1.2.b), then a reduction of the carrier concentration from 6.1×10^{18} cm^{-3} to 5.2×10^{17} cm^{-3} after

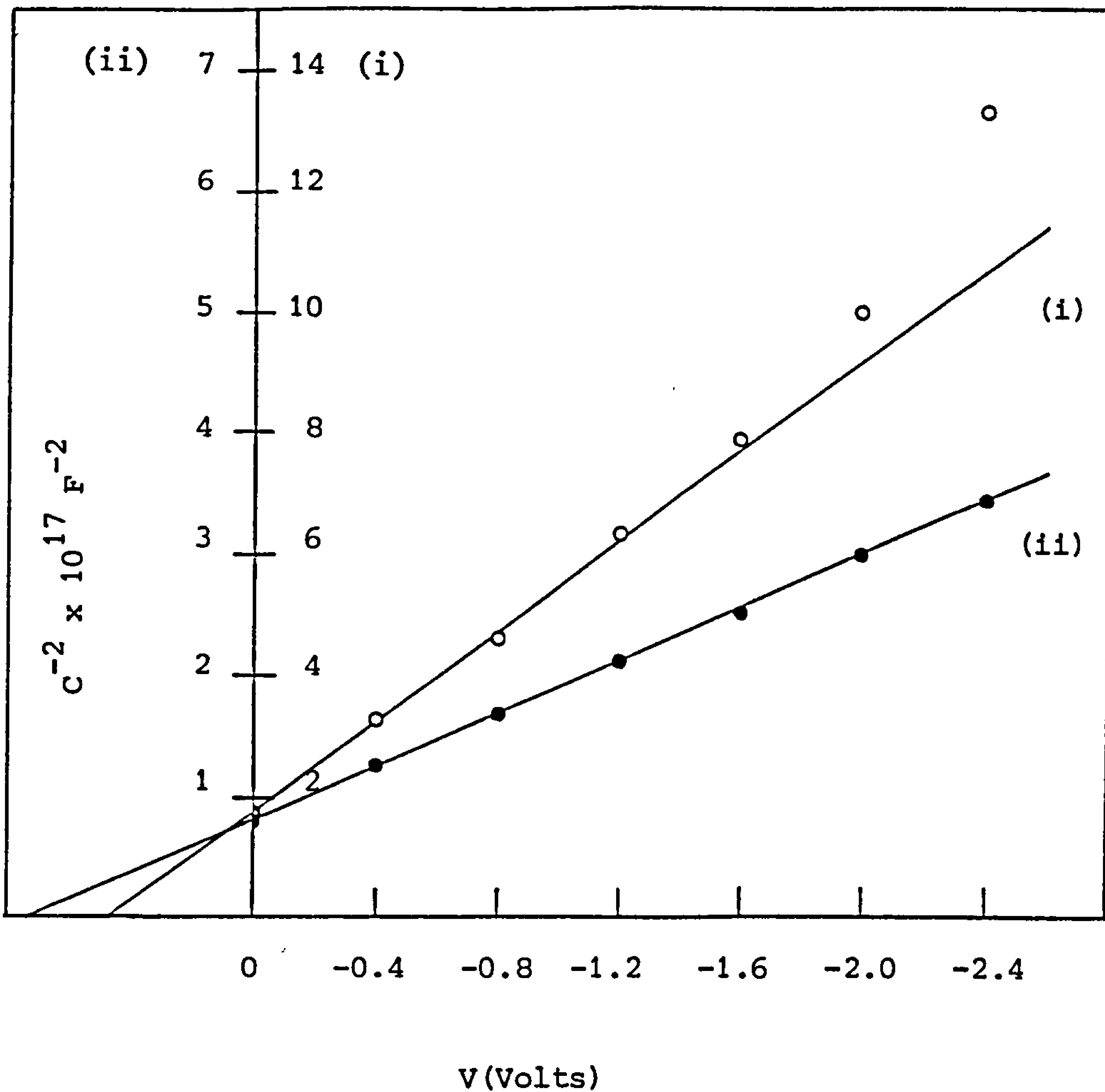


Figure (5-7) C^{-2} as a function of the reverse bias voltages for Au-CdS Schottky diodes, (i) before acid etching and (ii) after 10 sec etched in concentrated HCl acid. (Values of C^{-2} are given on the left side and right side of the ordinate axis for lines (i) and (ii) respectively).

the acid etching is obtained. The associated increase in the space charge width, with the accompanied increase in area is consistent with the capacitance at zero bias.

5.1.2 The Copper Sulphide Layer

5.1.2.a The Thickness and Composition of Cu_xS layer

The dipping of CdS films in a hot CuCl solution for solar cell formation demands high quality CdS films. Since any pinholes or tiny scratches over the film surface exert considerable influence on the process of Cu_xS growth. The microstructure and topography of the CdS films strongly influence the microstructure and topography of the subsequent Cu_xS films. In fact no change was observed in the scanning electron micrographs before and after the formation of Cu_xS and the surface structure of a CdS film with a Cu_xS layer is similar to that for CdS layer.

Auger electron spectroscopy (AES) and electrochemical analysis (ECA) were used to investigate different aspects of the growth behaviour of the Cu_xS films (details are given in chapter 4). To offset any variation in the growth of these films due to differences in the underlying CdS, films of identical structure and electrical properties were chosen. In fact, all the CdS films were deposited with the same evaporation conditions, using sintered Koch light CdS powder, and they were all etched in concentrated HCl acid for 10 seconds. The growth of Cu_xS layers was studied as a function of the CuCl molar concentration in the dipping solution, the dip period and the bath temperatures.

Figure (5-8) shows the variation of the equivalent thickness of the Cu_xS layer as a function of plating time. This thickness is a function of both the mid-grain thickness d_1 and the grain boundary depth d_2

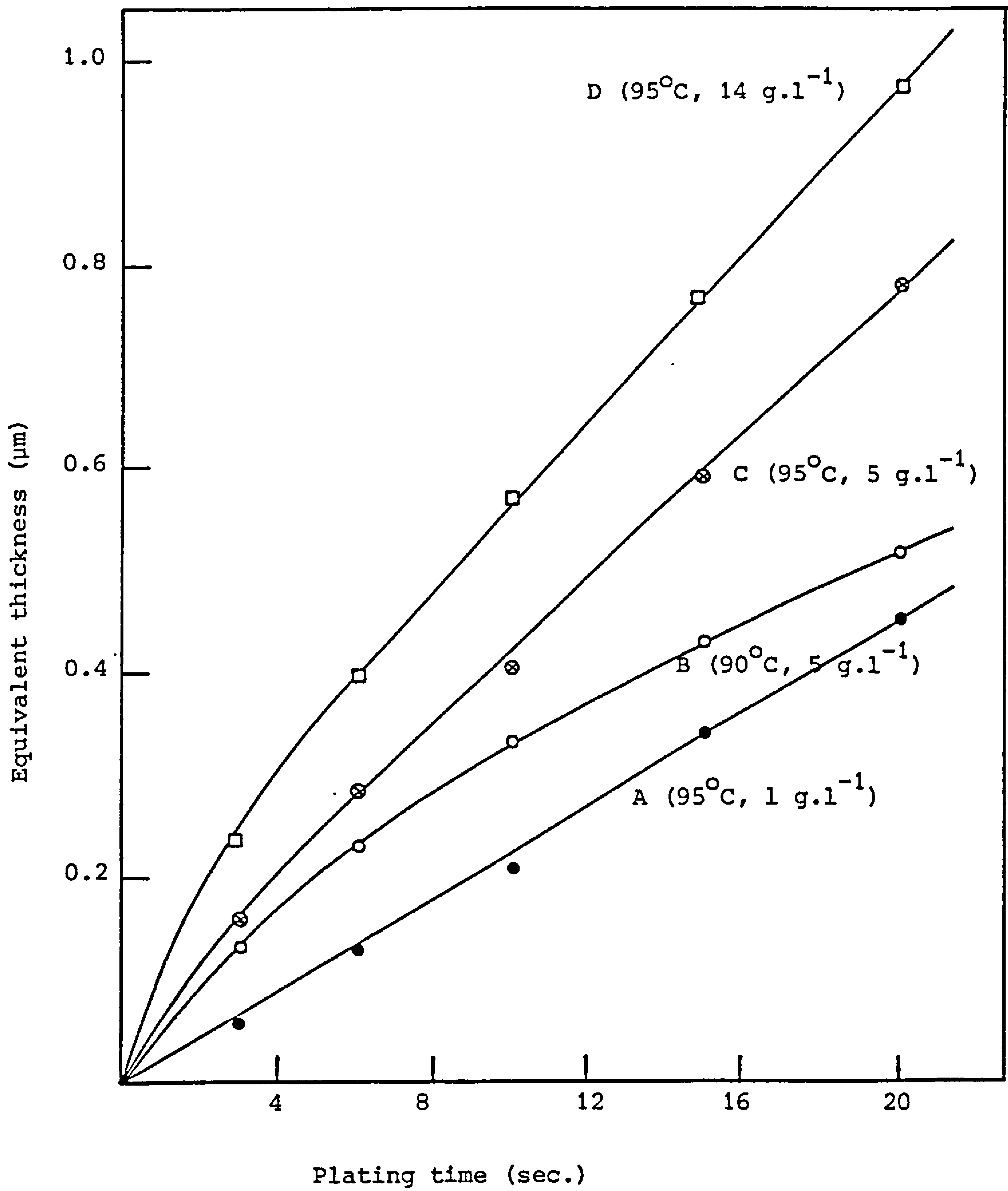


Figure (5-8) Variation of the equivalent thickness of the Copper Sulphide, $\bar{d}$, for different plating parameters as a function of plating time.

of Cu_xS (see Section 5.3.2). Curves A, C and D show these variations for three different CuCl concentrations 1, 5 and 14 g l^{-1} where the solution temperature and pH values were 95°C and 4 respectively. For the lowest CuCl concentration employed (1 g l^{-1}) curve A shows that the growth of the Cu_xS layer is reasonably linear with time, but as the CuCl concentration is increased two growth mechanisms are indicated by the growth curves which follow a parabolic law for small dip times and a linear variation over the longer term. The initial parabolic growth is clearly more significant for higher CuCl concentrations, as seen in curves C and D. When the solution temperature was decreased (Curve B) both of the above two mechanisms could still be observed but, in each case, it appears that the growth proceeds at a slower rate. These results are in good agreement with Salkalachen et al. [125] for plating solutions with a PH value of more than 4. Palz et al. [206], Lindquist and Bube [207] and Rothwarf [208] have attributed a linear growth to the penetration of the solution into the cracks and numerous grain boundaries in the CdS films. Baron et al. [133] have suggested that a paraabolic type of growth is restricted to the central region of the grains. This is consistent with results obtained on single-crystal CdS by Singer and Faeth [209] and Buckley and Woods, [210] who found that the growth of Cu_xS layers followed a parabolic law attributed to diffusion limited growth on the CdS surface. These observations were made for fairly large thicknesses of copper sulphide layers.

The composition of the as-dipped chemiplated layers are non-stoichiometric to varying degrees immediately after formation. The measurements in Figure (5-9) show the composition of the copper sulphide layers as functions of plating time. The values of x in the Cu_xS increases as plating time increases. It is clear that, for very thin layers of Cu_xS, the value of x is very low (curve A). This may be partly

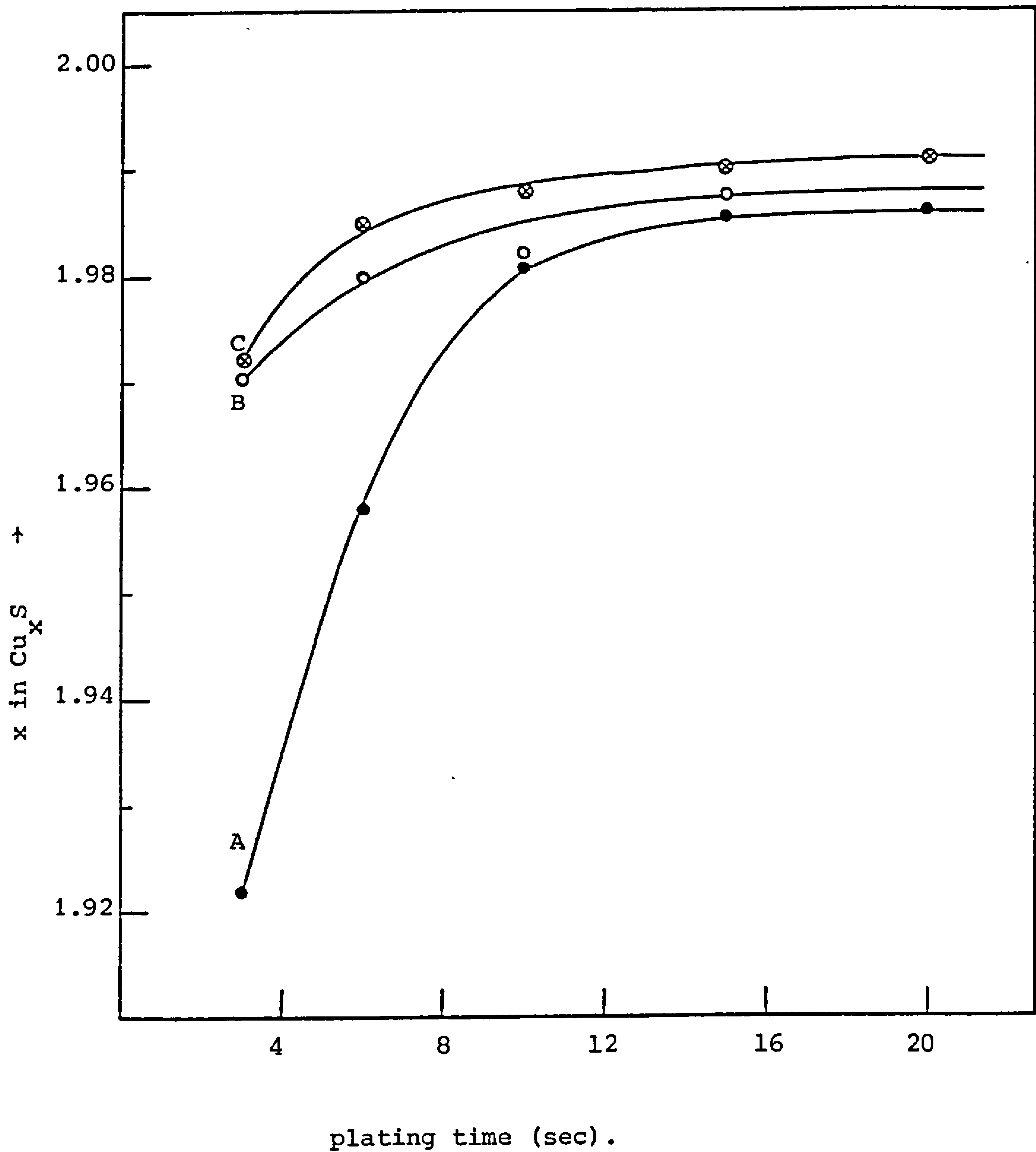


Figure (5-9) Composition of the Copper Sulphide, x, as a function of plating time for different plating parameters. Point symbols as in figure (5-8).

because the composition of the Cu_xS layers is affected by the laboratory atmosphere during transfer to the measurement system. The upper surface of the Cu_xS layer tends to become oxidized, while the under layer is less affected. However, it should be emphasised that all the measurements were taken immediately after the chemiplating process in order to minimize the time for oxidation.

It is significant that a higher CuCl concentration seems to have a positive influence in improving the stoichiometry of the layer. At 5 g l^{-1} the values of x in the Cu_xS layers are considerably increased as compared with lower CuCl concentrations (Curves A and C). Also the composition of the Cu_xS layer was improved as the CuCl solution temperature was increased, as is clearly shown in Figure (5-9) by comparing curves B and C. As the use of 14 g l^{-1} CuCl concentration requires only a very short dipping time for the required thickness of the Cu_xS layer to be formed it was found that greater control was achieved by use of a weaker solution. Therefore (unless stated otherwise) the following standard dipping conditions were used throughout the remainder of the reported work:

Plating solution - 5 g l^{-1} CuCl, 13 ml l^{-1} HCl, 11 ml l^{-1} hydrazine, pH = 4 (adjusted with HCl or hydrazine)

Solution temperature = 95°C

Plating time = 5-6 sec.

5.1.2.b <u>The effect of chemical etching</u>

In addition to its effect on the texture of the CdS surface, the chemical etching ofthe CdS films was found to affect the stoichiometry of the Cu_xS layer subsequently formed by dipping in CuCl solution. Table (5-5) shows that both the acid etch and the KCN treatment improves the stoichiometry of the Cu_xS layers.

TABLE (5-5). Copper sulphide stoichiometry and equivalent thickness changes due to different chemical etching of CdS films.

	x	$\bar{d}$	oxide %
A - unetched	1.9507	2051	1.14
B - KCN	1.9747	2175	0.9
C - "	1.9826	2598	1.1
D - "	1.9721	2791	1.65
E - HCl	1.9721	4076	0.838

In sample A, the Cu_xS layer was formed on the "as made" CdS layer, while the CdS film in sample E was given a 10 sec etch in concentrated HCl acid. For samples B, C and D the CdS layers were first dipped in CuCl solution for 2, 5 and 12 sec respectively, and the resultant Cu_xS layers were then removed using KCN solution. Cu_xS layers were once again formed on these samples using the same standard dipping procedure as for samples A and E. It should be noted that the thickness of the Cu_xS film quoted in table (5-5) is the equivalent thickness ($\bar{d}$) for which the surface area of the Cu_xS layer is taken as equal to the geometrical area of the exposed layer (see section 4-10). Therefore the results in table (5-5) reflect the increases of surface area and junction area as a result of the different surface preparation processes. If we assume the thickness and the growth mechanism of the Cu_xS layer are the same during the final dipping process for all the samples in table (5-5), the values of $\bar{d}$ indicate that there is an increase in the surface area of the CdS and, consequentially, of the junction area of the cell as a result of the etching process. This factor is approximately equal to 2 in the case of the HCl acid etch as shown by sample E (table 5-5) and, as

expected, increases steadily with increase in pre-dipping time for samples B, C and D.

5.1.2.c. The influence of different annealing conditions

As electrochemical analysis (ECA) is a destructive technique it is not possible to perform an electrical characterisation and a Cu_xS layer stoichiometry determination on a particular sample subjected to a variety of annealing treatments. However, in order to be able to correlate such data, the samples under investigation were taken from the same batch of CdS layers and processed together prior to the respective measurements being made.

The influence of annealing in air is demonstrated in table (5-6), which shows how the sheet resistance, the amount of oxide and the stoichiometry of the Cu_xS varies with annealing time. The results show

TABLE (5-6). Copper Sulphide stoichiometry (Cu_xS) and sheet resistance changes due to annealing in air.

Annealing time (mins.)	x	Oxide %	sheet resistance ($10^2\ \Omega$)
0	1.966	0.011	12.0
2	1.964	0.011	-
5	1.954	0.012	-
10	1.912	0.017	8.5
20	1.89	0.05	5.7

very clearly the deterioration in the stoichiometry of the copper sulphide as the annealing time increases and oxidation proceeds.

An improvement, rather than a deterioration, in the x-parameter is obtained by annealing in a vacuum or in flowing hydrogen,as can be seen

in table (5-7) which shows the effect of 20 mins. annealing in one of the three different ambient atmospheres. It is clear that while oxide formation is a significant effect in the case of air annealing, there is some reduction of the existing oxide layer in the case of vacuum or hydrogen annealing, together with the improvement in x values.

TABLE (5-7). Copper sulphide stoichiometry (Cu_xS) and oxide percentage changes due to 20 mins. annealing at 200°C for different annealing ambient atmospheres.

Annealing ambient	x	oxide %
-	1.966	0.011
Air	1.940	0.05
Vacuum	1.976	0.006
Hydrogen	1.979	0.003

As the copper vacancies which are produced in the copper sulphide layer (as a result of surface oxidation) act as acceptor centres, the departure of x from the value 2 causes an increase in the majority carrier density with a consequent reduction in the sheet resistivity of the copper sulphide layer. This is also seen from the data in Table (5-6). This well-known association between the sheet resistance of the Cu_xS layer and the composition parameter x is further demonstrated in figure (5-10), which also shows that the highest values of both sheet resistance and x are obtained by annealing in vacuum or in hydrogen.

The advantage of using a vacuum or a hydrogen atmosphere during the annealing stage is undoubtedly due to the avoidance of oxide formation

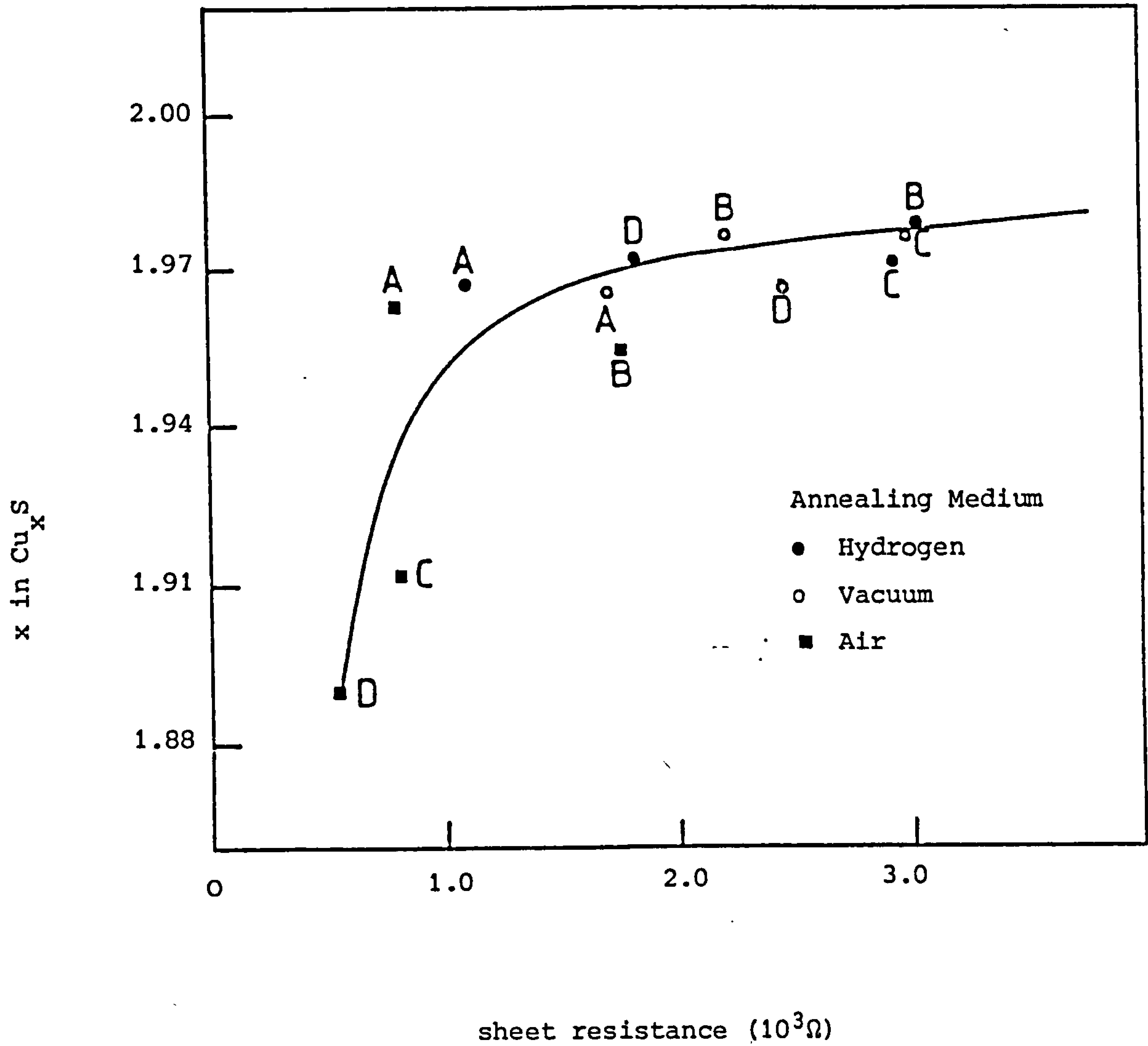


Figure (5-10) variation of the composition parameter x in Cu_xS with the sheet resistance of the Cu_xS layers. Points labelled A, B, C and D are for annealing times of 2 mins. 10 mins. and 20 mins. respectively.

with its consequent lowering of the x value in the Cu_xS phase at the surface of the cell. As Table (5-7) shows that a reduction of the oxide is possible, with an improvement in the x-parameter, it was anticipated that longer annealing times (particularly in hydrogen) would be beneficial. This has indeed been confirmed by examining the effects of annealing at different temperatures for up to 8 hours. The best value of the Cu_xS stoichiometry (x = 1.9927) close to optimum value for high efficiency CdS-Cu_xS solar cells was obtained when the Cu_xS layer was annealed under flowing hydrogen for 8 hours at 200°C. This finding is in a good agreement with the work at the Institute of Energy Conversion in Delaware.

5.1.2.d. The effect of copper overlayers

As discussed in section (5.2.4), an alternative method for avoiding a deterioration in the stoichiometry of the Cu_xS layer during the annealing stage is to provide an overlayer of copper. Subsequent annealing (in air) not only improves the stoichiometry but also the stability of these cells.

The effect of an additional copper layer (in this case 100 Å) and air annealing for up to 3 hours can be seen in Table (5-8). This lists the x values and oxide percentages of the Cu_xS layers before and after applying the Cu layer, and following air annealing at 200°C. It is clear that, in the presence of the copper overlayer, the first 90 mins. of annealing time allows the stoichiometry of the Cu_xS layers to be improved while at the same time a surface oxide layer is being generated.

If a Cu_xS layer coated with a thin layer of Cu is annealed in vacumm no significant improvement of the Cu_xS stoichiometry is obtained and the Cu layer remains largely unaffected. Therefore, to enhance the reaction between the Cu layer and the Cu_xS, the annealing of this system

TABLE (5-8). Composition parameter x in Cu_xS and oxide percentages of Cu_xS before and after applying copper over layer (~100 Å) and subsequent annealing treatment in air.

	x	oxide %
As-dipped	1.965	0.01
+ 100 Å Cu layer	1.951	0.02
20 mins. air annealing	1.981	0.10
40 mins. air annealing	1.985	0.17
90 mins. air annealing	1.988	0.2
180 mins. air annealing	1.980	0.21

must be done in air. Indeed a value of x as high as 1.992 was obtained for some samples as a result of this treatment. As previously noted, such a value can be obtained by the use of hydrogen annealing but only after many hours of annealing time. There is clearly an advantage for the copper overlayer treatment which requires a shorter annealing time and, at the same time, improves the stability of the cell (see section 5-4).

5.1.3. Properties of the top contact

In a front-wall solar cell the grid design must be a compromise between the current collection efficiency and the transmission of the incident light onto the Cu_xS surface. In the early stages of this investigation, the completed cells had a high series resistance and a low fill-factor when using a grid with up to 4 lines cm^{-1}. The grids were either of silver paste and printed onto the Cu_xS surface or vacuum evaporated gold through a mask. Because the copper sulphide layer is very thin its sheet resistance is high and, in order to minimise the series

resistance of the cell, the current conducting paths must be kept very short. Hence, a close-spaced grid structure is found to be essential. However, since the incident light must be transmitted through the spaces between the grid lines, the grid lines have to be proportionally narrow. With an improved grid design providing 16 lines cm^{-1}, improvements in the short-circuit current, the series resistance, the fill-factor and consequently the conversion efficiency of the cells have been obtained. Table (5-9) compares the effect of two different grid designs on some cell parameters and shows that the grid can have a significant influence on the overall efficiency which can be achieved. Apart from their grids, the cells compared in table (5-9) were almost identical, both having a Cu_xS layer with x value of 1.98 and Cu_xS real layer thickness approximately 0.2 μm. It must be noted that by using x values smaller than 1.96 fill-factors as high as 0.75 have been obtained, but the short-circuit current was then very small due to the reduced photon absorption coefficient.

TABLE (5-9). V_{oc}, J_{sc}, FF and η of two identical cells having different gold grids design.

	V_{oc} (Volts)	J_{sc} mA cm^2	FF	η%
4 lines cm^{-1}	0.51	15.7	0.51	4.08
16 lines cm^{-1}	0.51	18.5	0.7	6.60

In addition to the density of grid lines, the series resistance of the cell and also the fill-factor are influenced by the grid material, line thickness and line width. In order to have grid lines with sufficiently low resistance, a line thickness over 0.5 μm was found to be necessary. Obviously, the grids must be made from metals which form a good ohmic

contact with the copper sulphide layer. Grids made from evaporated silver metal were found to be unsuccessful, since the open circuit voltage, V_{OC}, was significantly reduced (in some cells it was as low as 0.32 volts). More satisfactory grids were obtained using evaporated copper metal, but much better and more reproducible results were obtained from gold evaporated grid contacts.

5.2 Characteristics and properties of the CdS-Cu_xS solar cells

5.2.1. The effect of CdS properties

Figure (5-11) shows typical I-V characteristics for CdS-Cu_xS solar cells made from CdS films with different resistivities. Before annealing, the cell made from low resistivity CdS film (Curve A) had poor diode and photvoltaic characteristics, i.e. the current voltage relationship was almost ohmic, the open-circuit voltage and the fill-factor were low, and the dark saturation current was high. The photovoltaic effect shows improvement after the annealing treatment, but the open-circuit voltage always remains below the normally-achieved standard value (~ 0.5 V). Better output was obtained immediately after the dipping process when the resistivity of the CdS was increased, and the open circuit voltages were then found to reach the above standard value of this device. As seen in figure (5-11) the annealing treatment improves the photovoltaic properties (curve C and D), but the series resistance and the fill-factor were found to be rather poor in the case of CdS films with electrical resistivity higher than 500 Ω cm (curve C). The rather low short-circuit current for the cell formed in high conductivity CdS (curve B) is undoubtedly due partly to the stoichiometry of the Cu_xS, which was found to degrade more rapidly for Cu_xS layers made from low resistivity CdS (see

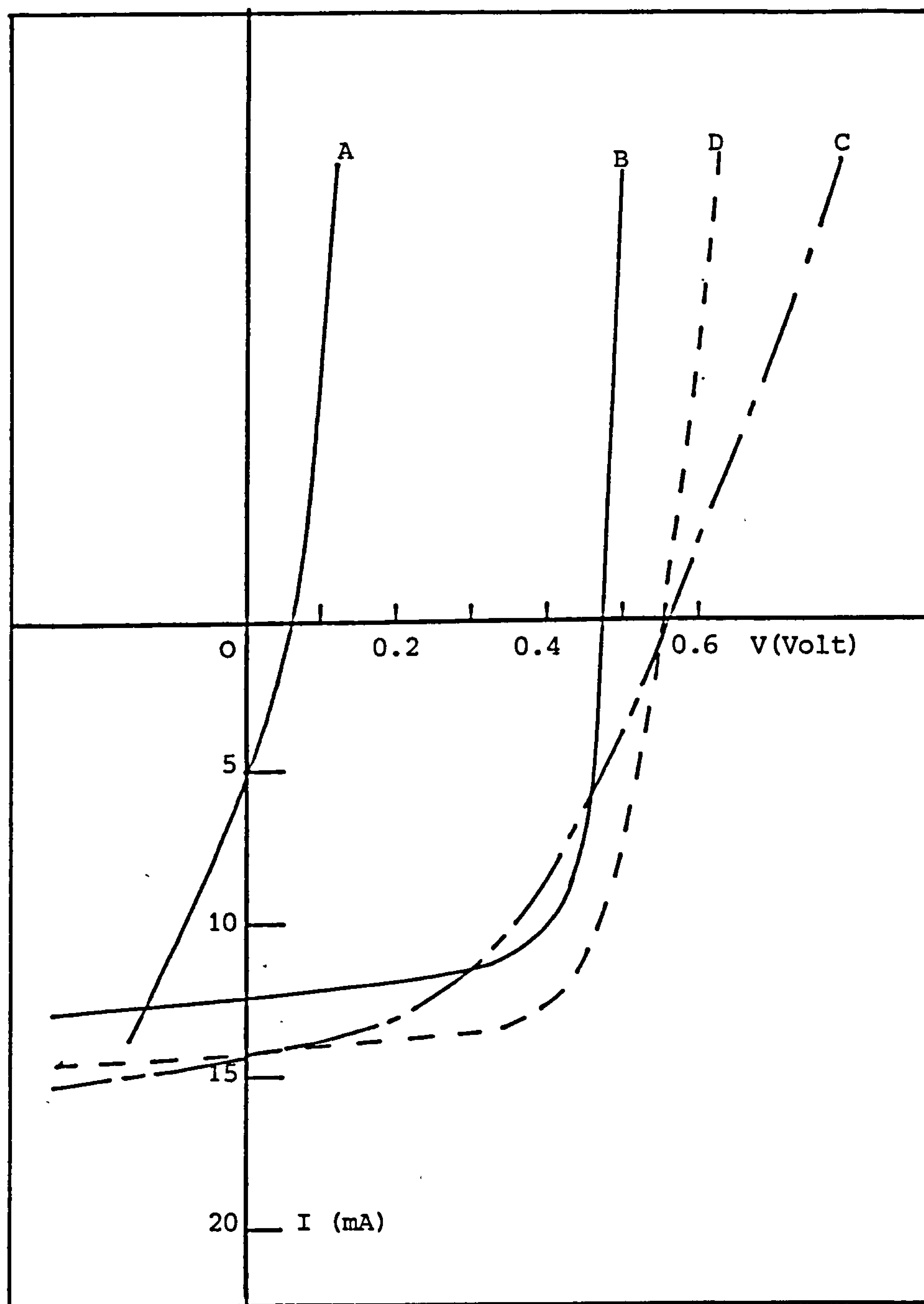


Figure (5-11) I-V characteristics of $CdS-Cu_xS$ Solar cells. The electrical resistivity of Cells A, C and D are 0.1, 42 and 700 Ω cm respectively. Curves B , C and D are taken after 20 mins. hydrogen annealing treatment at 200°C.

section 5-4).

An investigation of the effect of etching the CdS surface prior to dipping showed that improvements of the cell efficiency are obtained after HCl etching for 5-10 sec. Typical results are shown in table (5-10).

TABLE (5-10). V_{oc}, and I_{sc} changes due to different etching time of the CdS layer.

HCl	V_{oc} (V)	J_{sc} mA cm^{-2}
unetched	0.52	10.2
2 sec. etch	0.515	13.7
5 sec. etch	0.5	16.7
10 sec. etch	0.5	17.0
20 sec. etch	0.49	15.4

These results were obtained using relatively high resistivity CdS films (500 Ωcm). The etched films were formed into cells using the standard dipping procedure (summarised in section 5.1.2.a) and post-fabrication annealing was carried out in hydrogen for 20 mins. at 200°C. The fall in the open-circuit voltage with increased etching time (table 5-10) can be attributed to the increase in the area of the actual heterojunction, A_J, according to the following relation [47]

$$\Delta V_{oc} = \frac{kT}{e} \ln \frac{A_J}{A_\perp} \qquad (5\text{-}1)$$

where $A_\perp$ is the projected area of the cell. From the data in table (5-10) the ratio $\frac{A_J}{A_\perp}$ was found to be 2.16 for a 5-10 sec HCl etch which fits well with the data in section (5.1.2.b). In order to improve the V_{oc}, the ratio of $\frac{A_J}{A_\perp}$ must be close to one. By using a weak HCl etch (20%) the unwanted surface contaminated layer of the CdS can be removed without severe surface texturing. It has been found that this does avoid the

reduction in V_{oc} values but, as expected, the short-circuit current and the efficiency are always lower than that for a highly textured surface. The importance of the acid-texturing is demonstrated by comparing table (5-10) with results in table (5-11) which were obtained using films which had been given the KCN treatment. The CdS films were first dipped in CuCl solution for 2, 6, 8, 12, and 20 sec. The copper sulphide was then removed by KCN and the devices were then redipped in CuCl for 5-6 sec and finally annealed in air for 5 mins. at 200°C. These results show, once again, that the V_{oc} falls as the effective area of the junction, A_J, is increased (in this case due to increased grain boundary penetration of the Cu_xS layer) but for these cells there is no significant improvement in the short-circuit current, presumably due to the relative smoothness of the cell surface and the consequent poor photon absorption properties of the Cu_xS layer.

TABLE (5-11). V_{oc} and J_{sc} changes due to different KCN etching time. Note that the predipped Cu_xS are annealed in air at 200°C for 5 mins.

First dip time (sec)	V_{oc} (Volts)	J_{sc} (mA cm^{-2})
2	0.5	10.25
6	0.5	12.8
8	0.49	
12	0.48	9.68
20	0.46	8.5
HCl acid etch (5 sec)	0.49	14.8

5.2.2. The influence of the copper sulphide layer

As discussed in section (5.1.2.a) the required Cu_xS stoichiometry can be achieved by appropriate control of the CuCl solution temperature, and concentration. However, the photovoltaic properties of the completed cell depend markedly on the thickness of the Cu_xS layer as well as on the stoichiometry.

Table (5-12) shows how the thickness of the Cu_xS (determined by the plating time) affects several cell properties. The cells were fabricated using 35 μm thick CdS films which had been etched in a concentrated hydrochloric acid at room temperature for 10 sec. The films were dipped in CuCl solution for 3, 6, 10, 15 and 20 seconds using the standard CuCl solution (see section 5.1.2.a). Prior to deposition of gold grids (16 lines cm^{-1}) the cells were annealed in vacuum for 20 mins. at 200°C. Table (5-12), shows that the open-circuit voltage decreased as the plating time increased as would be expected from the deeper penetration of the Cu_xS through the grain boundaries of the CdS causing an increase in the junction area. The calculated increase in junction area (using eq. 5-1) is shown in figure (5-12). This deep penetration of the Cu_xS is also responsible for the low value of the fill-factor at 20 mins. plating time.

As the Cu_xS is responsible for the absorption of the major portion of the light, its optimum thickness is a compromise between the need to make it as large as possible to maximize light absorption and the opposing requirement that the thickness should not exceed a value related to the diffusion length of the Cu_xS minority carriers (electrons). Therefore, in spite of the improvement of the Cu_xS stoichiometry as the plating time is increased the short-circuit current is seen to reach a maximum value after approximately 6 seconds plating time, which corresponds to copper sulphide equivalent thickness of about 0.28 μm (real layer

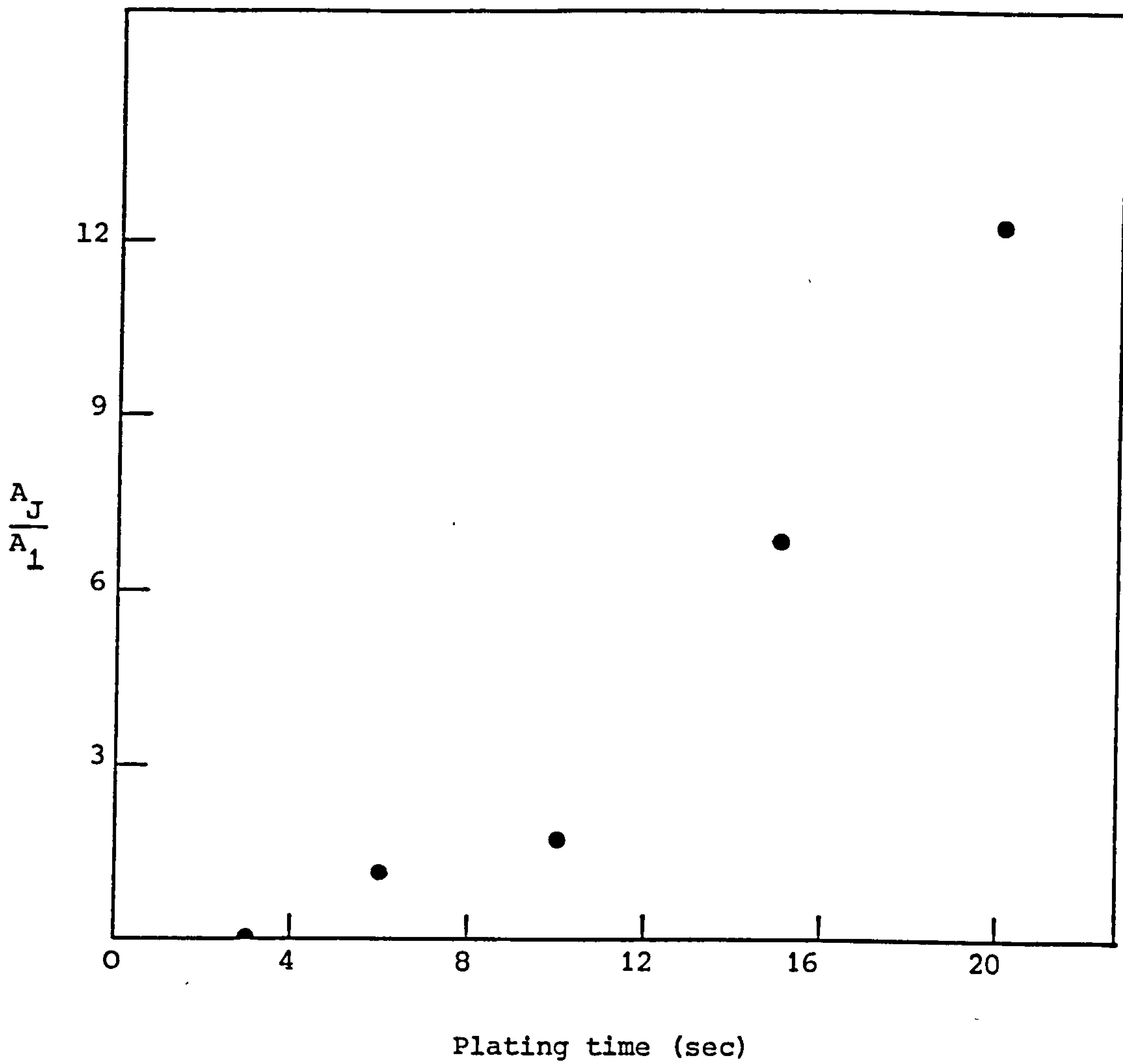


Figure (5-12) Calculated $\frac{A_J}{A_1}$ values as a function of plating time.

thickness of ~ 0.12 μm).

The effect of the Cu_xS thickness on the electrical properties has been investigated using a variety of CdS films with different electrical properties. These have been processed in a variety of CuCl solutions with different CuCl concentrations and solution temperatures. For cells which were given the same post-fabrication annealing conditions the optimum real layer thickness of the Cu_xS for the best efficiency cells was always in the range 0.10-0.2 μm. For this thickness the short-circuit current is found to increase with higher values of x as shown in figure (5-13) for cells under AMI light intensity. In the presence of a djurleite-digenite mixture ($1.96 > x > 1.89$), the short-circuit current is only slightly sensitive to the x-value. However as x increases above 1.96, the short-circuit current increases very rapidly and reaches its maximum values when x is very close to 2. These results are in a good agreement with Palz et al. [109,137].

TABLE (5-12). Cell parameters as a function of plating time.

plating time (sec)	$\bar{d}$ (A^o)	x	J_{sc} (mA cm^{-2})	V_{oc} (volts)	FF	η %
3	1590	1.9	10.87	0.525	0.735	4.2
6	2840	1.976	15.71	0.52	0.7	5.71
10	4040	1.977	13.42	0.51	0.692	4.73
15	4900	1.983	12.04	0.475	0.673	3.84
20	7810	1.986	9.75	0.46	0.535	2.4

5.2.3. The effect of different annealing conditions

The influence of annealing in one of three different ambient atmospheres is demonstrated in figure (5-14) which shows how the open-

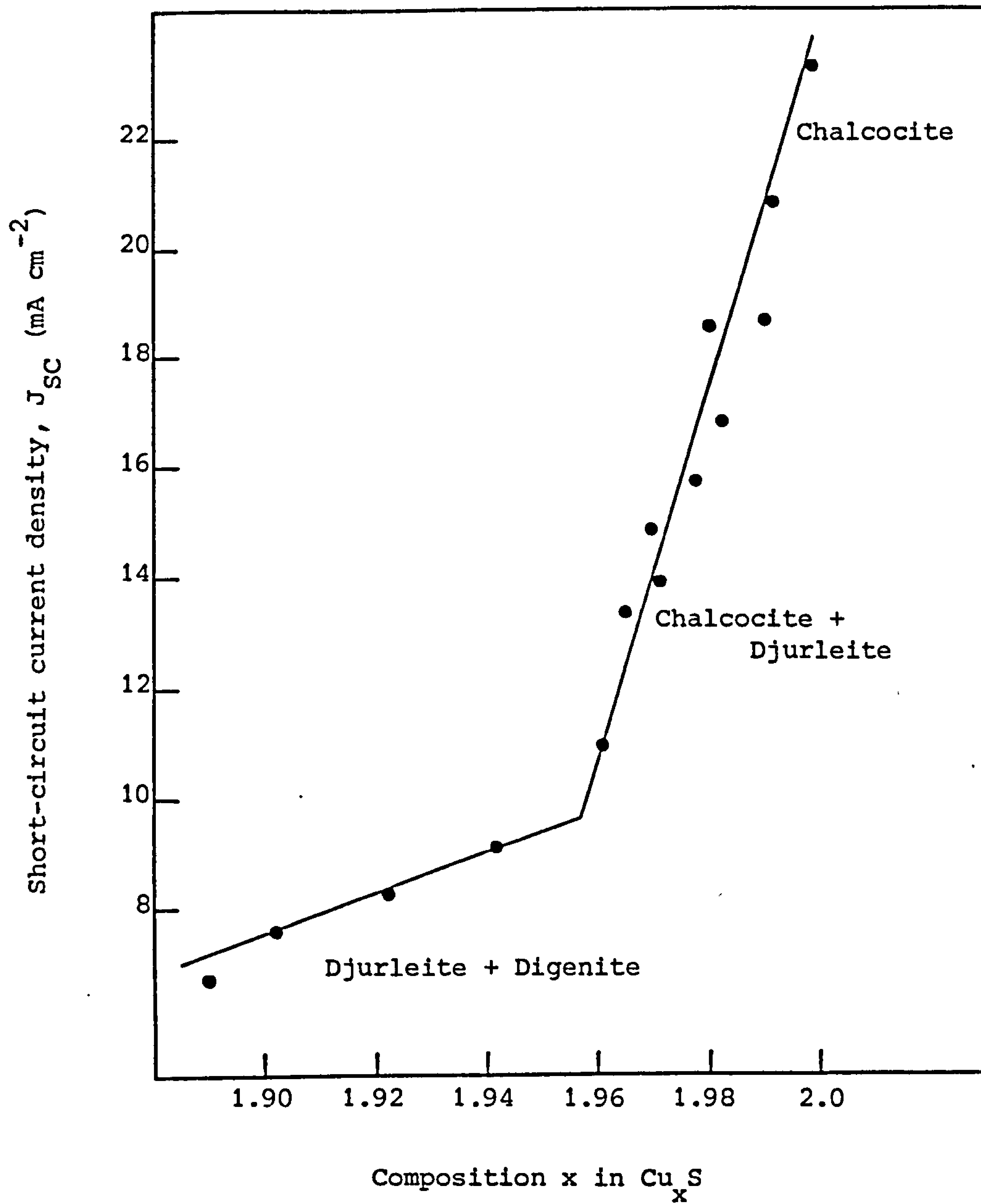


Figure (5-13) Short-circuit current of CdS-Cu_xS Solar Cell as a function of x parameter in Cu_xS.

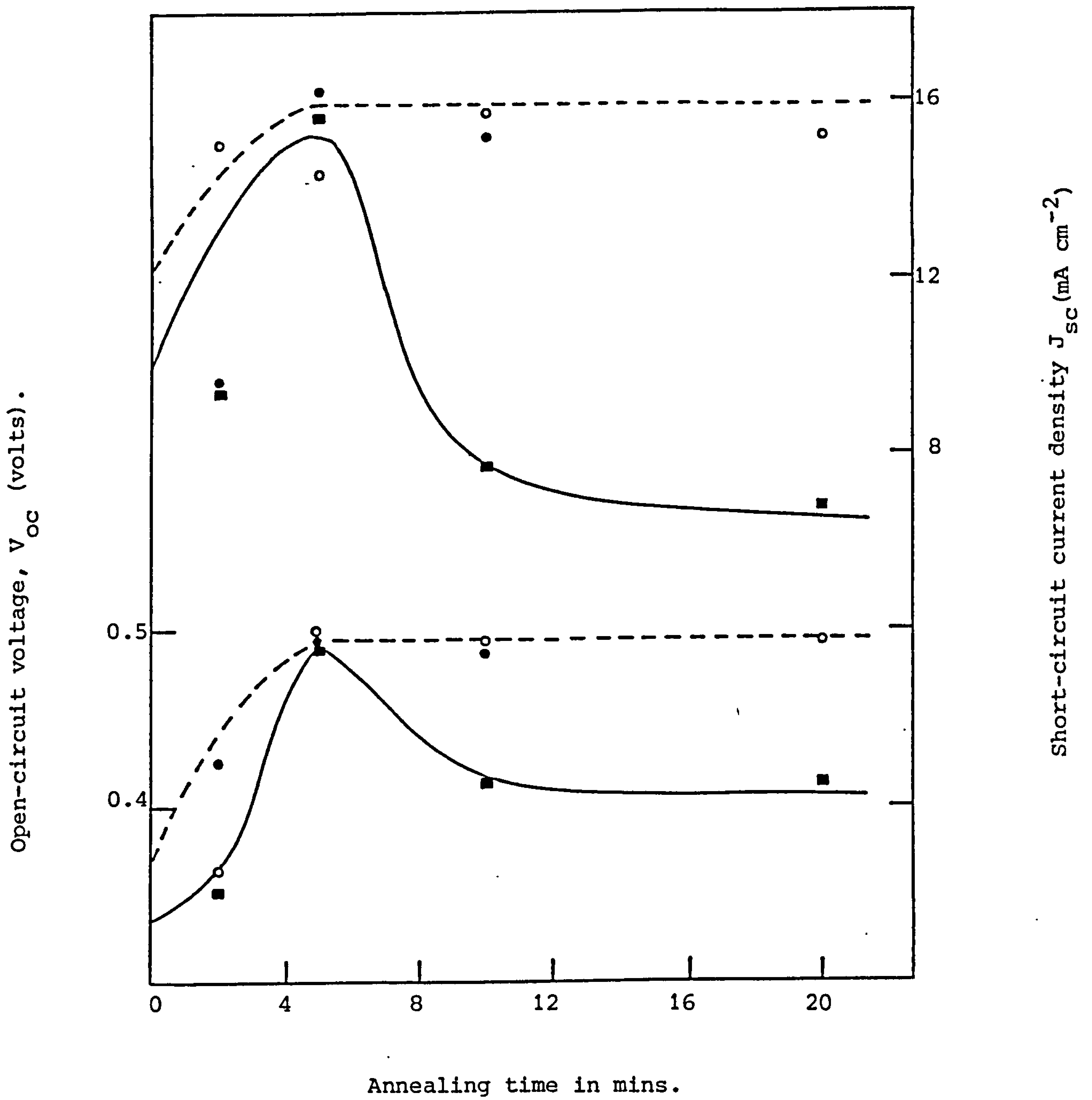


Figure (5-14) The open-circuit voltage, V_{oc}, and the short-circuit current, J_{sc}, as function of annealing time in air (■), vacuum(o) and hydrogen (●). The full curves refer to anneals in air and the broken curves for anneals in vacuum or hydrogen.

circuit voltage, V_{oc} and the short-circuit current, J_{sc}, both vary with annealing time. In every case there is an improvement in V_{oc} and J_{sc} for very short annealing times, but while further heat treatment in air gives rise to a subsequent deterioration in these electrical characteristics (full curves in figure 5-14) no such deterioration occurs with further annealing in either vacuum or hydrogen (broken curves in figure 5-14). Thus, although there is a clear optimum time for annealing in air (in the region of 5 mins. for the case shown in figure 5-14) no such optimum time can be associated with annealing in either a vacuum or a hydrogen atmosphere. Indeed, very much longer periods of hydrogen annealing have been employed with no sign of deterioration of the cells. During the course of this investigation some cells were heated for up to 10 h and in other laboratories annealing in hydrogen for periods up to 64 h (at the slightly lower temperature of 150°C) has been successfully employed [211,212]. During this project, the best recorded value of the short-circuit current (23.2 mA cm^{-2} at AM1 as shown in figure 5-13) was obtained after 8 hours annealing in flowing hydrogen at 200°C. This high value for J_{sc} was undoubtedly due to the corresponding improvement in the Cu_xS stoichiometry with the x value (x = 1.9927) similarly being the highest recorded value obtained during this work, as seen in figure 5-13. As discussed previously (section 5.1.2.c), cells exposed to air suffer oxidation with a corresponding fall in the Cu content of the Cu_xS phase and resultant deterioration of the electrical characteristics. Annealing in a vacuum or in hydrogen atmosphere is expected to reverse this process to some extent and this was confirmed by spectral response measurements, an example of which is shown in figure (5-15). In order to make clear the changes which occur under different ambient conditions, the effect of a long (20 days) exposure to air is compared here to the effect of subsequent

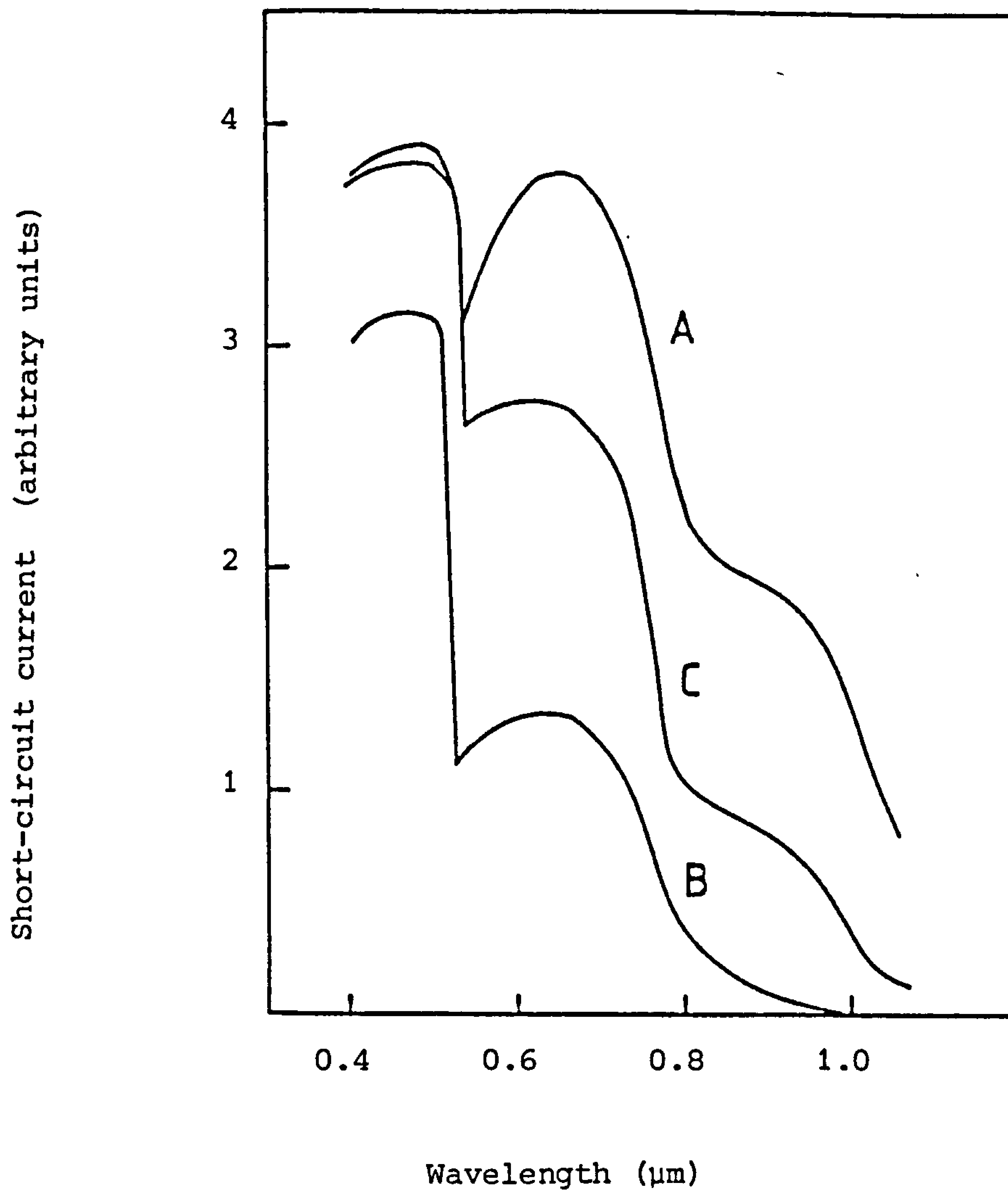


Figure (5-15) The spectral dependance of the short-circuit current (corrected for variations in the incident photon flux) for a freshly prepared cell (curve A), the same cell after exposure to air for 20 days (curve B) and the air-exposed cell after annealing at 200°C in vacuum for 30 mins. (curve C).

annealing in vacuum for a slightly longer period (30 mins.) than was employed for the samples in figures (5-10) and (5-14). The spectral responses show three main features - two broad maxima at approximately 0.9 μm and 0.7 μm and a sharp edge at 0.5 μm. The long wavelength maximum is due to absorption by chalcocite which has a smaller band gap (~ 1.2 eV) than that of djurleite (1.8 eV) [213]. Absorption by the latter phase contributes to the maximum in the region of 0.7 μm and the feature at 0.5 μm is due to absorption in CdS. Accordingly, as has been clearly demonstrated using single-crystal cells [213], the relatively greater fall in the long wavelength photoresponse compared with the fall in the 0.7 μm response (curves A & B figure 5-15) is a consequence of an undesirable reduction in the value of the composition parameter x due to the effect of oxygen. However, some recovery of the long wavelength response of this cell was obtained by annealing in vacuum, as is clearly shown in curve C.

5.2.4. Effect of copper overlayers

The beneficial effect of applying an overlayer of copper to a Cu_xS/CdS cell has been discussed previously (section 5.1.2.d). However, as the various cell fabrication conditions for optimum device performance are very much interrelated, it was necessary first of all to determine the effect of different thicknesses of copper and of different annealing times on the properties of cells produced by an adaptation of the standard procedure summarised in section (5.1.2.a). For this purpose, after the CuCl dipping stage, the cells were placed in the vacuum evaporation unit and a thin layer of copper was deposited over the Cu_xS surface to a thickness measured by a quartz crystal monitor. The cells were then completed with the usual linear array of gold contacts evaporated onto the

surface through a mask. The results of this experiment for copper thicknesses in the range 0-200 Å are presented in table (5-13). With no heat-treatment, it is clear that deposition of copper had an expected adverse effect on the electrical properties of the cells. However, during the following 3 h annealing treatment at 200°C in air an interesting variety of behaviour was observed. The cell with no copper layer degraded rapidly, as expected, while the copper-covered cells all displayed steadily improving (but copper-thickness dependent) characteristics for the first 90 mins., after which degradation ensued.

This experiment in which the best result was achieved for the sample with a 100 Å thick layer of copper after 90 mins. heat treatment is consistent with the work of Bloss and Hewig [214] who obtained optimum cell characteristics with copper layer thicknesses in the range 50-100 Å. The full I-V characteristics for the cell with 100 Å copper layer are shown in Figure (5-16) for annealing times of 0, 40, 90 and 180 mins.. An important feature of the copper treatment is its relative insensitivity to the processing time. This is clearly demonstrated by the data in table (5-13) and figure (5-16) which show that after the first 40 mins. of heating, the changes taking place during the subsequent 2 h were quite minor and these cells were then found to retain their charcteristics for long periods under operational conditions without encapsulation, as described in section 5-4.

5.2.5. Temperature dependence of the photovoltaic properties

The experimental data of the temperature dependence of the short-circuit current, J_{SC}, and the open-circuit voltage, V_{OC}, are shown in figures (5-17) and (5-18) for three cells A, B and C. The cells were

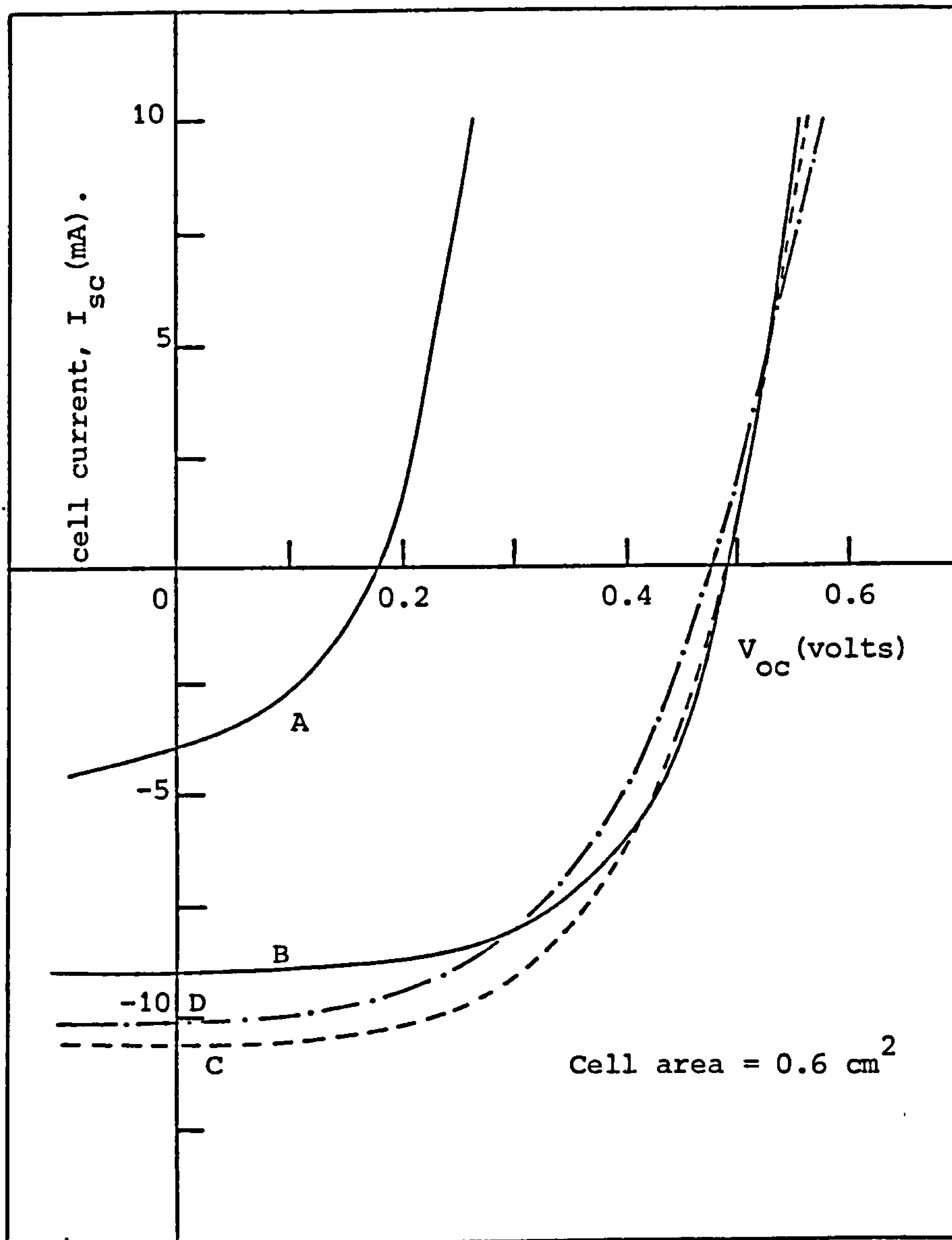


Figure (5-16) Effect of heating in air for (A) o mins., (B) 40 mins., (C) 90 mins.or (D) 180 mins. on the I-V characteristics of CdS-Cu_2S cell having a 100 Å over layer of copper.

TABLE (5-13). Variations in electrical characteristics with time of annealing in air at 200°C for cells with different thicknesses of copper overlayer.

Annealing time		Thickness of copper overlayer 0	50 Å	100 Å	200 Å
0 mins.	V_{oc} (V)	0.42	0.18	0.17	0.21
	I_{sc} (mA)	14.3	3.5	3.8	1.9
	J_{sc} mA cm^{-2}	19.06	5.8	6.3	3.1
8 mins.	V_{oc}	0.48	0.25	0.21	0.32
	I_{sc}	10.5	4.0	3.5	2.8
	J_{sc} mA cm^{-2}	14.0	6.6	5.8	4.6
20 mins.	V_{oc}	0.48	0.39	0.45	0.36
	I_{sc}	9.2	4.3	6.8	4.0
	J_{sc}	12.2	7.1	11.3	6.5
40 mins.	V_{oc}	0.47	0.49	0.49	0.44
	I_{sc}	6.0	8.3	8.8	6.0
	J_{sc}	8.0	13.8	14.6	9.8
60 mins.	V_{oc}	0.44	0.48	0.495	0.47
	I_{sc}	4.3	8.3	9.0	6.8
	J_{sc}	5.7	13.8	15.0	11.14
90 mins.	V_{oc}	0.4	0.48	0.49	0.48
	I_{sc}	3.8	9.0	10.5	6.9
	J_{sc}	5.0	15.0	17.5	11.3
180 mins.	V_{oc}	0.25	0.46	0.48	0.48
	I_{sc}	2.8	6.8	10.0	5.9
	J_{sc}	3.7	11.3	16.6	9.67

prepared using the standard preparation conditions as described previously but they were annealed under different annealing conditions (different time, and different ambient atmosphere). For the measurement of V_{oc} and J_{sc} in the range -80°C to 80°C, the cells were mounted onto a temperature controlled Cu block and kept in vacuum. Simulated solar radiation at AMI (100mW cm^{-2}) was once again employed and care was taken to ensure that sufficient time was allowed for thermal equilibrium to be achieved before any reading was taken.

Figure (5-17A) shows the variation of J_{sc} with the temperature for the cell A before and after 3, 6, 20 and 40 mins. annealing in air at 200°C, while in figure (5-17B) and (5-17C) the cells were annealed for 20, 140, 240 and 480 mins. in vacuum and hydrogen ambient atmospheres respectively.

In cell A, the short-circuit current, as expected, initially increased as the annealing time was increased and, while being relatively insensitive to temperature over most of the temperature range employed, there was a strong decrease of J_{sc} in curves b and c at temperatures higher than +50°C. No such change occurred in curve d or e, following the deterioration in J_{sc} due to excessive annealing in air (for 20 and 40 mins. respectively). However, before the annealing took place (curve a) the short-circuit current, J_{sc}, showed a distinct increase at high temperatures (over 70°C). This is likely to be due to the fact that the time taken for each measurement at the elevated temperature is equivalent to a short anneal in vacuum during which there would be a consequent improvement in the value of J_{sc}. For vacuum annealing (figure 5-17B), although an improvement of the short-circuit current is obtained at low temperature for annealing times up to 4 hours, its value is seen to drop very rapidly with temperature above a certain threshold, with the threshold moving to lower

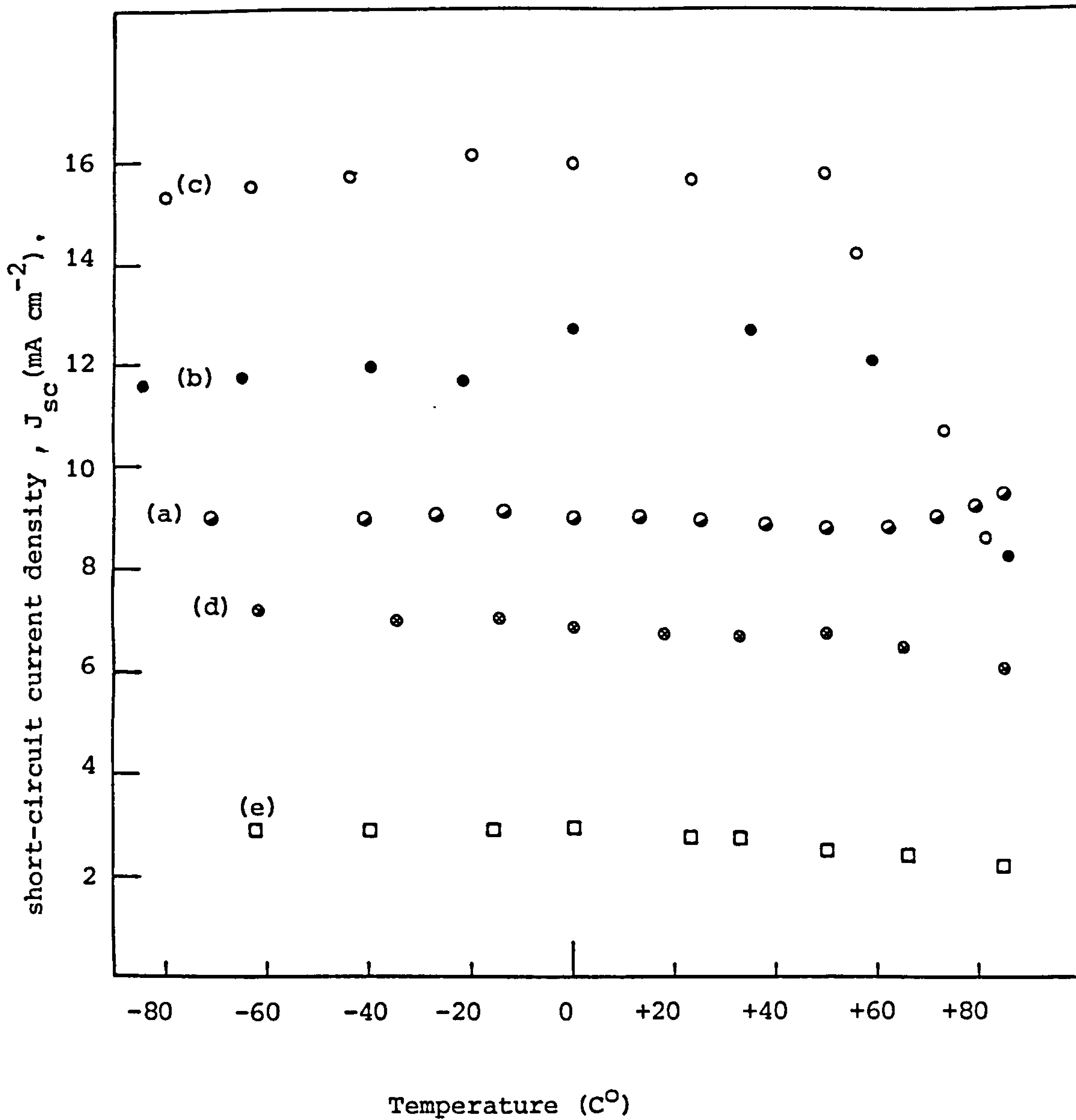


Figure (5-17) Short-circuit current, J_{sc}, as a function of temperature before and after various annealing time.

Figure (5-17A) Air annealing : (a) for freshly prepared cell, while b, c, d and e for the same cell after 3, 6, 20 and 40 mins. annealing treatment.

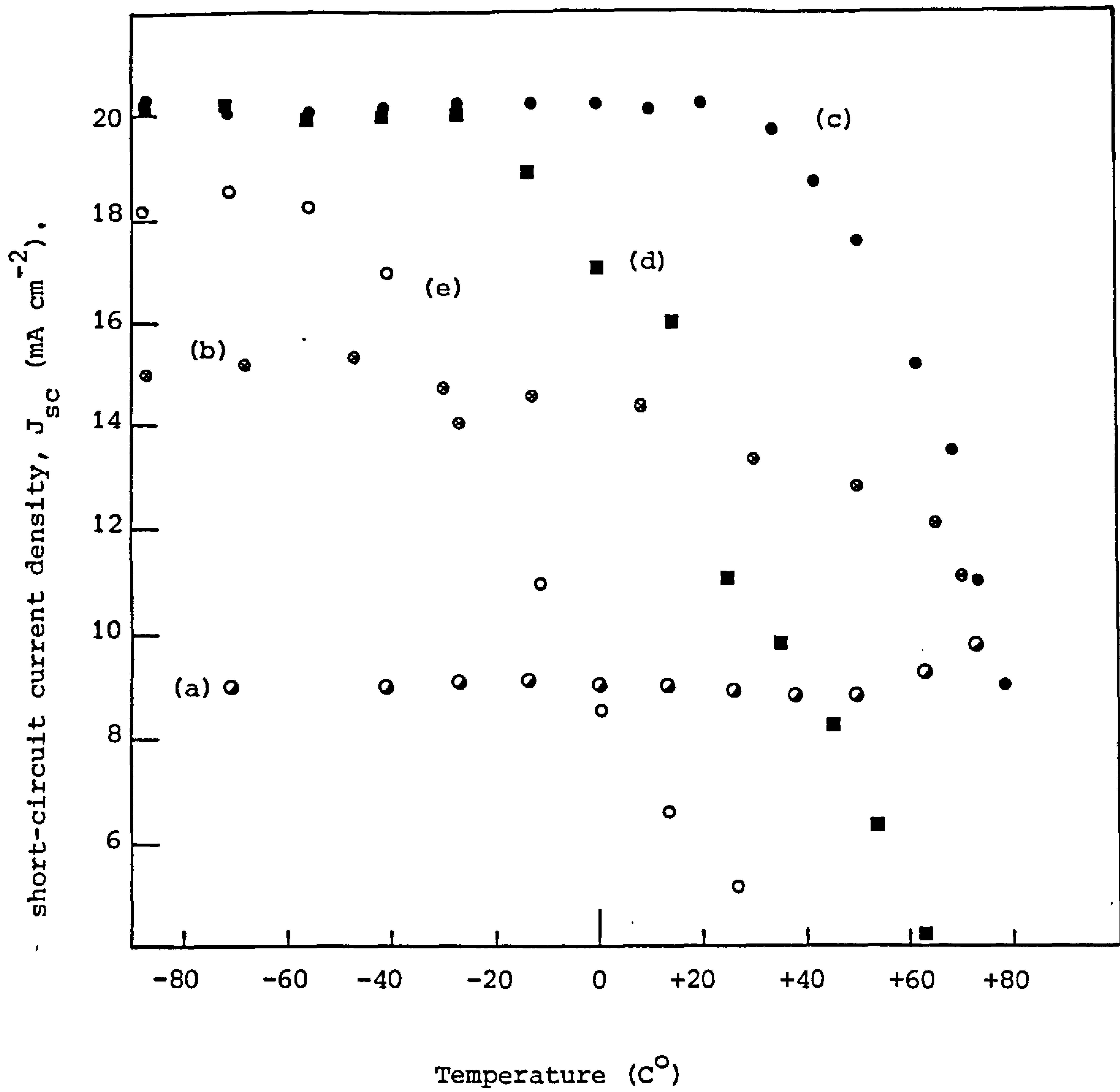
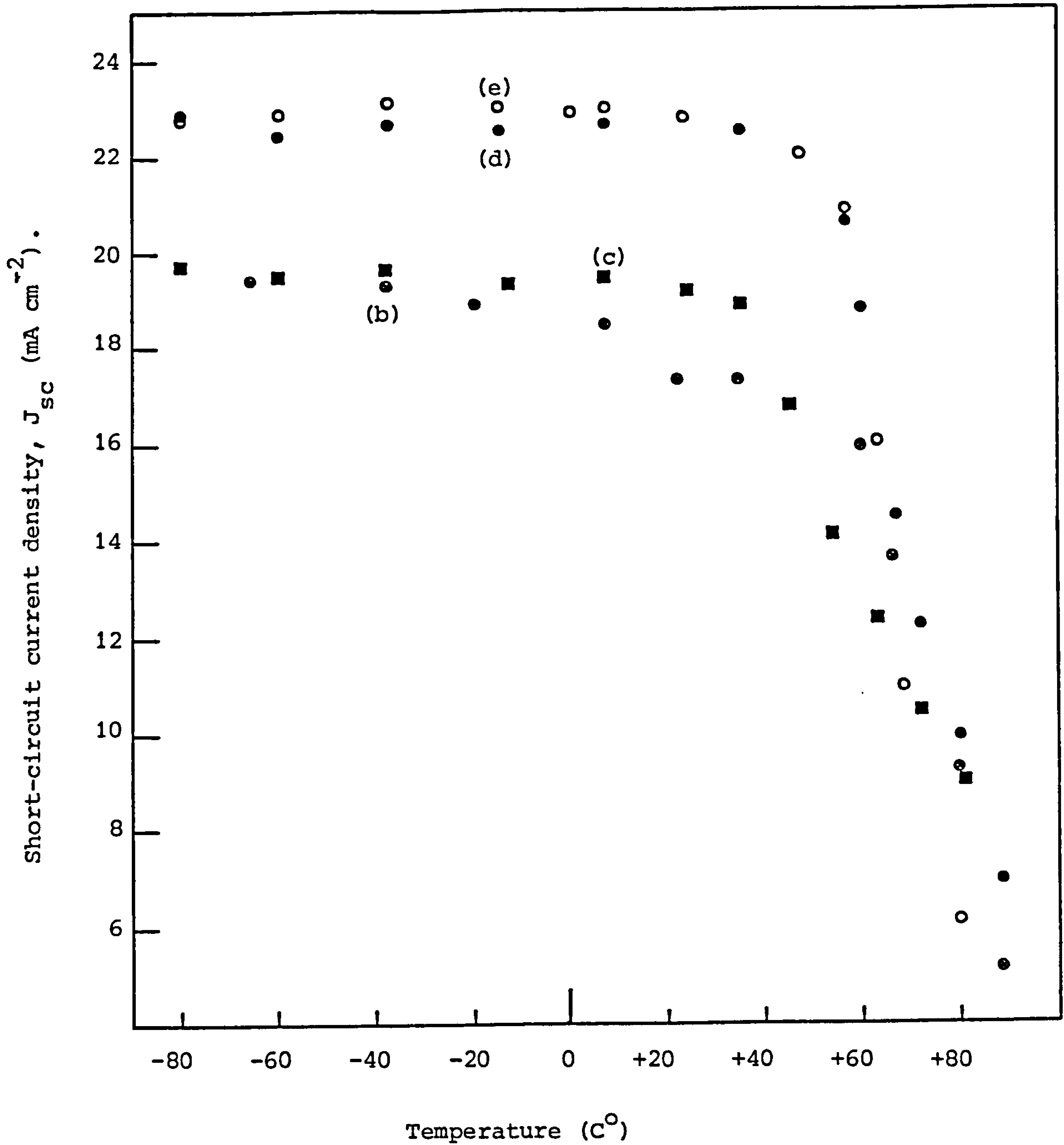


Figure (5-17B) Vacuum annealing : (a) for freshly prepared cell, while b, c, d and e for the same cell after 20, 140, 240 and 480 mins. annealing treatments.



Figure(5-17C) Hydrogen annealing: b, c, d and e for the same cell after the same cell after 20, 140, 240 and 480 mins.annealing treatment.

temperatures as the annealing time of the cell was prolonged. Accordingly, after 8 hours annealing in vacuum the value of J_{SC} is very small at room temperature whereas, if the annealing was terminated after 140 mins. (curve c, figure 5-17B), a high and nearly temperature independent short-circuit current is sustained to temperatures up to approximately 40°C.

For the cell annealed in hydrogen (figure 5-17c) the short-circuit current is seen to improve as the annealing time is increased and after 8 hours of annealing time, this cell displays temperature insensitivity up to 40°C, similar to the improved vacuum-annealed cell (cell B, curve c).

The variation of the open-circuit voltage, V_{OC}, with temperature is shown in figure (5-18A) and (5-18B). Figure (5-18A) shows the effect of air annealing, while figure (5-18B) shows the effect of vacuum annealing. For hydrogen annealing similar results to that shown in figure (5-18B) were obtained. It is seen that the V_{OC} value drops over the entire range slowly at first until a temperature of about -50°C is reached and then more rapidly over the rest of the range.

5.2.6. The effect of illumination intensity

Typical results showing the effect of different light intensities on the I-V characteristics of the $CdS-Cu_xS$ cells are shown in figure (5-19). The curves were taken at light intensity values from 10 to 180 mW cm^{-2} at room temperature. As expected, the short-circuit current, I_{SC}, increases approximately linearly with the light intensity, and the open-circuit voltage, V_{OC}, rises with higher light levels and starts to saturate. It is clear from figure (5-19), that the slopes of the I-V curves at the current axis become less horizontal with increasing light,

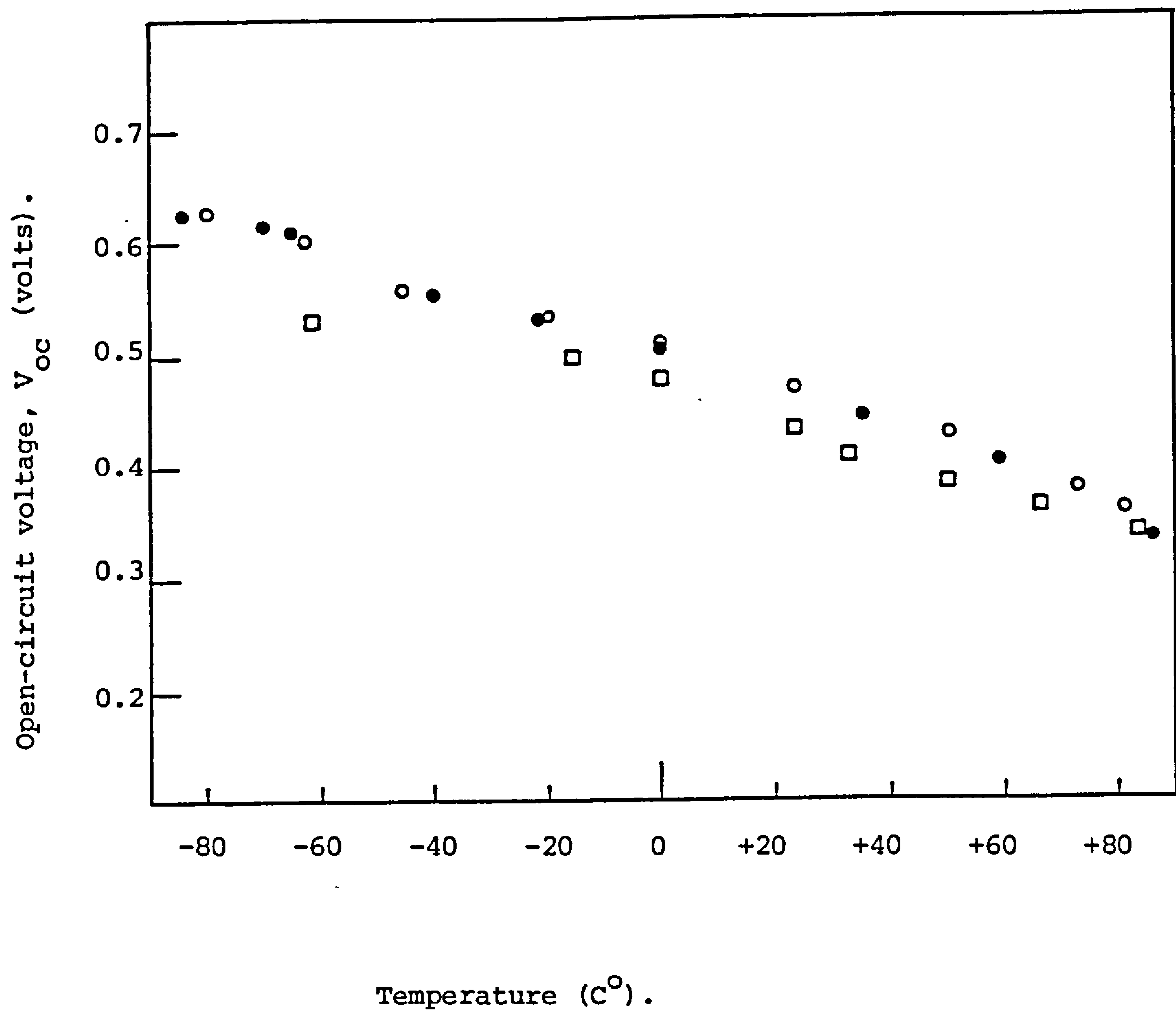


Figure (5-18) Open-circuit voltage, V_{oc}, as a function of temperature for various annealing times.

Figure (5-18 A) Air annealing. Point symbols as in figure (5-17A).

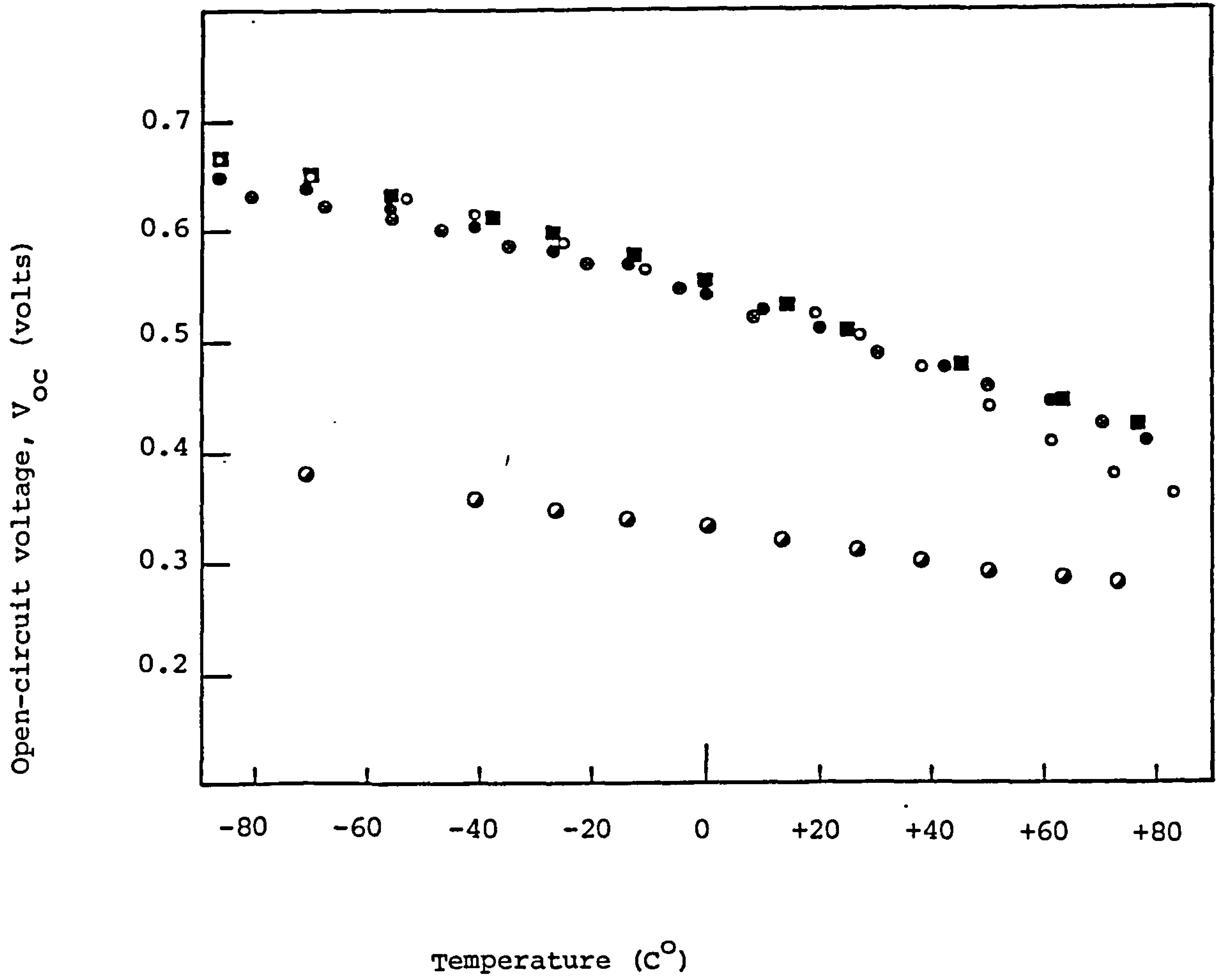


Figure (5-18B) Vacuum annealing. Point symbols as in figure (5-17B).

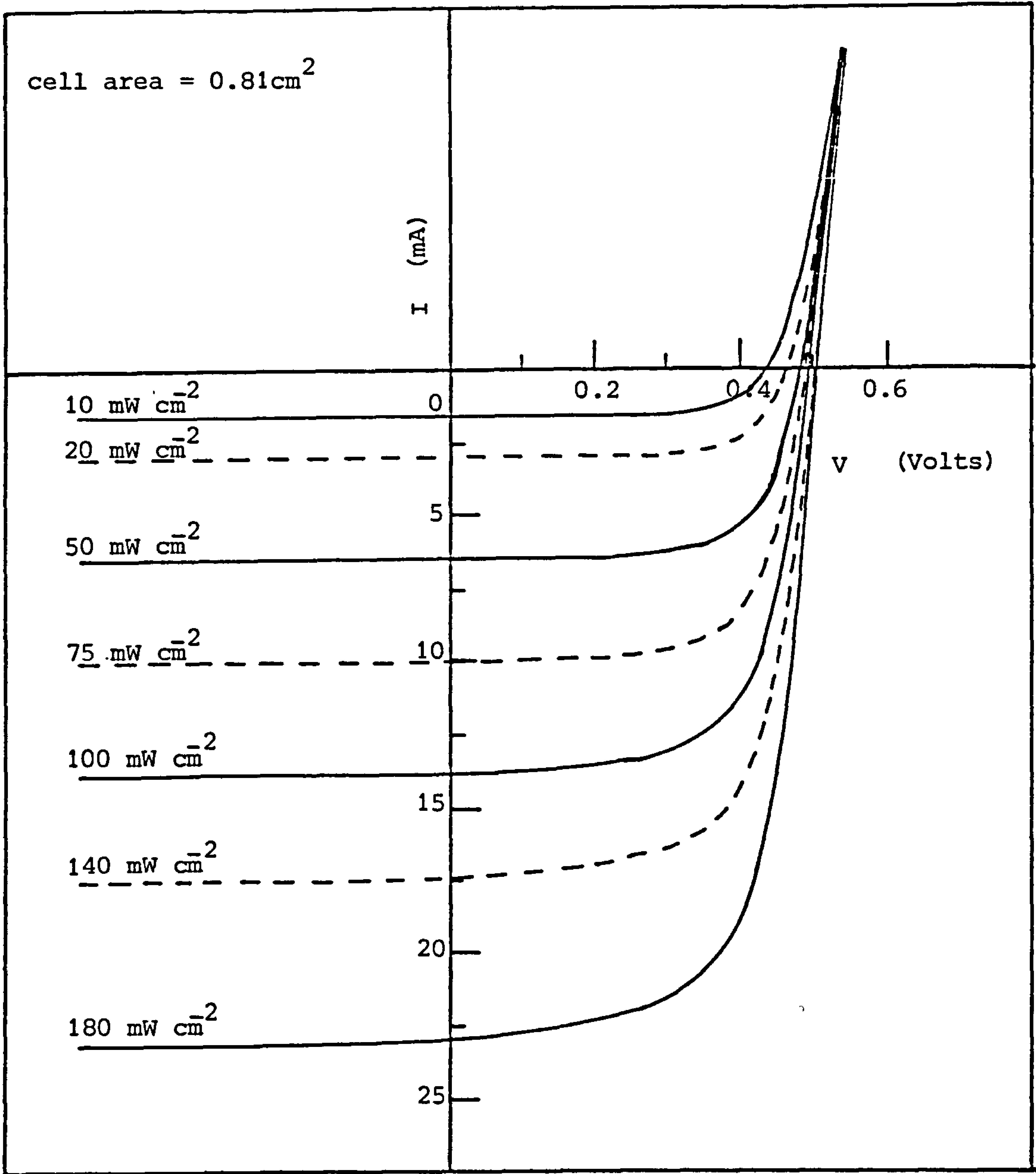


Figure (5-19) I-V characteristics for 20 mins. hydrogen annealed $CdS-Cu_xS$ solar cell under different light intensities.

which indicates a decrease in the shunt resistance of the device. However, offsetting this is the rise in open-circuit voltage and a decreasing internal series resistance indicated by the slope of the curves at the voltage axis becoming more nearly vertical with increasing light intensity.

From the values of V_{oc} and I_{sc} in figure (5-19), a plot of ln J_{sc} versus V_{oc} gives a straight line, as can clearly be seen in figure (5-20). This plot indicates that the relation between V_{oc} and I_{sc} in equation (3-7) holds perfectly well ($J_{sc} \sim J_L$), and values of n = 1.18 and $J_o = 1.68 \times 10^{-6}$ mA cm^{-2} at room temperature were obtained.

5.2.7. Determination of heterojunction parameters

(i) Freshly prepared cells.

The dark, room-temperature I-V characteristics of a typical freshly prepared CdS-Cu_2S heterojunction are shown in figure (5-21). It is clear that three different regions can be distinguished which correspond to different conduction mechanisms occurring over different voltage ranges. At low voltages (less than 0.15 volts) the conduction follows Ohm's law whereas at higher voltages the conduction follows diodic behaviour with two different slopes. However at forward voltages above 0.7 volts, as is clearly shown in figure (5-21), the series resistance of the cell becomes important and the linearity is lost.

The two regions which follow the diodic behaviour (regions II and III) can be fitted to equation (3-28), and values of the diode ideality factor, n, and the reverse saturation current, I_s, can be obtained. The resulting values are listed in table (5-14). The barrier height can be calculated using the expression for the reverse saturation current, as has

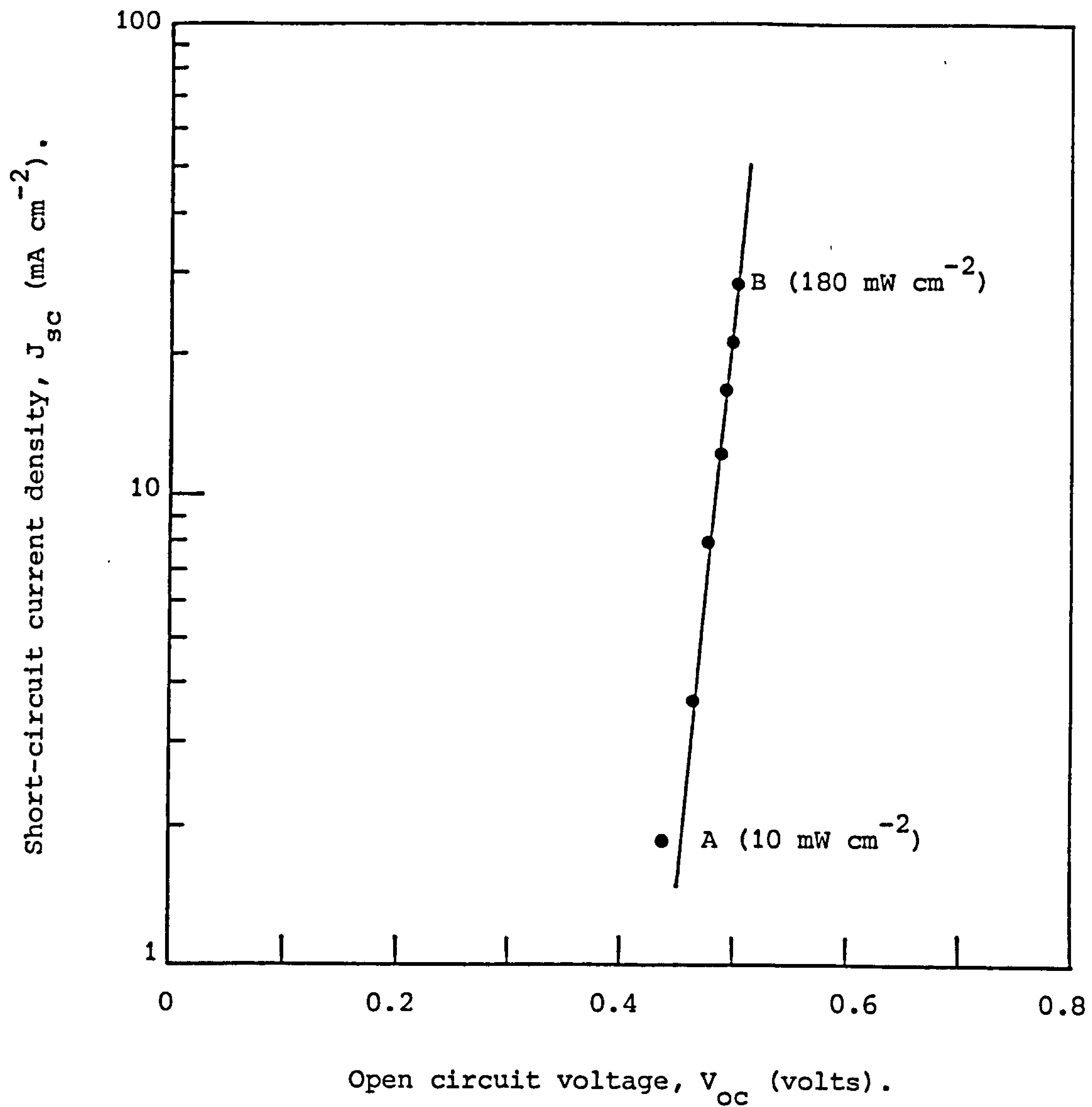


Figure (5-20) The dependence of short-circuit current on open-circuit voltage as a function of intensity for the same cell in figure (5-19).

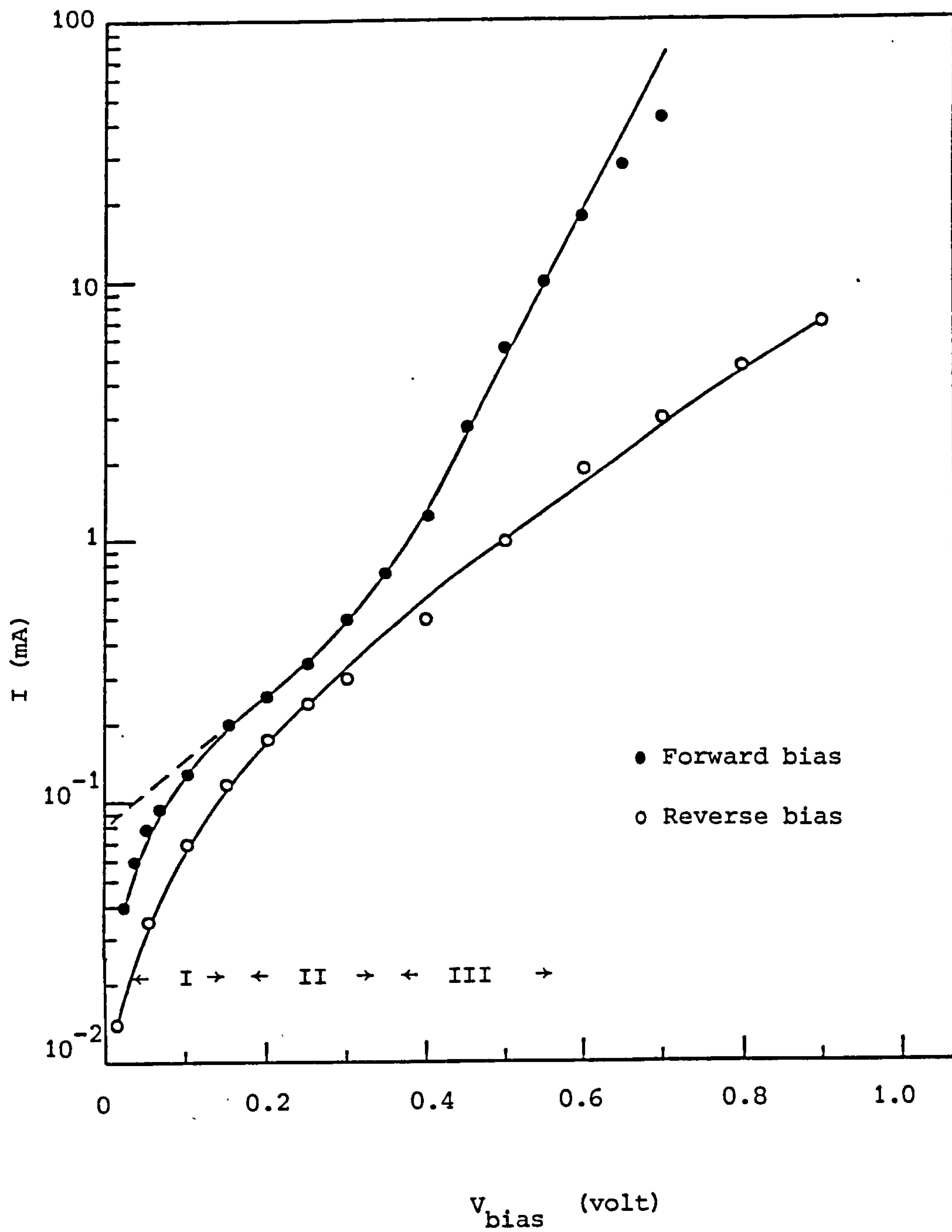


Figure (5-21) Dark current-voltage characteristics for a freshly made cell at room temperature.

been proposed by Rothwarf (157) using the interface recombination model. According to this model the reverse saturation current is given by

$$J_s = e\, S_I\, N_c \exp\ (-e\phi/kT) \qquad (5\text{-}2)$$

or

$$\phi = \frac{kT}{e}\ \ln\ \left(\frac{J_s}{e\, S_I\, N_c}\right) \qquad (5\text{-}3)$$

where S_I is the interface recombination velocity, and N_C is the effective density of states for CdS [$N_C = 2\ (2\pi\, m^*\, kT\, h^{-2})^{3/2} = 4.42 \times 10^{14}\ (T)^{3/2}$] (99) where m^* is the effective mass at room temperature $N_C \sim 2.2 \times 10^{18}\ cm^{-3}$. Assuming a value for S_I of about 5×10^6 cm sec^{-1} (163), the barrier heights listed in table (5-14) were obtained for the cell whose characteristics are shown in figure (5-21).

Figure (5-22) shows the plot of log I_R versus log V_R. This plot demonstrates that the reverse characteristics can be described by the expression $I_R\ \alpha\ V_R^{\gamma}$. At low voltage (less than 0.1), $\gamma = 1$ is calculated from the slope in the region a. As the reverse bias increases, γ is seen to increase, thus for voltage above 0.4 volts (region c) the reverse current is compatible with Zener effect ($J_R = B\, V^{\gamma}$, $\gamma > 2$) and a value of $\gamma = 3.2$ is calculated.

(ii) The effect of post-fabrication annealing treatment.

As discussed in section (5.2.3), annealing in a hydrogen atmosphere is an important step in achieving high efficiency cells. Therefore we have been concerned to study changes in the conduction processes in the cells after hydrogen annealing. Figure (5-23) shows the dark I-V characteristics (for the cell discussed in the previous section) after 20 mins. hydrogen annealing at 200°C. It is clear that these curves

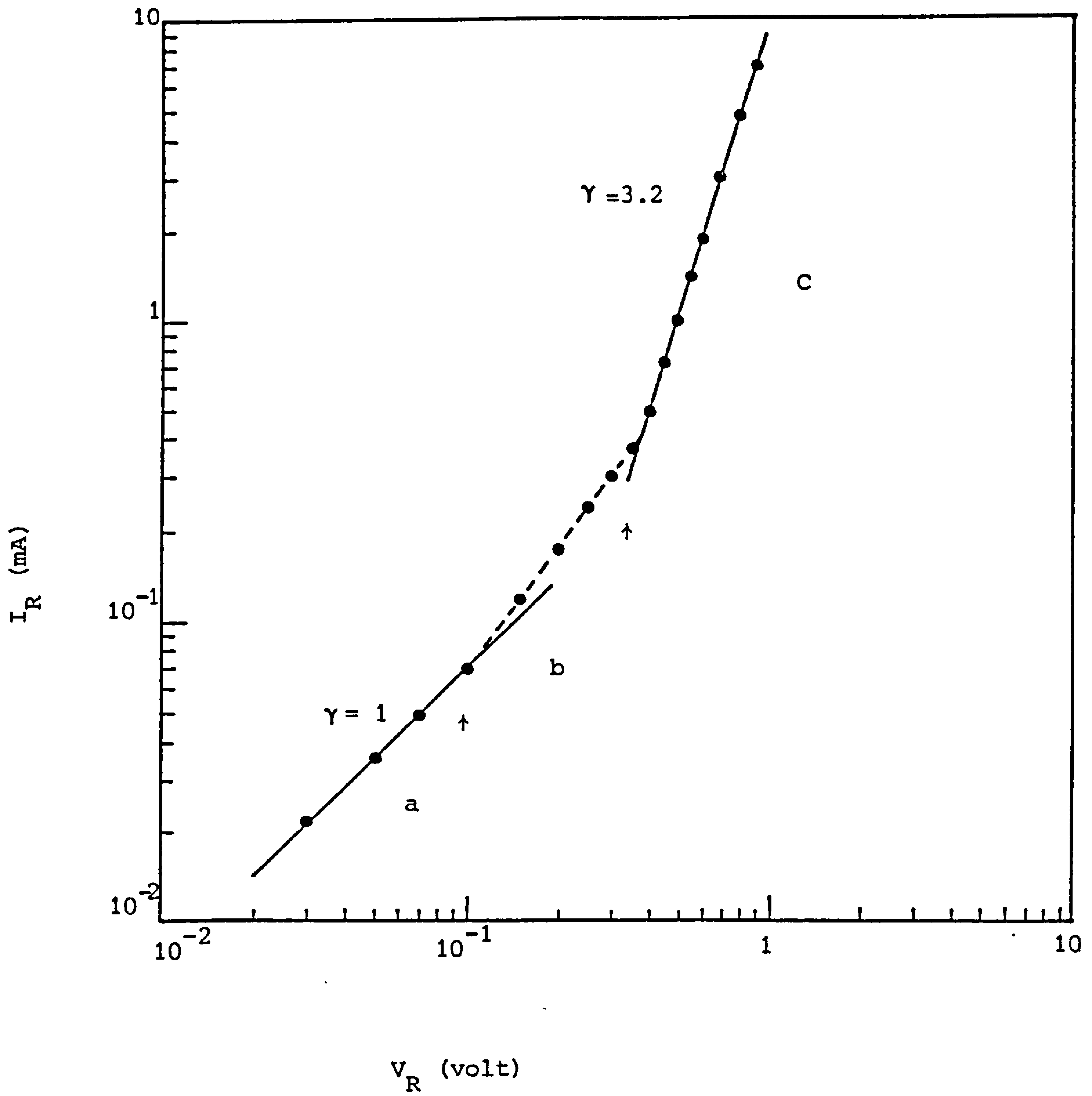


Figure (5-22) Log-log plot dark reverse current-voltage characteristics at room temperature for a freshly made cell.

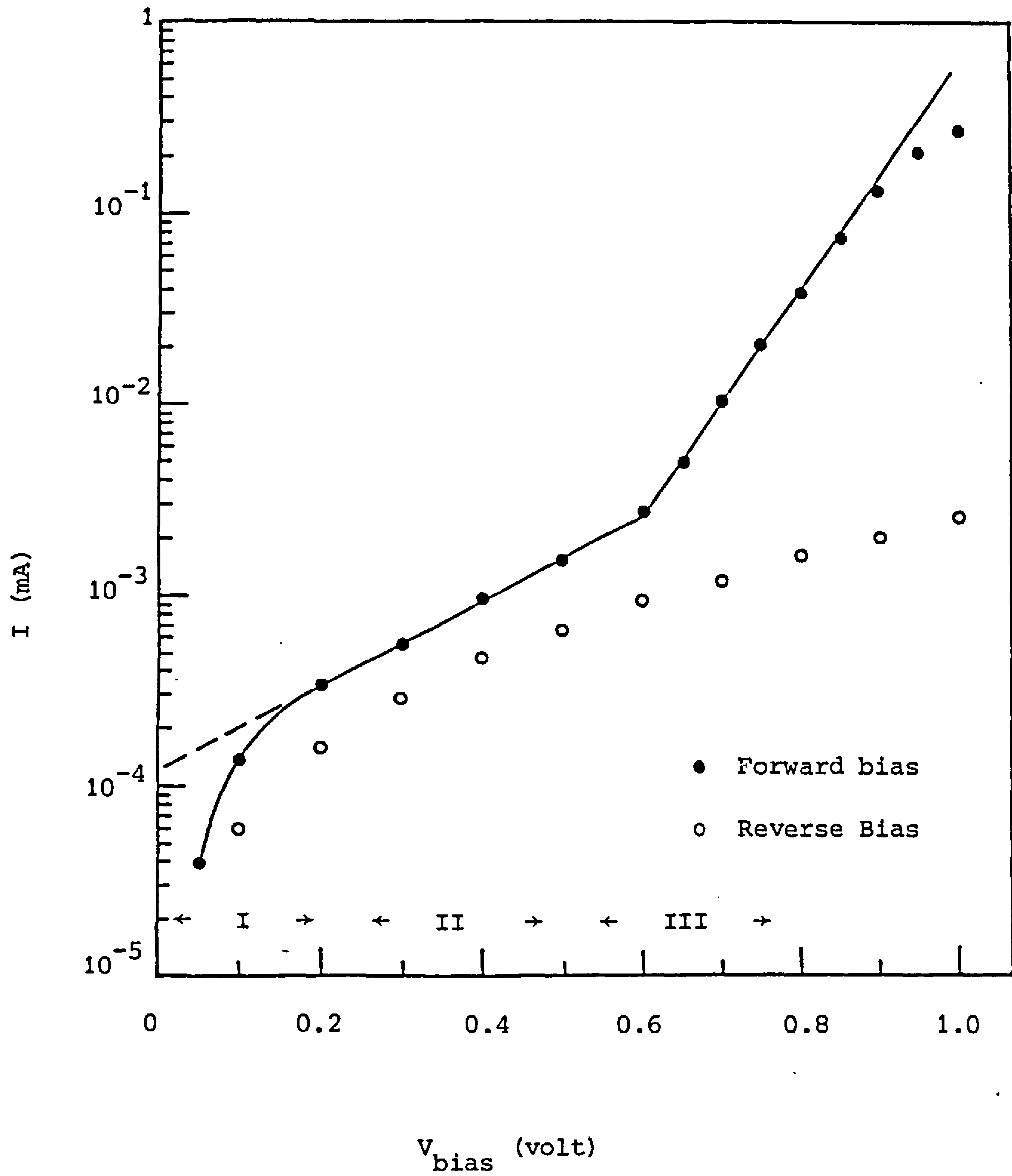


Figure (5-23) Dark current-voltage characteristics at room temperature for the same cell in figure (5-21) after 20 mins. hydrogen annealing at 200°C.

TABLE (5-14). Values of reverse saturation current density, J_s, diode ideality factor, n, and barrier height of CdS-Cu_xS cell before and after annealing.

	region	J_s (mA cm^{-2})	n	Φ (ev)
A - For freshly prepared cell	II	1.06×10^{-1}	6.94	0.60
	III	1.0×10^{-2}	3.03	0.66
B - After 20 mins. hydrogen annealing treatment at 200°C.	II	1.5×10^{-4}	7.65	0.77
	III	1.12×10^{-6}	2.88	0.90

have a similar structure to those shown in figure (5-21) for the as-prepared cell, but the three regions seem to have shifted towards higher voltages and provide different values for the diode ideality factor and barrier heights as listed in table (5-14). It is clear that as a result of this annealing treatment an increase in the barrier height values are seen in II and III regions with accompanied reductions of the reverse saturation current. As can be seen in figures (5-21) and (5-23) the region II seems to occur at relatively higher forward bias after annealing treatment and is sustained up to 0.6 volts, where region III begins. In fact when the annealing treatment was continued up to 8 hours in hydrogen at 200°C no conversion to region III was observed, with region II being maintained up to at least 3 volts.

The variation of reverse current with applied voltages is shown in figure (5-24). Once again the three different regions a, b and c similar to that in as-prepared cells are clearly seen after 20 mins. annealing treatment in hydrogen at 200°C. However, the region between the ohmic behaviour and Zener effect (region b) seems to be wider as compared with

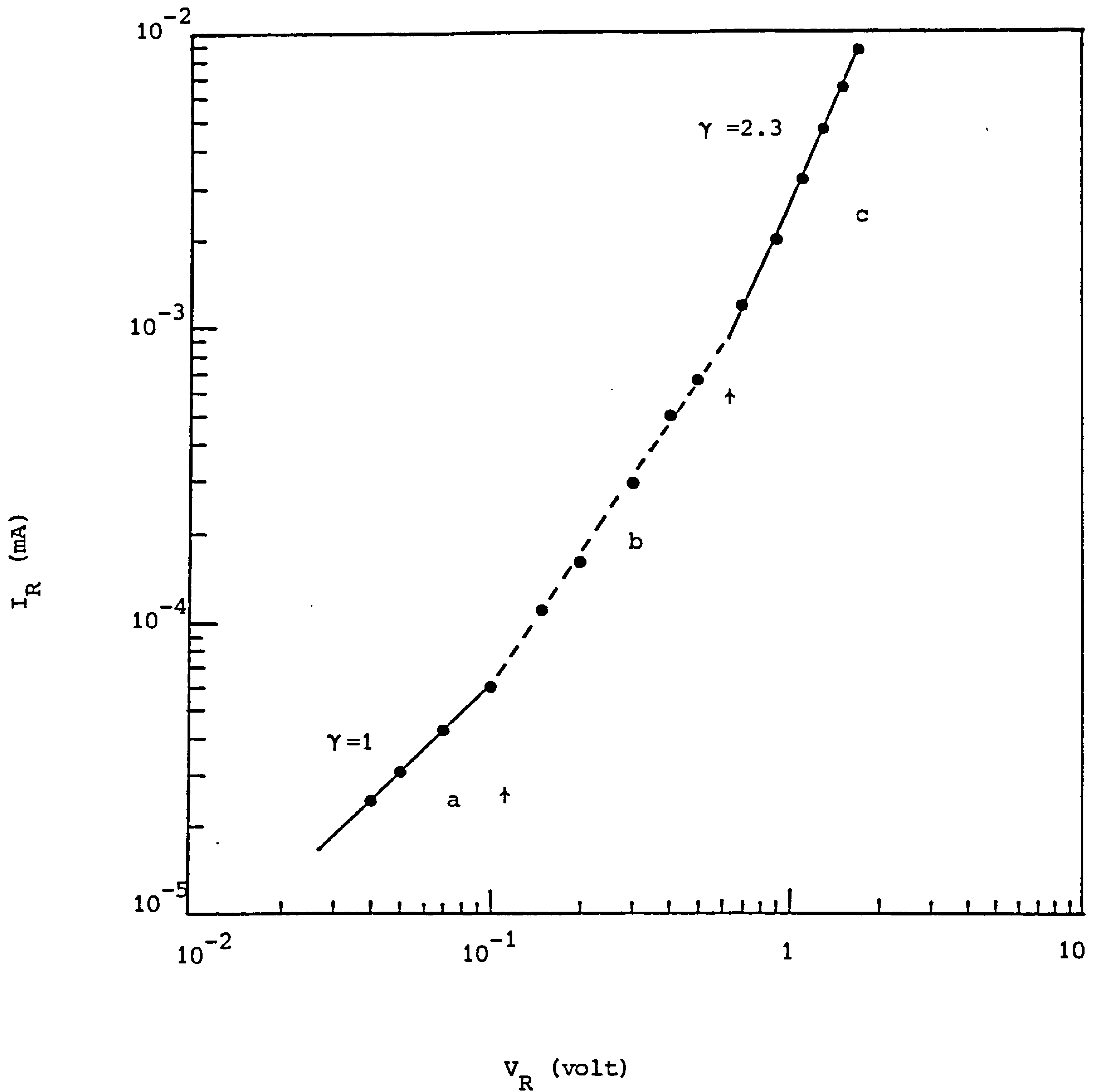


Figure (5-24) log-log plot of dark reverse current-voltage characteristics at room temperature for the same cell in figure (5-21) after 20 mins. hydrogen annealing at 200°C.

figure (5-22) for as-prepared cell and the value of γ = 2.3 is found to be smaller in the region c, in the case of annealed cell.

The above cell was also investigated under illumination at AMI light intensity. Figure (5-25) shows the plot of eV_{OC} versus kT. This plot is a straight line over temperature in the range 170-340 K. At lower temperatures the open-circuit voltage is found to saturate. However, when the line is extrapolated to kT = 0 a value of 0.95 eV, corresponding to the barrier height is obtained. According to equation (2-2), a value of ΔE_C, the electron affinity difference can be calculated. Taking the band gap of Cu_2S as 1.2 eV then the value of ΔE_C from the extrapolated value of $(E_{g1} - \Delta E_C)$ is found to be 0.25 eV. This value is found to be independent of illumination intensity. It should be noted that for other cells values of ΔE_C in the range of 0.20-0.3 eV have been calculated. This variation is due partly to experimental errors and partly to assuming the presence of a pure chalcocite phase of copper sulphide with a band gap equal to 1.2 eV. However these calculated values of ΔE_C are in good agreement with the values reported by other authors [134, 215], although Boer [216] has quoted a value of 0.35 eV.

Figure (5-26) shows the I-V characteristics of the CdS-Cu_2S solar cells similar to that studied above, but the annealing treatment was continued up to 8 hours in hydrogen at 200°C. The cell parameters are listed next to the I-V characteristics. The quoted thickness of the copper sulphide layer together with the values of x were made on a different but identically fabricated cell, using a CdS film from the same batch.

5.2.8. Capacitance - Voltage characteristics

Capacitance - voltage characteristics for Au-CdS and CdS-Cu_xS

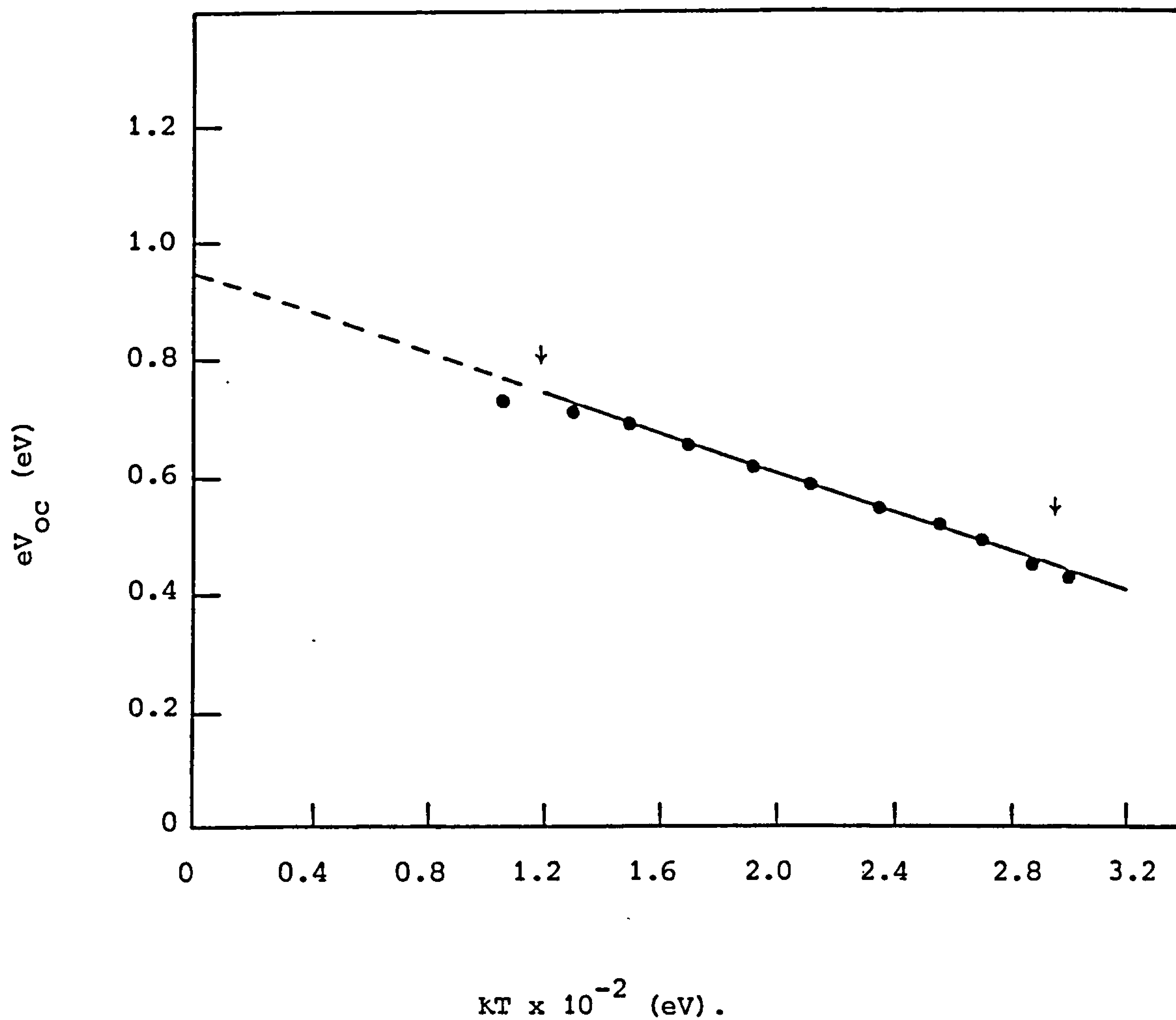


Figure (5-25) Plot of eV_{oc} versus KT for CdS-Cu_2S solar cell after 20 mins. hydrogen annealing at $200^{o}C$.

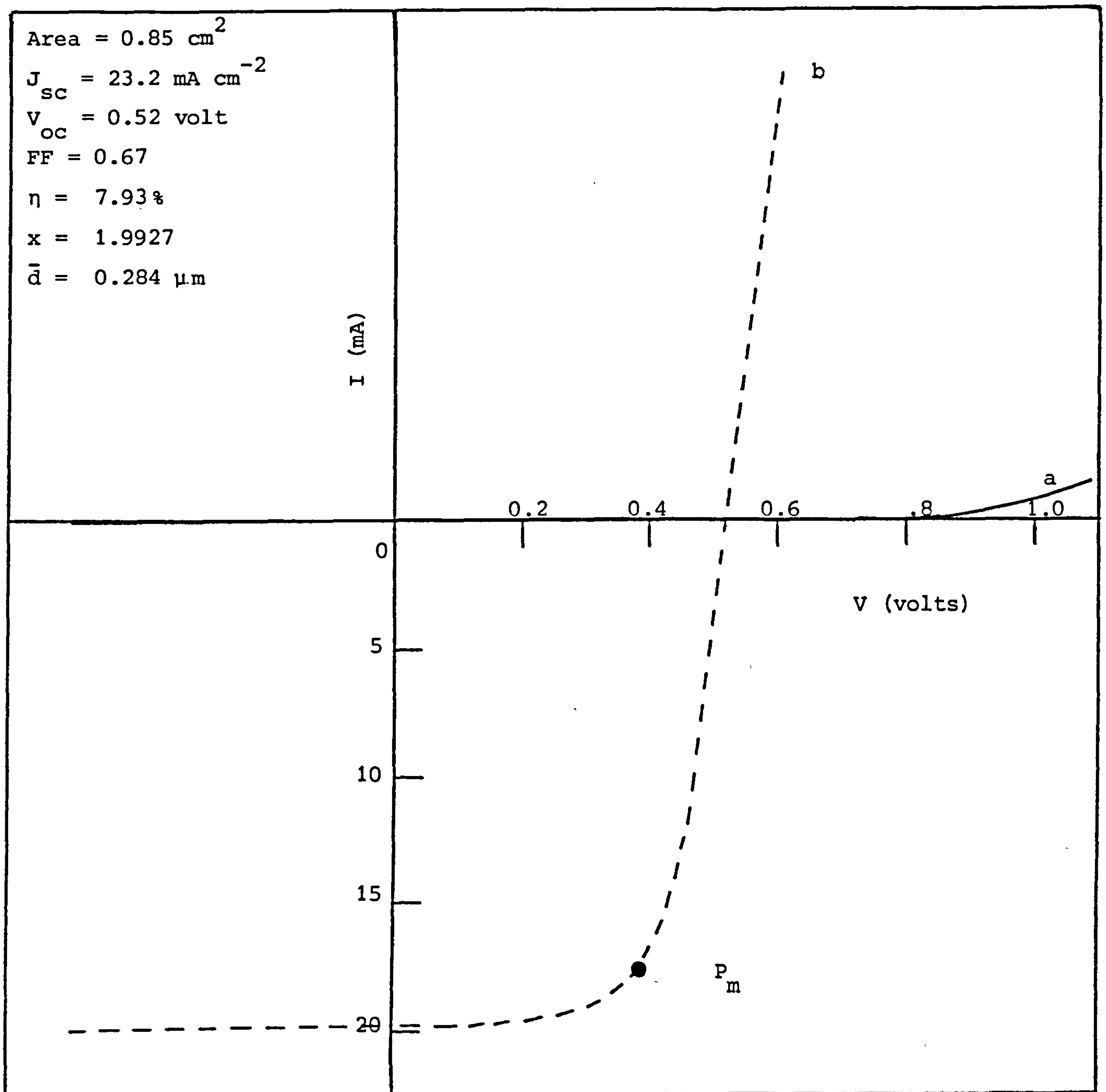


Figure (5-26) current-voltage characteristics of CdS-Cu_2S solar cell after 8 hrs. hydrogen annealing at 200°C, (a) in the dark and (b) under AM1 light intensity.

junctions were studied to gain information concerning the majority carrier concentration (the net donor density) of the CdS, the diffusion voltage and changes in the space charge layer width resulting from different annealing treatments.

Typical results for dark junction capacitance - voltage characteristic of a Au-CdS Schottky diode are shown in figure (5-27). From the plot of C^{-2} versus applied reverse bias, the carrier concentration and the diffusion voltage are found to be 3.1×10^{17} cm^{-3} and 0.5 volts respectively.

Figure (5-28) shows the effect of annealing a $CdS-Cu_2S$ cell (cell A) which was fabricated from the same batch of CdS layers from which the sample in figure (5-27) was taken. These plots all yielded straight lines, and for the newly formed junction (curve i) it is clear that the carrier concentration of 2.66×10^{17} cm^{-3} calculated from the slope of the plot (i) agrees very closely with that obtained from the corresponding Au-CdS Schottky diode (figure 5-27). The low value of the diffusion voltage (0.54 volts) of the $CdS-Cu_xS$ cell in curve (i) is due to the high conductivity CdS layer. The annealing treatment resulted in decreased junction capacitance, indicating the formation of a compensated region of CdS at the $CdS-Cu_xS$ interface. It is clear in curve (ii) of figure (5-28) that the value of the diffusion voltage is increased. This value is very close to the expected value for the diffusion voltage of the $CdS-Cu_xS$ device (Case I in section 3-5). As the annealing treatment is prolonged, more copper diffuses to the CdS layer causing an increase in the width of the compensated layer and reduction in the carrier concentration, as is clearly shown in table (5-15) . The voltage - axis intercept, V_D^* of the plot (iii) is no longer equal to the diffusion voltage as a result of the formation of a region of highly compensated CdS at the $CdS-Cu_xS$ interface.

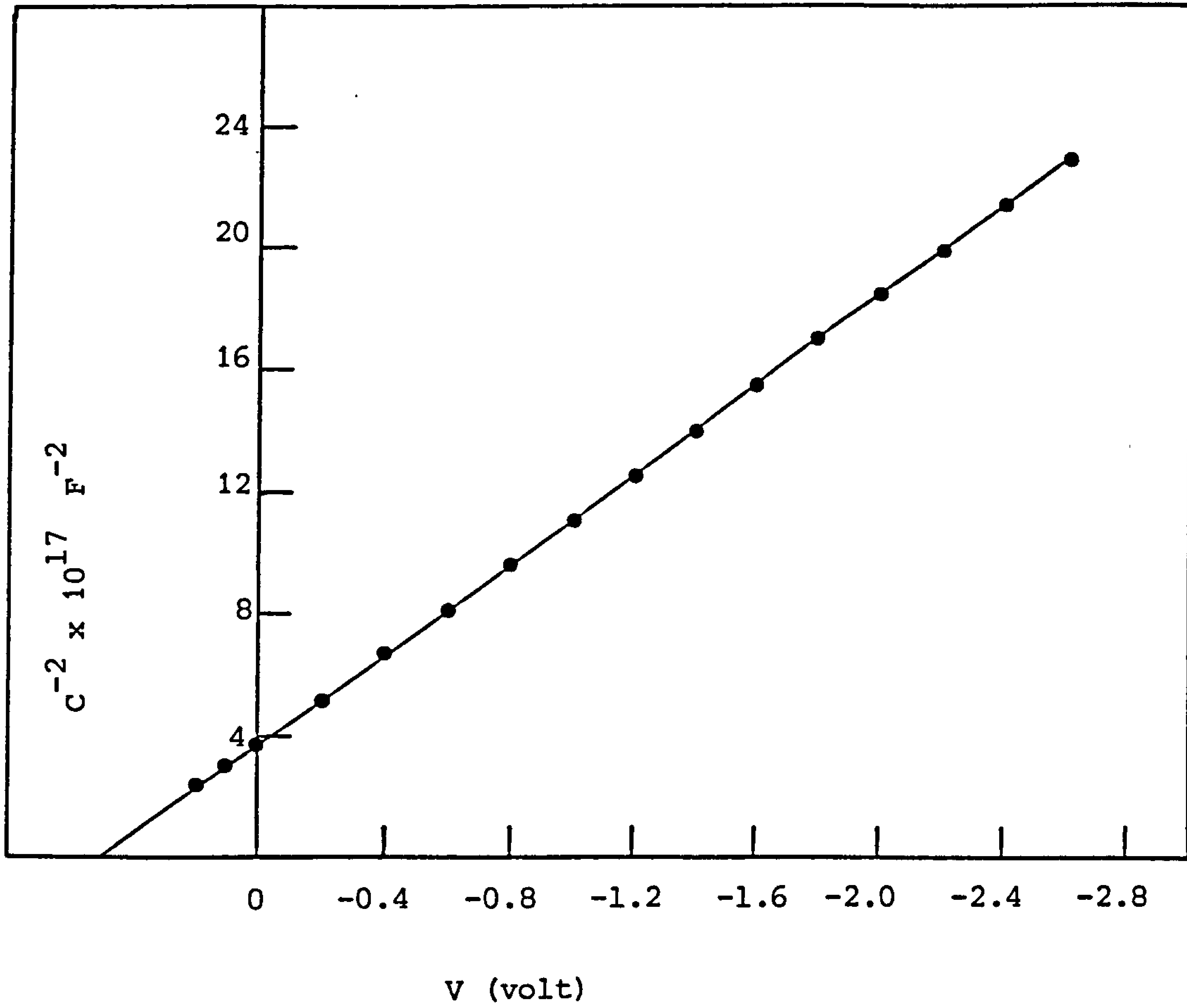


Figure (5-27) C^{-2} versus reverse voltage at room temperature for Au-CdS Schottky barrier.

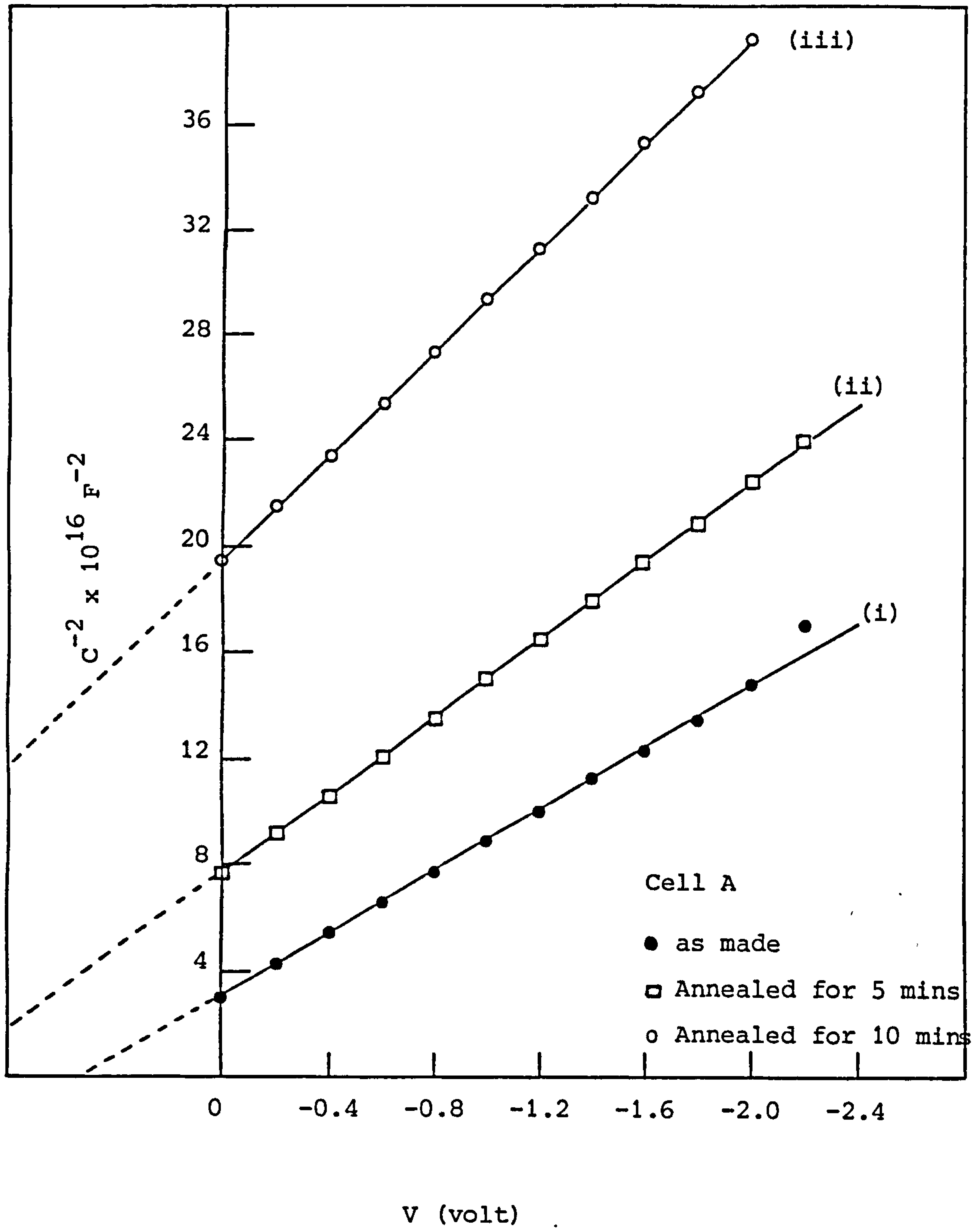


Figure (5-28) C^{-2} versus reverse voltage at room temperature for a $CdS-Cu_2S$ cell given different periods of annealing treatment in air at 200°C.

(This result conforms to Case III in section 3-5. From equation 3-48 a value of the thickness of the insulating layer $d_2 = 10.5 \times 10^{-6}$ cm is calculated).

When the copper sulphide was formed on a CdS layer having a much higher carrier concentration ($>10^{18}$ cm^{-3}) than that for cell A, the capacitance value at zero bias was higher than the upper limit of the capacitance meter (6000 pf) and no measurement could be made before any annealing treatment. Such behaviour indicates that the space charge layer width of the junction was very narrow, yielding nearly ohmic properties, as confirmed by measuring the I-V characteristics.

For a cell (cell B) made using a lower carrier concentration than that for cell (A), the capacitance - voltage characteristics before and after annealing treatment are shown in figure (5-29). The carrier concentration, N, and the voltage intercept V_D^*, together with the space charge layer width, W, for both cells A and B are listed in table (5-15). It is clear from figure (5-29) that even before annealing treatment of cell (B) the intercept of the plot (i) with the voltage axis is not equal to the expected diffusion voltage of the CdS-Cu_xS cell. This indicates that, the space charge layer is not homogenous even for the freshly prepared cell. The thickness of the insulating layer d_2 was calculated using equation (3-48) with the value for the diffusion voltage of $V_D = 0.8$ volt, (see section 6-3) obtained from the barrier height measurements (section 5.2.5).

As the capacitance meter was limited to the range 0 - 6000 pf, the devices under investigation had to be of very small area (of the order of 1-2 mm^2). As a consequence, the active area of the copper sulphide layer was entirely covered with the gold contact. With this contact in position during the annealing treatment for both cells A and B, the diffusion process at the CdS-Cu_xS interface was expected to be different to

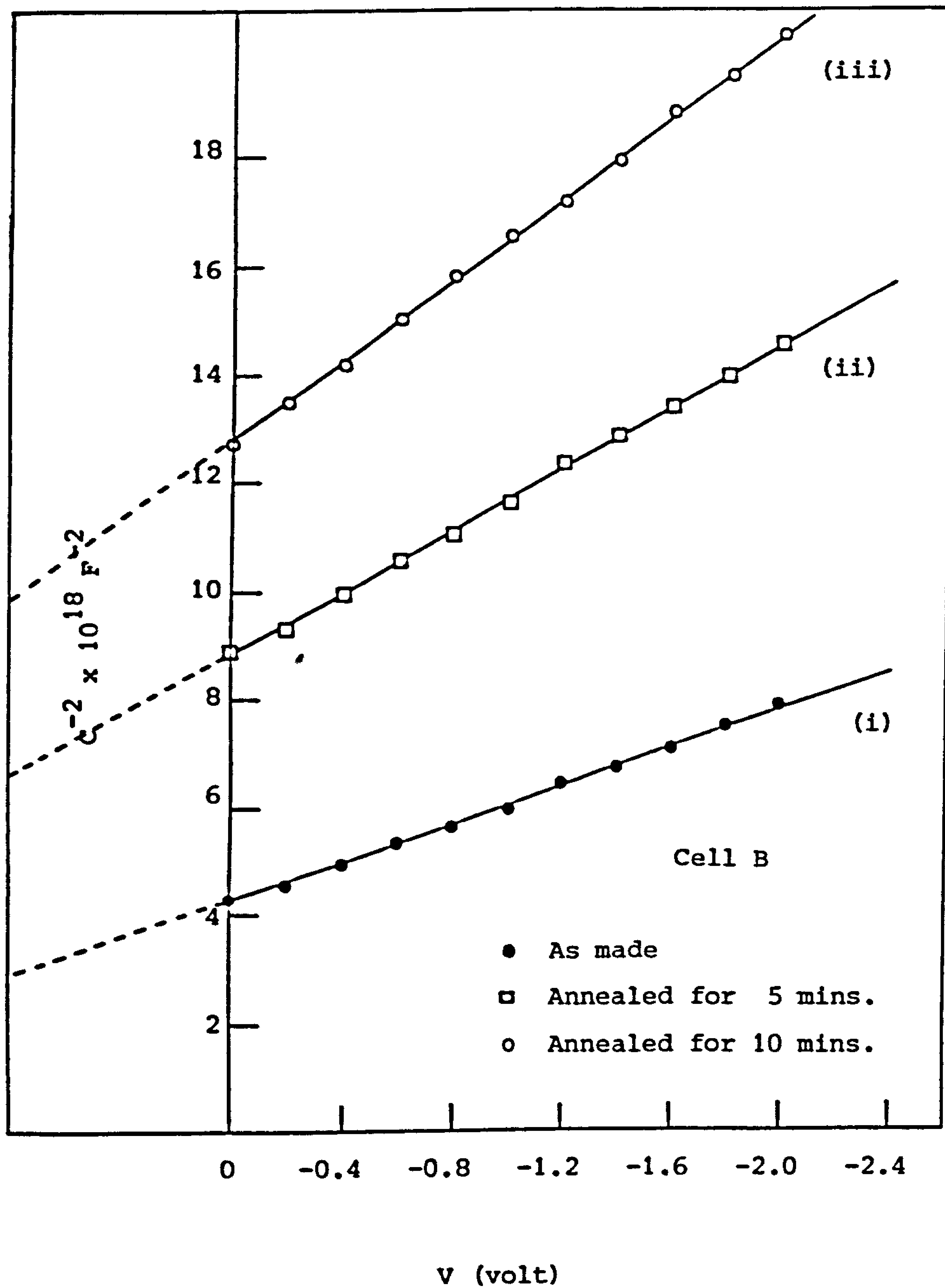


Figure (5-29) C^{-2} versus reverse voltage at room temperature for a CdS-Cu_2S cell given different periods of annealing treatment in air at 200°C.

TABLE (5-15). Carrier concentration, intercept voltage, space charge layer width and insulating layer width values for gold covered cells before and after air annealing.

	Annealing time (mins.)	N (cm^{-3})	V_D^* (volts)	W (cm)	d_2(cm)
Cell A	0	2.66×10^{17}	0.54	4.67×10^{-6}	—
	5	1.87×10^{17}	1.06	7.36×10^{-6}	3.92×10^{-6}
	10	1.19×10^{17}	2.0	11.1×10^{-6}	10.5×10^{-6}
Cell B	0	1.97×10^{16}	2.44	3.67×10^{-5}	3.03×10^{-5}
	5	1.23×10^{16}	3.14	5.28×10^{-5}	4.48×10^{-5}
	10	0.97×10^{16}	3.5	6.32×10^{-5}	5.54×10^{-5}

that applying in the absence of the contact. In fact the changes in the space charge layer width summarised in table (5-15) were found to occur after much shorter annealing times if the gold contact was evaporated after the annealing treatment. This is clearly shown in figure (5-30), where the space charge layer width is plotted as a function of annealing time for cell B (curve ii) and a set of similar cells annealed prior to gold contacting (curve i). For the latter case, the space charge layer width increases very rapidly with the annealing time for the first 20 mins., after which the values seem to saturate. If the annealing treatment was continued beyond 40 mins., the capacitance became nearly independent of the reverse voltage.

Annealing cycles in vacuum or hydrogen ambients were found to reduce the junction capacitance in a similar way to air annealing, but longer times were required to obtain changes equivalent to those illustrated in table (5-15).

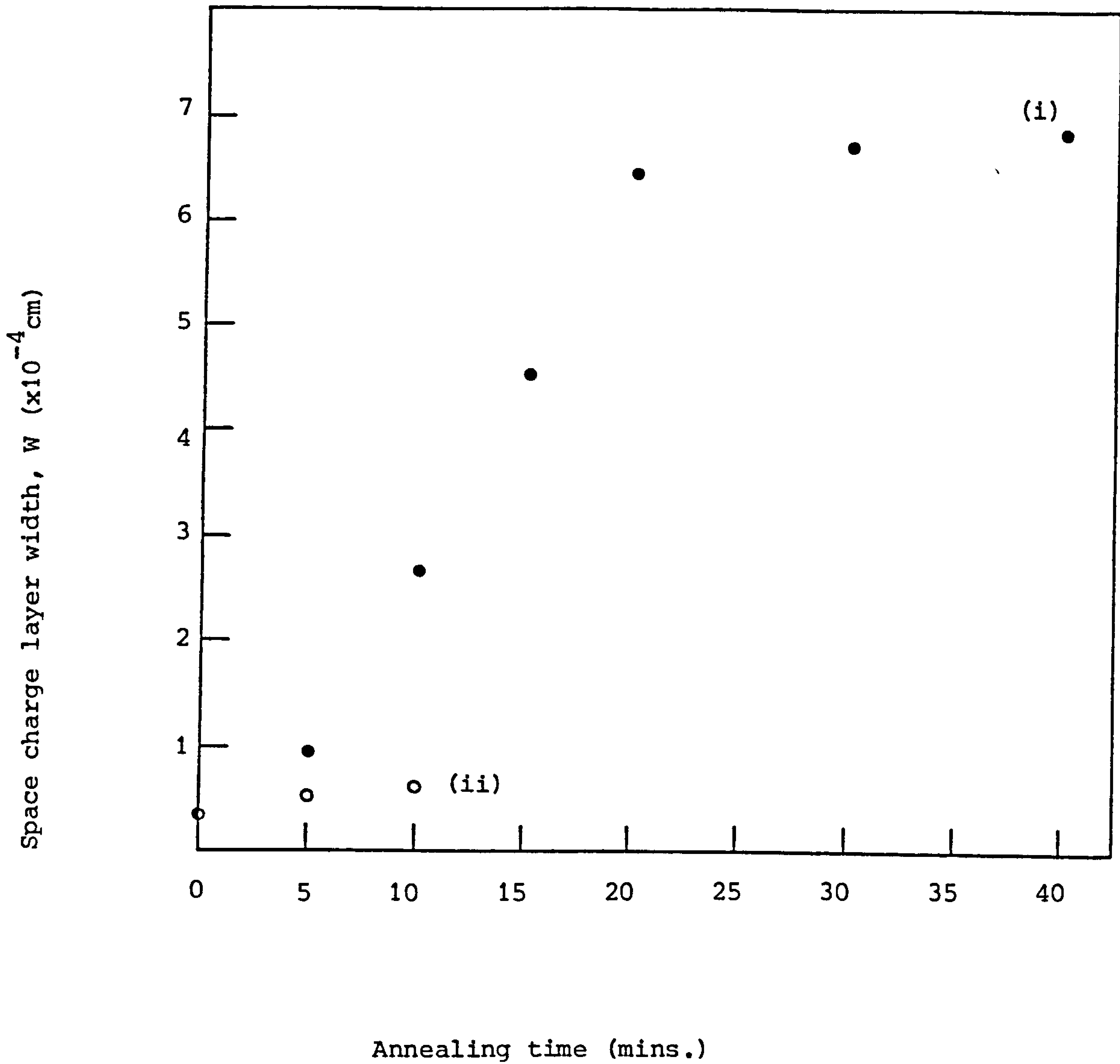


Figure (5-30) Space charge layer width as a function of annealing time in air, (i) refers to anneals prior to the gold contacting and (ii) for anneals after the gold contacting.

5.2.9. Deep levels in $CdS-Cu_xS$ solar cell

An indication of the presence of traps in the $CdS-Cu_xS$ solar cells was occasionally noted during the measurement of I-V characteristics when the current was found to drift with time at a fixed voltage setting. This drift generally increased with increasing forward bias and temperature.

In order to obtain some information about these traps a brief investigation was carried out using the DLTS technique. The transient capacitance apparatus for recording DLTS spectra made use of a double boxcar detection system, similar to that described by Lang [217], and a Boonton 72B capacitance meter. The measurements were made for two cells similar to those used in the previous section. The reverse bias did not exceed 2 volts, in order to avoid excessive current being drawn as a result of junction breakdown. The trap filling was achieved by applying a forward bias pulse of magnitude approximately equal to the reverse bias.

The DLTS spectrum for each $CdS-Cu_xS$ heterojunction solar cell, before and after 10 mins. air annealing treatment is shown in figure (5-31).

The trap emission rate, e_n, is given by [217]:

$$e_n = \ln \left(\frac{t_2}{t_1}\right) / (t_2 - t_1) \qquad (5\text{-}4)$$

where t_1 and t_2 are the boxcar gate opening times. The emission rate is related to the trap depth, E_T, and the capture cross section, σ_n, through the expression [217]:

$$e_n = N_c \, \sigma_n \, \nu_{th} \, \exp\left(-\frac{E_T}{kT}\right) \qquad (5\text{-}5)$$

where ν_{th} is the thermal velocity of the electrons ($\nu_{th} = 1.5 \times 10^6 \, T^{1/2}$ cm sec $^{-1}$) and N_C is the effective density of the states in the conduction band. Thus, from the slope and intercept of Arrhenius plots of $e_n \, T_m^{-2}$ versus T_m^{-1} (where T_m is the temperature of the DLTS peak) the trap depth

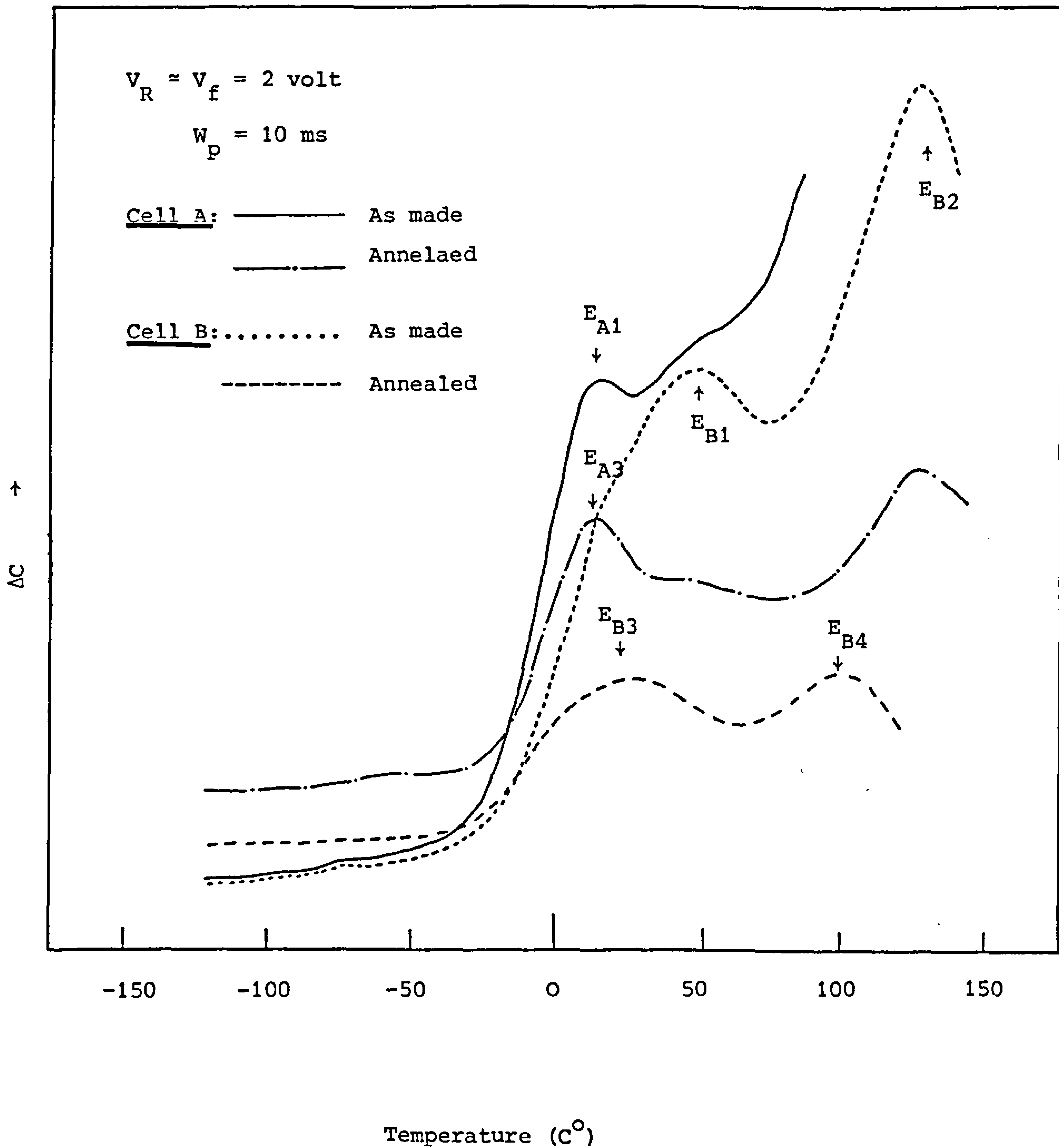


Figure (5-31) DLTS spectra before and after 10 mins. air annealing at 200°C for two $CdS-Cu_2S$ cells prepared using two different CdS electrical properties.

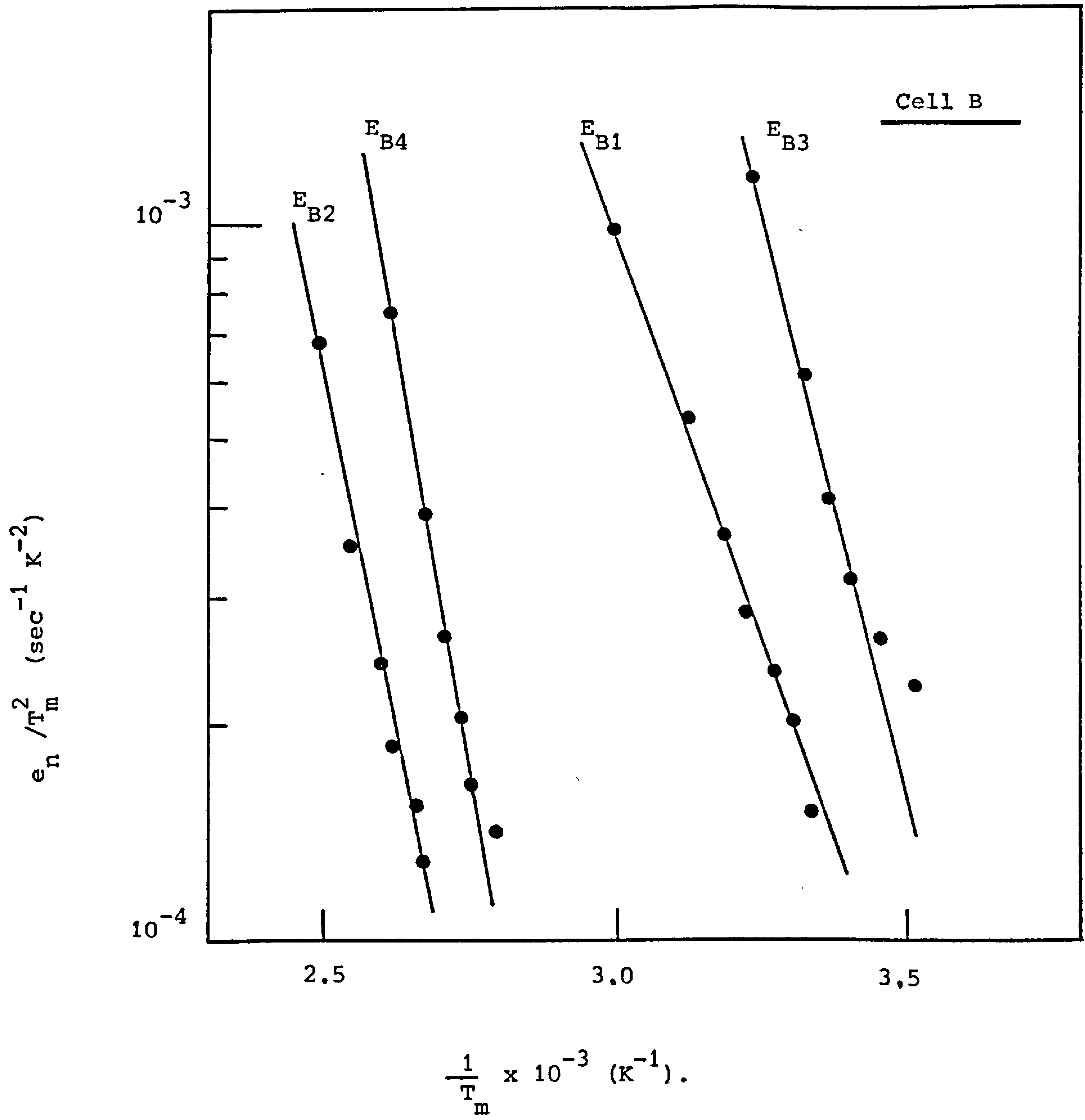


Figure (5-32) Arrhenius plot of emission rate of traps observed in Cell (B).

and the capture cross section (assumed to be temperature independent) can be calculated. The corresponding plots for cell B before and after annealing are shown in figure (5-32) and the results are listed in table (5-16).

The trap concentration N_T was calculated by the use of the expression [218]

$$N_T = 2N \frac{\Delta C}{C(v)} \left| 1 - \frac{2\lambda}{W(v)} \left(1 - \frac{C(v)}{C(o)}\right) - \left(\frac{C(v)}{C(o)}\right)^2 \right|^{-1} \qquad (5\text{-}6)$$

where N is the carrier concentration, ΔC is the change in capacitance at $t = 0$, C(V) and C(O) are the steady state capacitance with and without applied reverse bias respectively, W(V) is the width of the space charge layer with an applied reverse bias V, and λ is the width of the edge region of the depletion layer given by [218]

$$\lambda^2 = 2 \varepsilon \varepsilon_o \, (E_f - E_T) \,/\, e^2 N \qquad (5\text{-}7)$$

Here E_F is the Fermi energy and the other terms have their usual meaning. The traps E_{A1} and E_{A3} for cell (A) in figure (5-31) before and after annealing are found to have the same energy depth (0.62 eV), and capture cross section ($\sim 10^{-13}$ cm^2).

5.3. Cell diffusion processes and stability.

5.3.1. Introduction

It is obvious from the evidence presented in the earlier sections of this chapter that diffusion at the CdS-Cu_2S interface is influenced by the cell fabrication and post-fabrication processes. In order to study this aspect, Auger spectroscopy was employed (as described in section 4.8) to determine the compositional profiles and the effect on the profiles of different fabrication processes. This information was later correlated with the electrical characteristics of the cells.

TABLE (5-16). DLTS parameters for the electron traps observed in cell B before and after annealing treatment.

Before annealing treatment	E_T (eV)	σ_n (cm^2)	N_T (cm^{-3})	Temperature range (K)
E_{B1}	0.44	5.8×10^{-18}	6.5×10^{14}	300 - 330
E_{B2}	0.80	8.5×10^{-15}	-	370 - 400
After annealing treatment				
E_{B3}	0.65	6.0×10^{-14}	9.2×10^{14}	280 - 310
E_{B4}	0.94	2.4×10^{-12}	-	360 - 390

5.3.2. AES depth profiles for as-formed CdS-Cu_2S cells

A typical set of Cu, Cd and S concentration-depth profiles for a freshly fabricated cell is shown in figure (5-33). It is clearly possible to identify three distinct regions: (I) where the concentration of copper is nearly constant, (II) where this concentration falls sharply, and (III) at greater depth where the copper concentration falls more slowly.

Region I is assumed to be associated with the copper sulphide layer (approximately 80 nm thick in this case) covering the exposed surface of the CdS grains. The rapidly decreasing copper signal in region II is considered to be associated both with diffused copper in the upper surface layer of the CdS grains and with copper in the grain boundaries, while region III can be interpreted as being due solely to deep intrusions of copper sulphide along the grain boundaries. These deductions, which are more clearly illustrated in figure (5-34), are supported by the following three observations. Firstly, the cadmium-to-sulphur signal ratio saturates with increasing depth into the cell indicating the bulk CdS region. The observed intense copper signal at such depths within the

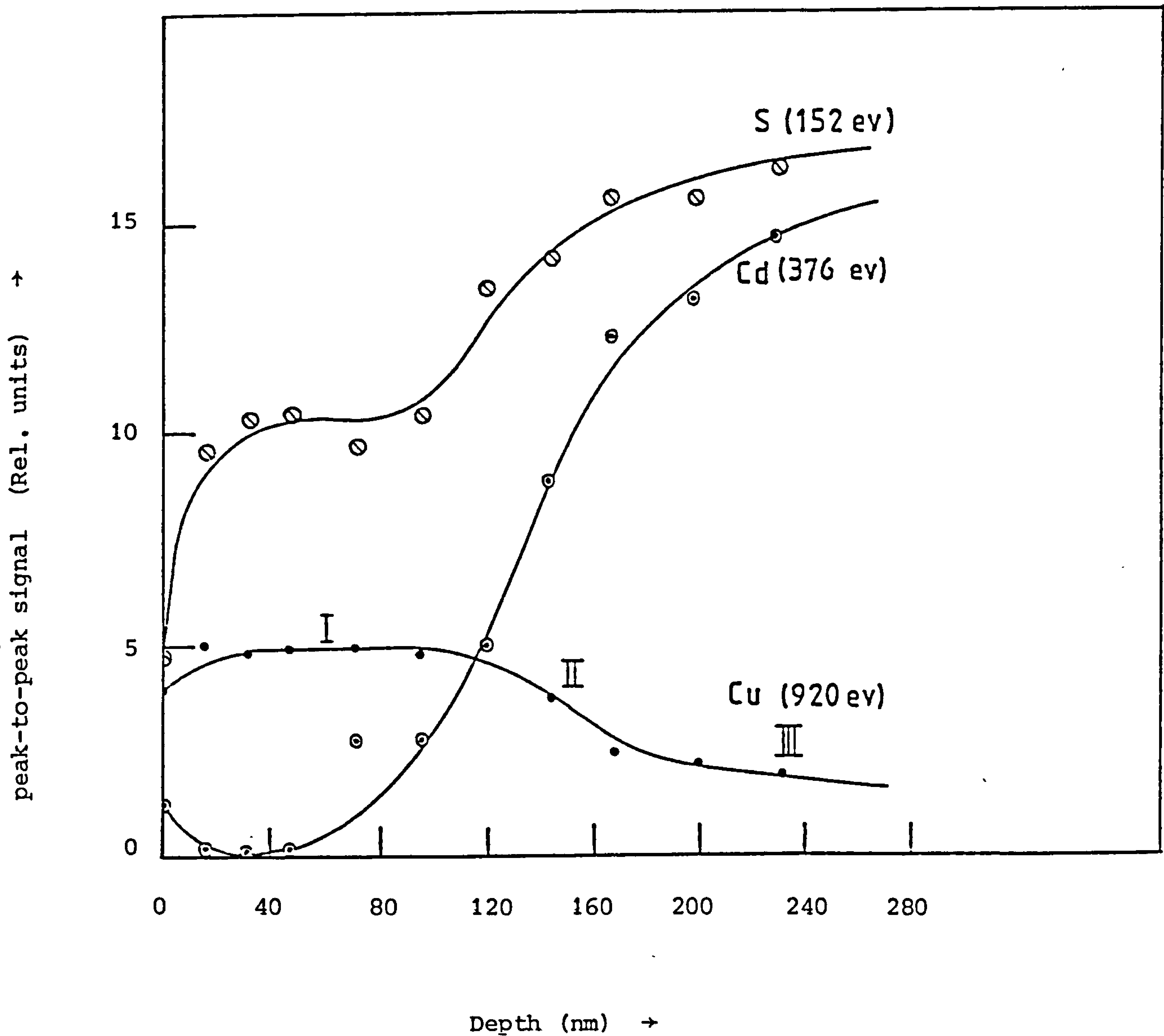


Figure (5-33) Auger electron spectroscopy depth profile of a $CdS-Cu_2S$ cell formed by dipping for 5 sec in CuCl solution at 98° C.

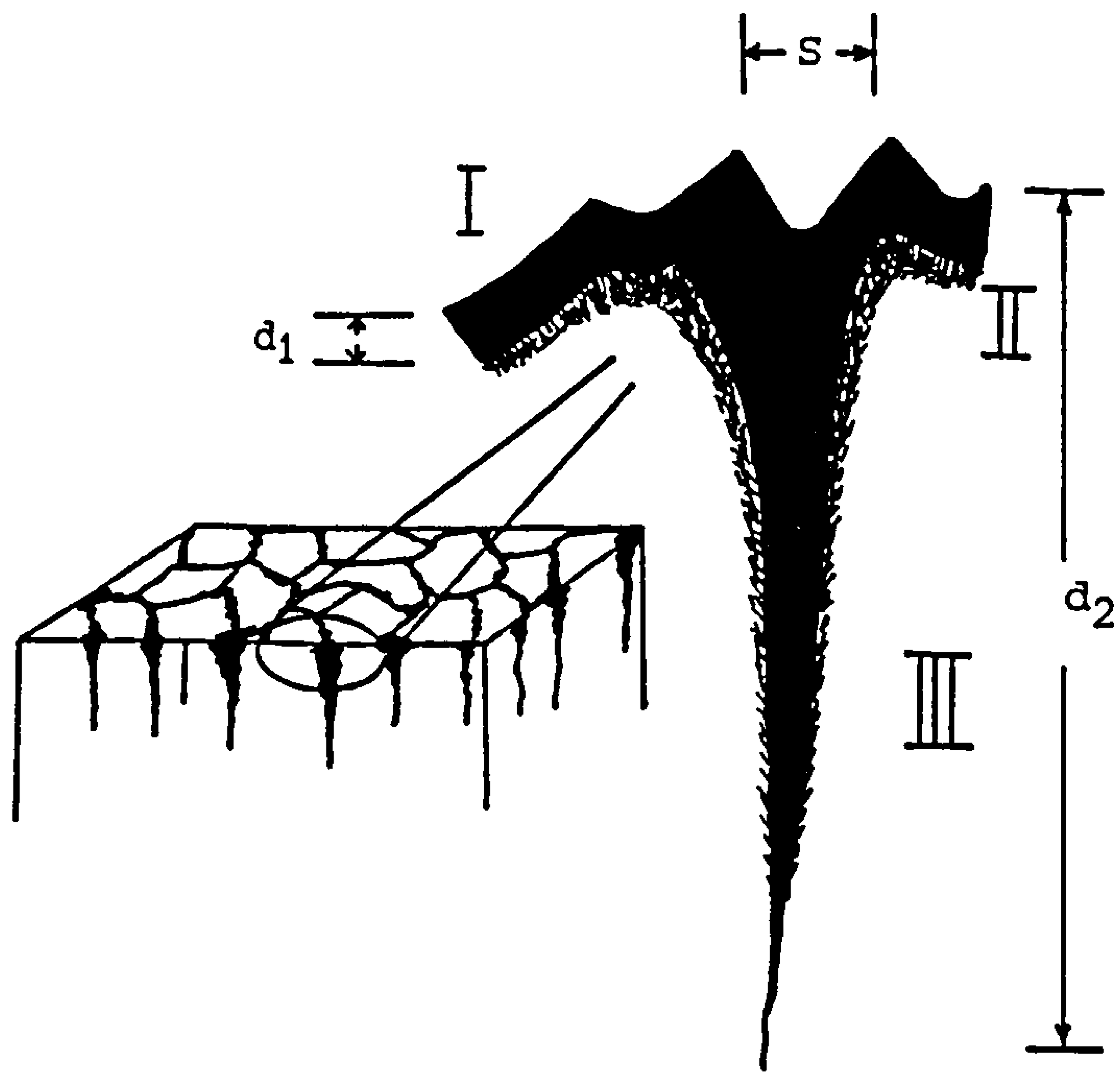


Figure (5-34) Schematic diagram shows the grain structure model in terms of which the copper profile in figure (5-33) is interpreted.

layer could only be associated with grain boundaries. Secondly, evaporated Cu_2S and/or single-crystal CdS heterojunctions are characterized (146-148) by abrupt concentration profiles of copper and cadmium in contrast with the trailing copper signal (region III) in cells fabricated from chemiplated copper sulphide and polycrystalline CdS. Thirdly, the grain boundary width S, measured from scanning electron microscope topography (Figure 5.5) of the layers on which the grain boundary has been revealed by leaching the Cu_2S from the cells with a KCN solution, was found to be approximately twice the mid grain thickness d_1 of the copper sulphide layer. For example, for the sample of figure (5-5) the boundary width S at the surface was found to be 170 nm. This corresponds to a maximum thickness of $d_1 = \frac{S}{2} = 85$ nm for the Cu_2S on the side surfaces of the adjacent grains bordering an intrusion, and this is consistent with the film thickness obtained from depth profile data.

5.3.3. Depth profiles for different chemiplating temperatures

In order to provide a further check on the validity of the above model, the profiles for cells produced using a range of CuCl bath temperatures were compared. Figure (5-35) shows the Auger electron spectroscopy copper profiles for cells prepared with CuCl bath temperatures in the range between 50-98°C. The ion exchange reaction was clearly rather slow at 50 and 75°C and resulted in a very thin copper sulphide film on the upper surface of the CdS grains and almost no growth within the grain boundaries. The dramatic change in concentration profiles at higher temperatures indicate the accelerated growth of the copper sulphide layer with extensive intergrain penetration as well as significant mid-grain growth.

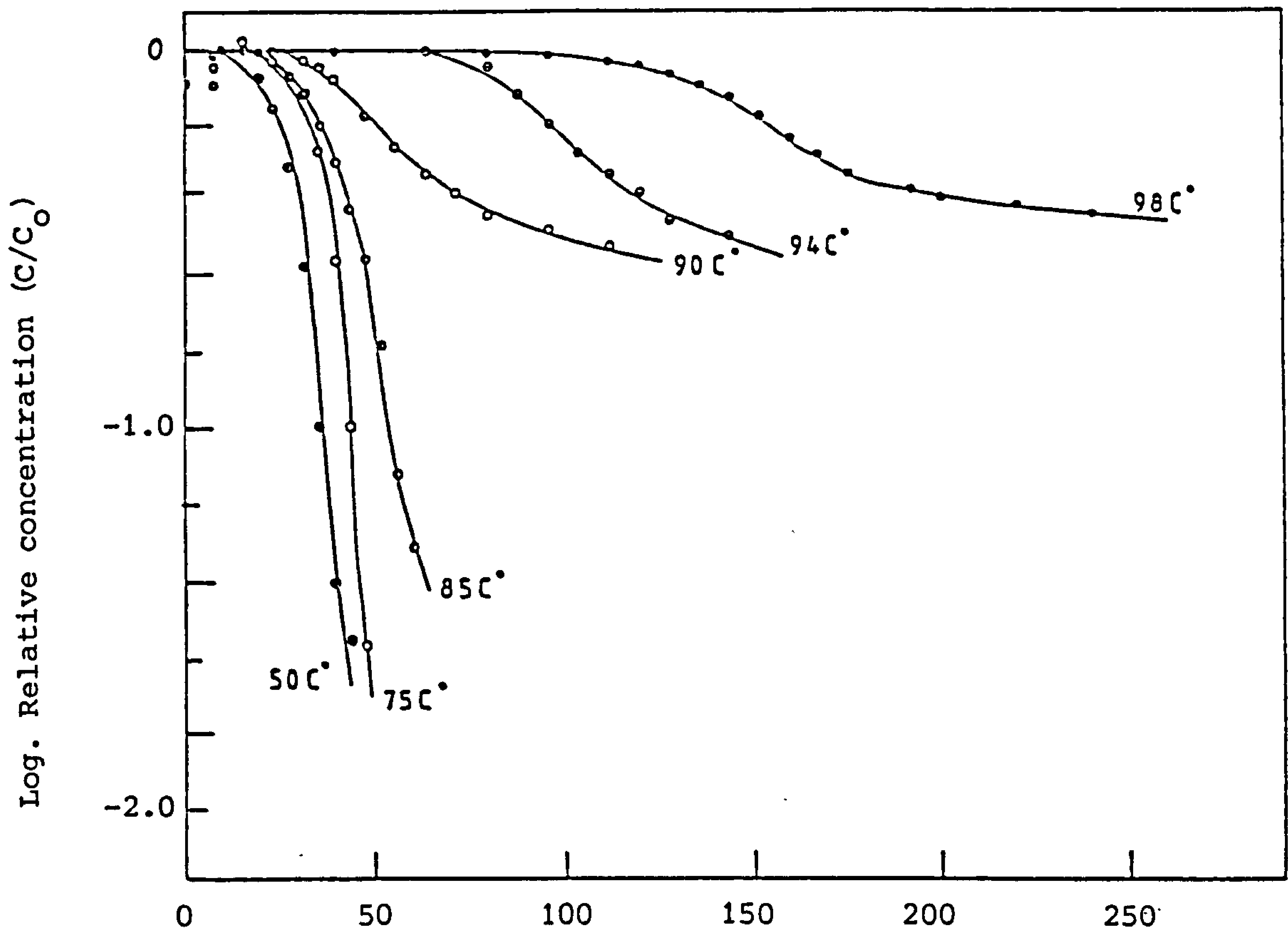


Figure (5-35) Auger electron spectroscopy copper profiles for cells produced with CuCl bath temperatures in the range 50-98°C (CuCl concentration, 14 gℓ^{-1}, diptime, 5 sec).

These results were confirmed by ECA experiments. These experiments yield an equivalent thickness $\bar{d}$ of the copper sulphide which is a function of both the mid-grain thickness d_1 and the grain boundary depth d_2 of copper sulphide. The data for d_1 from AES measurements and $\bar{d}$ obtained from the ECA experiments are displayed in figure (5-36), where both values are seen to increase rapidly for CuCl bath temperatures between 85 and 90°C. However, while the equivalent thickness $\bar{d}$ gives a measure of the total amount of copper present in the sample the AES profiling data yields more explicit information about the contributions of mid-grain and grain boundary growth.

It is interesting to note that some impurities, such as O, C and Cl, were found on the surface of these samples. The impurity peaks disappeared completely after a brief Ar^+ ion bombardment (less than 1 mins.). The presence of both Cd and Cl on the top surface indicates that $CdCl_2$ formed during the reaction is not fully washed away.

5.3.4. The effect of different annealing treatments on the copper and cadmium profiles

In order to study the effect of annealing on the composition profiles of the $CdS-Cu_2S$ heterojunctions, a batch of cells fabricated under identical conditions were subjected to a variety of different annealing treatments. The three ambient atmospheres widely employed for post-fabrication annealing processes are air, vacuum or hydrogen. As discussed previously, it is usual, in the case of air, to heat for only a few minutes at temperatures up to about 200°C whereas vacuum or hydrogen treatments require very much longer periods for optimal results. In this investigation, each cell was annealed for a period of 10 mins. at

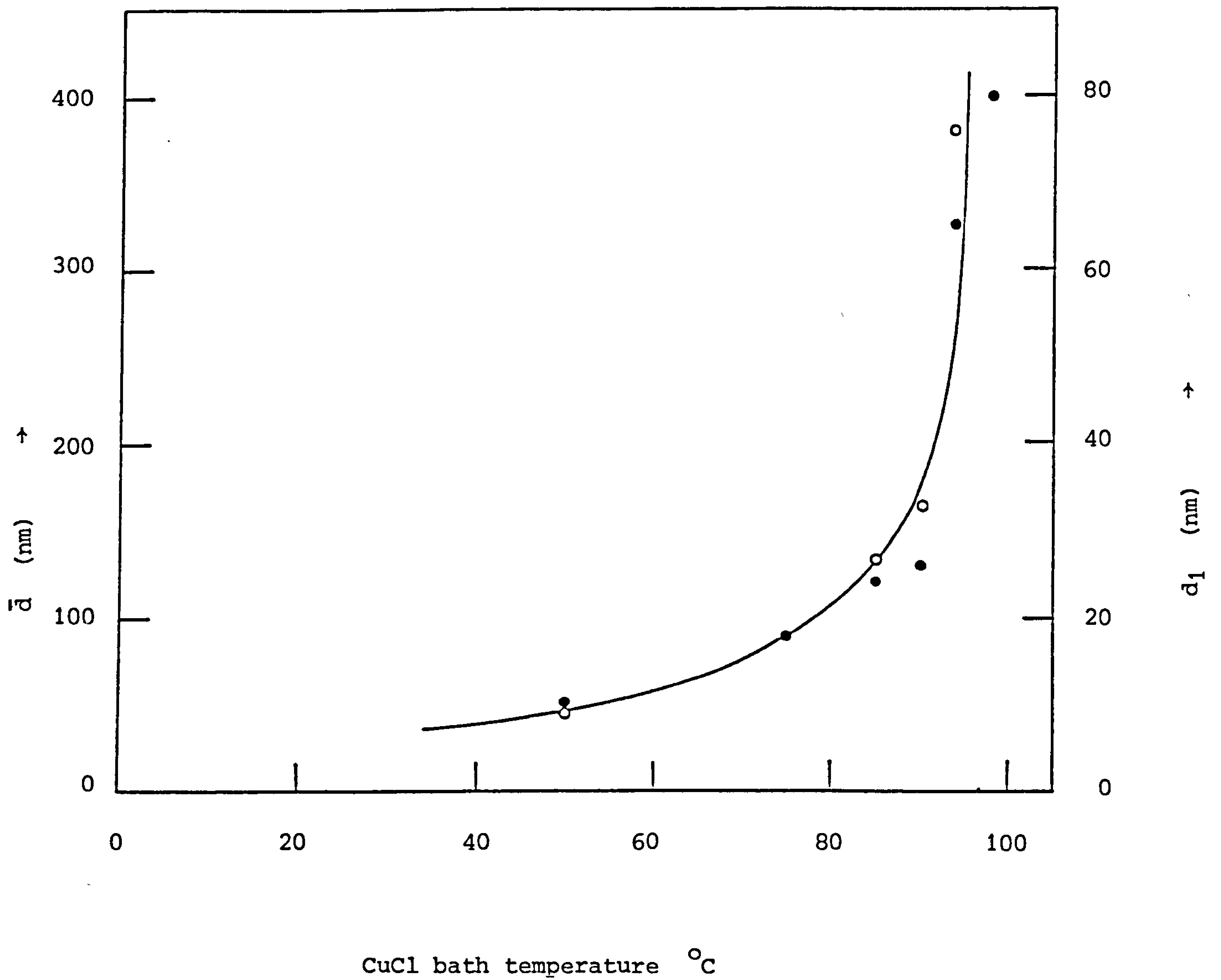


Figure (5-36) Copper sulphide equivalent thickness $\bar{d}$ (o) and mid-grain thickness d_1 (•) as functions of the CuCl bath temperature.

temperatures of 100, 200, 400 or 600°C in air, vacuum (10^{-5} torr) or flowing hydrogen (0.8 ℓ min^{-1}).

Some important differences between the effects of the three different annealing atmospheres could be clearly defined. In the first place, air-annealed cells were found to exhibit substantial concentrations of cadmium throughout the copper sulphide layer. Only as the temperature was raised to 600°C did significant out-diffusion of cadmium occur under vacuum or under hydrogen. Secondly, the relative concentration of copper found deep within the cells was highest for air-annealed cells and lowest for hydrogren-annealed cells but, as might be expected, with progressive increases in temperature the sharpness of the fall in copper concentration across the interface was progressively diminished in all cases.

Finally, the samples annealed in hydrogen were found to display lower surface concentrations of both sulphur and chlorine than those for samples annealed in air or vacuum, presumably as a result of chemical reduction and vaporization.

Figure (5-37) shows typical concentration profiles for copper in cells annealed for 10 mins. at 200°C. It is clear that, in comparison with the profile for an unannealed cell (Figure 5-33), some broadening of the junction has taken place and this is particularly significant in the case of air annealing. After heat treatments at 400°C, the disparity between the effects of air and the other two ambient atmospheres is even more dramatic, as can be seen in Figure (5-38). In this case, the diffuse nature of the profile for the air-annealed case makes it difficult to distinguish between a region II and a region III (section 5.3.2) and difficult therefore to identify the location of the interface between the copper sulphide and CdS layers of the cell. The compositional instability of the junction when it is annealed in air is further demonstrated by

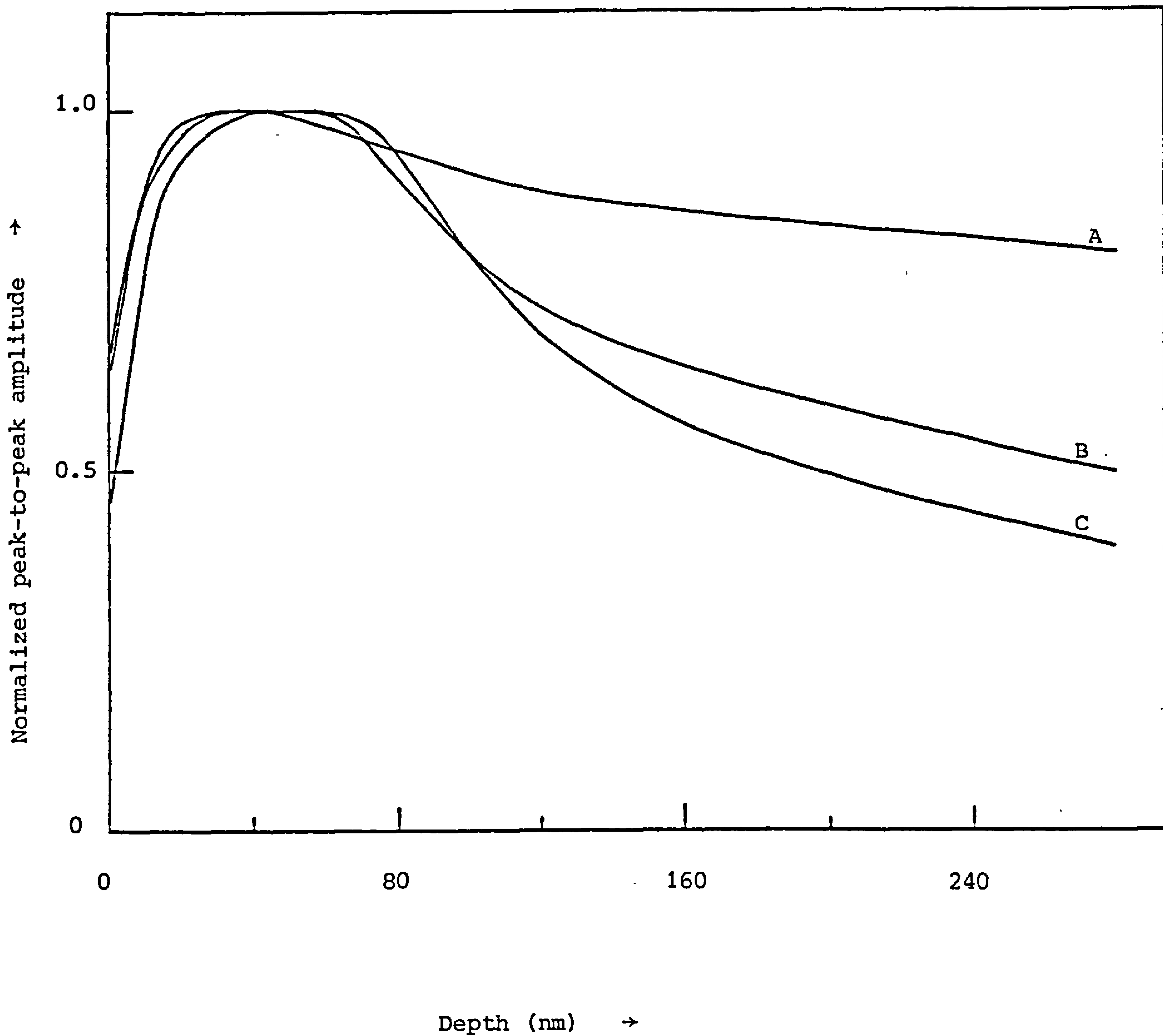


Figure (5-38) Auger electron spectroscopy copper profiles for a cell annealed for 10 mins. at 400°C in air (curve A), in vacuum (curve B) and in flowing hydrogen (curve C).

examination of the cadmium profile after different annealing treatments. Figure (5-39) shows such profiles for cells annealed for 10 mins. at 100° or 400°C. These results show clearly that a reasonably abrupt junction is maintained after annealing at 400°C in either vacuum or hydrogen (curves A and B). In contrast, annealing at 400°C in air is seen to result in significant out-diffusion of cadmium (curve D), and even after 10 mins. at 100°C a substantial cadmium concentration is detected throughout the Cu_2S layer (curve C). Only after heating to 600°C in vacuum or hydrogen was a significant concentration of cadmium detected in the Cu_2S layer.

5.3.5. Depth profile for CdS-Cu_xS Solar cells with a copper overlayer

Figure (5-40) shows a set of Auger depth profile measurements for a sample given the optimum treatment according to results discussed in section (5.2.4) (i.e. 100 Å thick layer of copper followed by 90 mins. annealing at 200°C in air). This result can be compared with profiles for an untreated cell (Figure 5-33) and a cell which had been annealed in air without a surface layer of copper (Figure 5-41). The copper oxide, copper sulphide and cadmium sulphide regions of the system are reasonably clearly distinguished in figure (5-40), with the copper signal showing its characteristics long tail due to the deep copper sulphide grain boundary intrusions. There is evidence of significant interdiffusion of oxygen and sulphur across the copper oxide-copper sulphide interface, but it is especially interesting to note that the CdS-Cu_2S interface, as marked by the Cd profile, is relatively abrupt. This result contrasts markedly with the effect of air-annealing on cells without a copper overlayer. For such cells as discussed above, cadmium diffuses across the CdS-Cu_2S boundary in

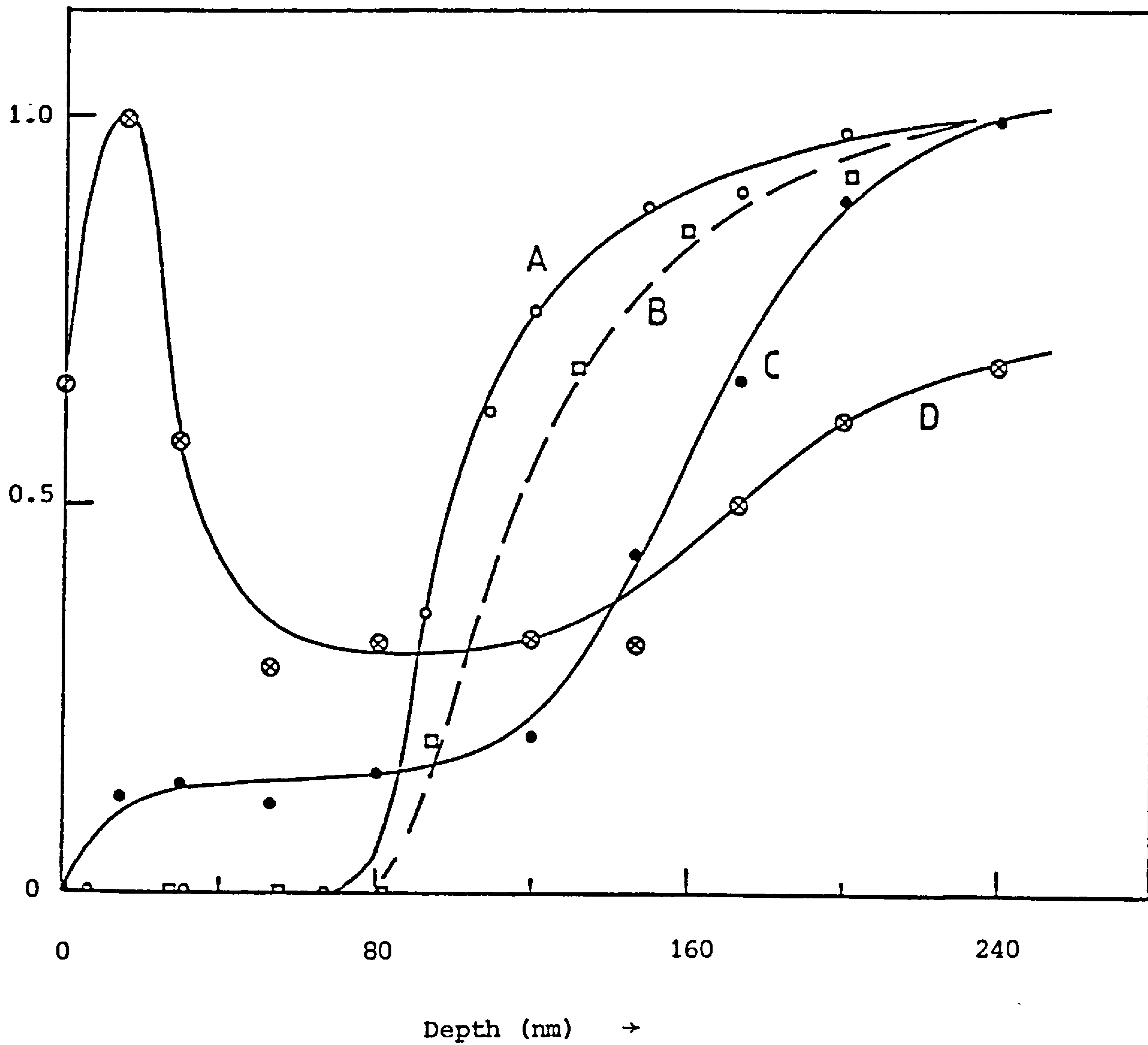


Figure (5-39) Auger electron spectroscopy Cadmium profiles for cells annealed for 10 mins. at 400°C in hydrogen (curve A) and in vacuum (curve B) and for 10 mins. in air at 100°C (curve C) and at 400°C (curve D).

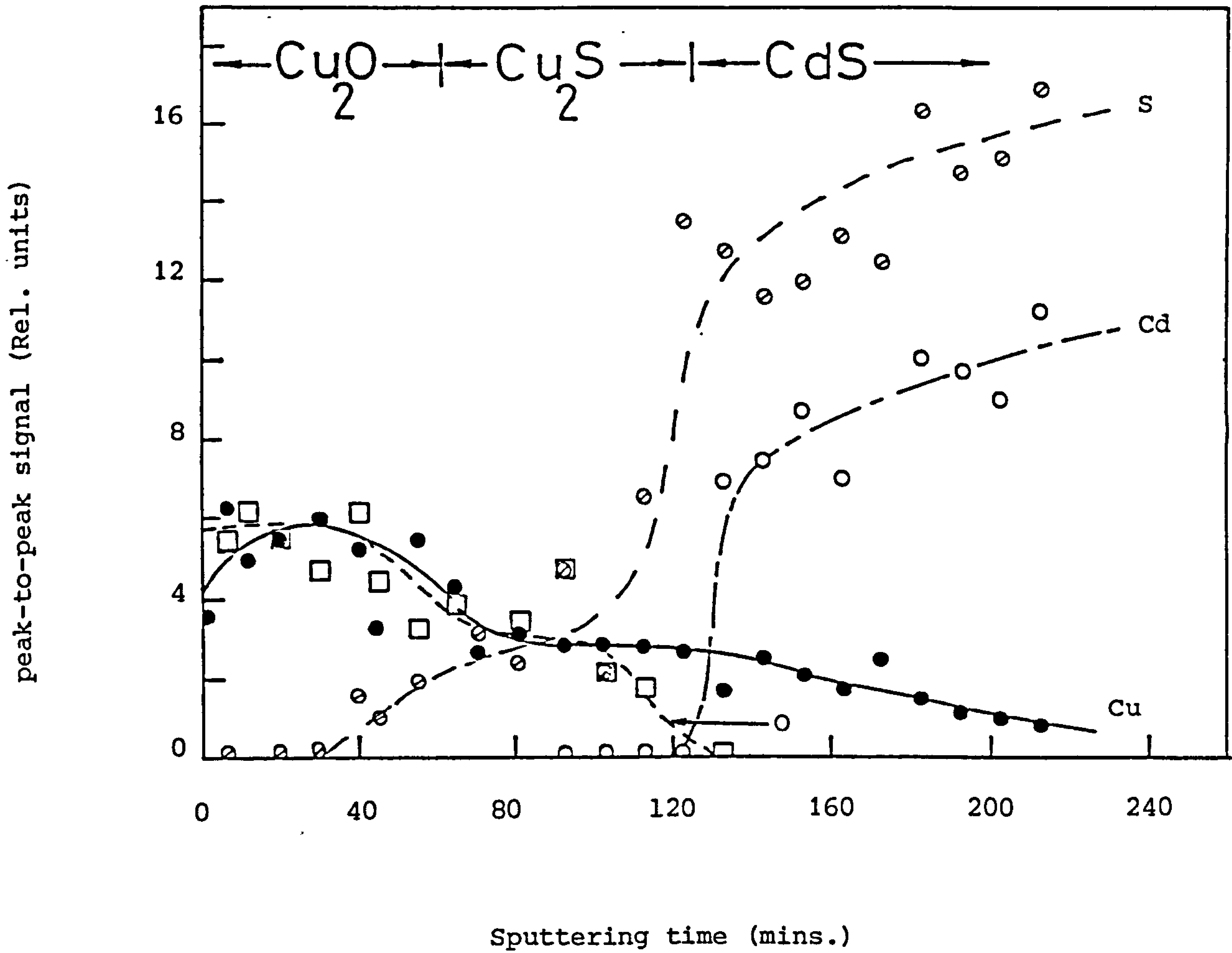


Figure (5-40) Auger electron spectroscopy depth profiles of Cu, Cd, S and O for a copper-coated cell after 90 mins. annealing at 200°C in air.

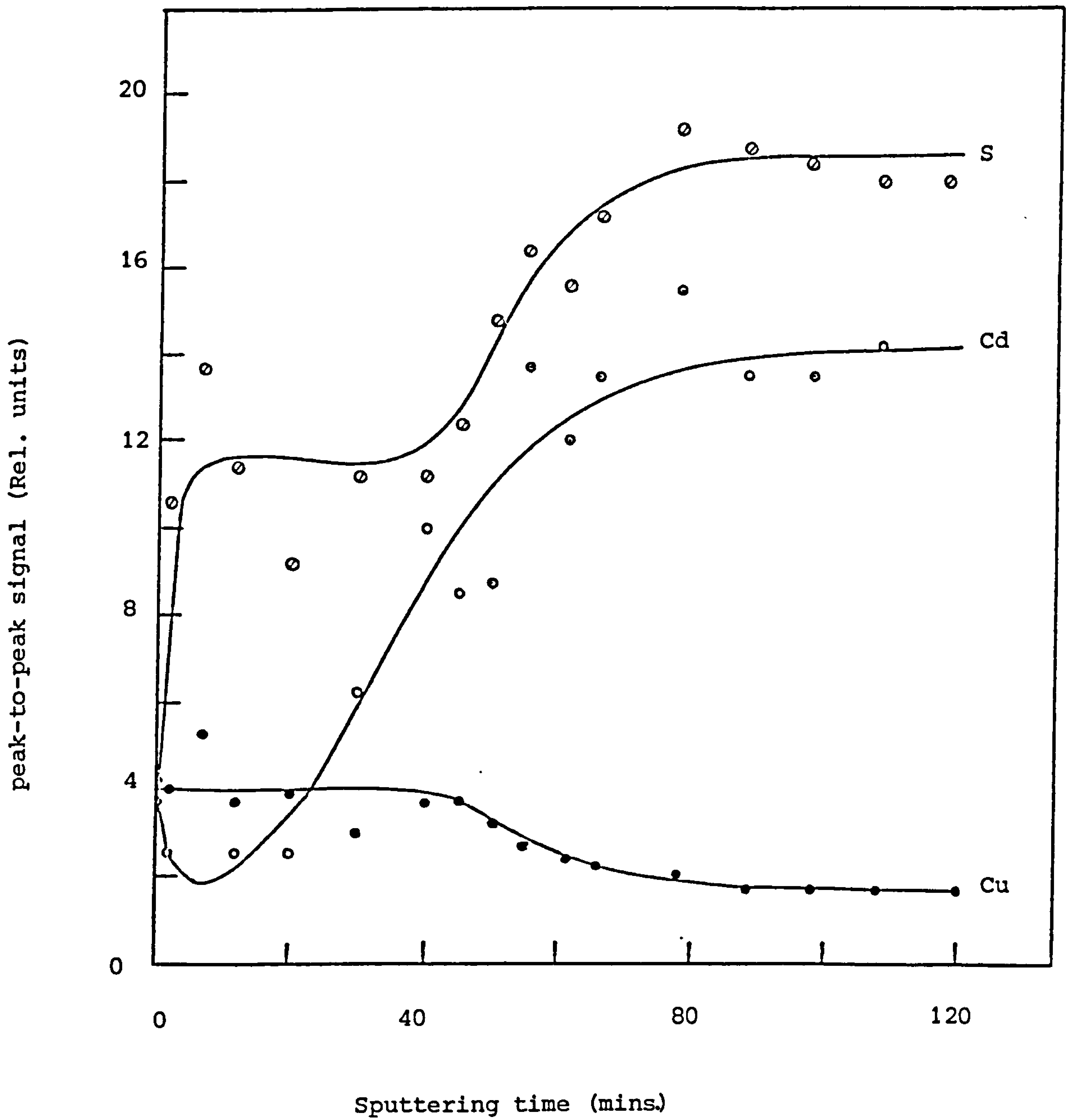


Figure (5-41) Auger electron spectroscopy depth profiles of Cu, Cd and S for a cell with no copper over layer, after annealing for 90 mins. at 200°C in air.

significant quantitites even for annealing conditions of much shorter duration and much lower temperature than those employed in the case of the copper coated cell.

5.3.6 Diffusion characteristics of copper in CdS films

As we have seen earlier, there is considerable penetration of copper into the CdS layer in both the grain and grain boundary regions. Clearly it is of technical (as well as general scientific) interest to study this diffusion process and also to estimate the diffusion coefficients of Cu in the grain and grain boundary regions of the CdS films during the annealing treatments under different annealing conditions.

In order to draw quantitative conclusions relating to these diffusion processes, it is necessary to separate the grain and grain boundary contributions to the total copper concentration across the depth profile. This can be done by identifying the three regions I, II and III referred to in section (5.3.2). For example, in figure (5-42) which shows results for samples annealed in vacuum at different annealing temperatures these 3 regions are fairly clearly distinguished. In general the copper concentrations at any depth within the CdS layer can be expressed as

$$C = C_g + C_{gb}$$

where C_g is the concentration in the upper, exposed regions of CdS grains and C_{gb} is the concentration within the grain boundaries. According to the grain structure model in section (5.3.2), C_g is zero within region III where the copper signal arises solely from copper in the grain boundaries. According to the analysis of Le Claire [192] the diffusion coefficient in the grain boundary, D_{gb}, can be found by determining the slope of log C_{gb} against $y^{6/5}$ (as discussed in section 3-6). Figure (5-43) shows the data

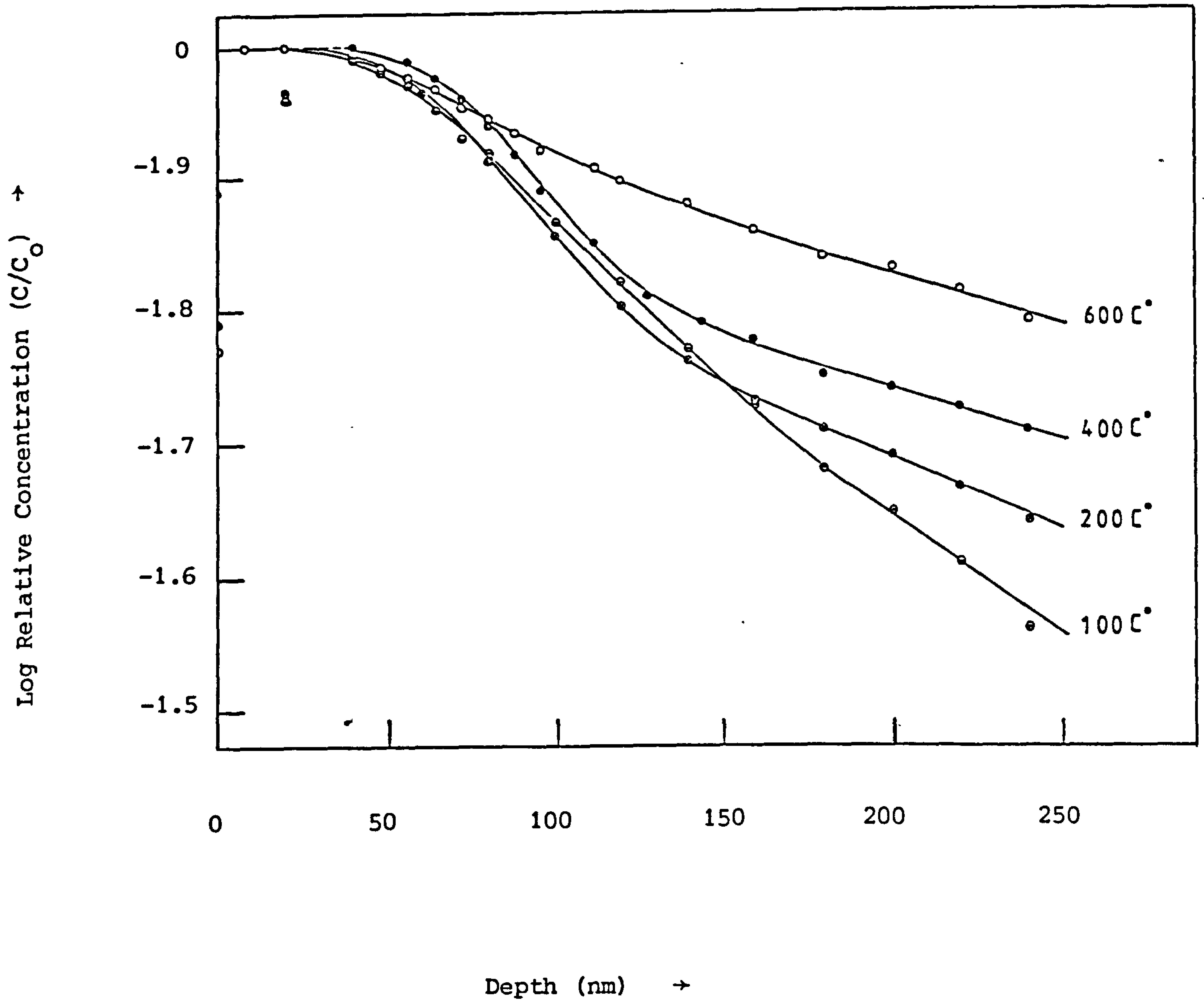


Figure (5-42) Auger electron spectroscopy for cells annealed in vacuum (10^{-5} torr) for 10 mins. at temperatures in the range 100°c - 600°c.

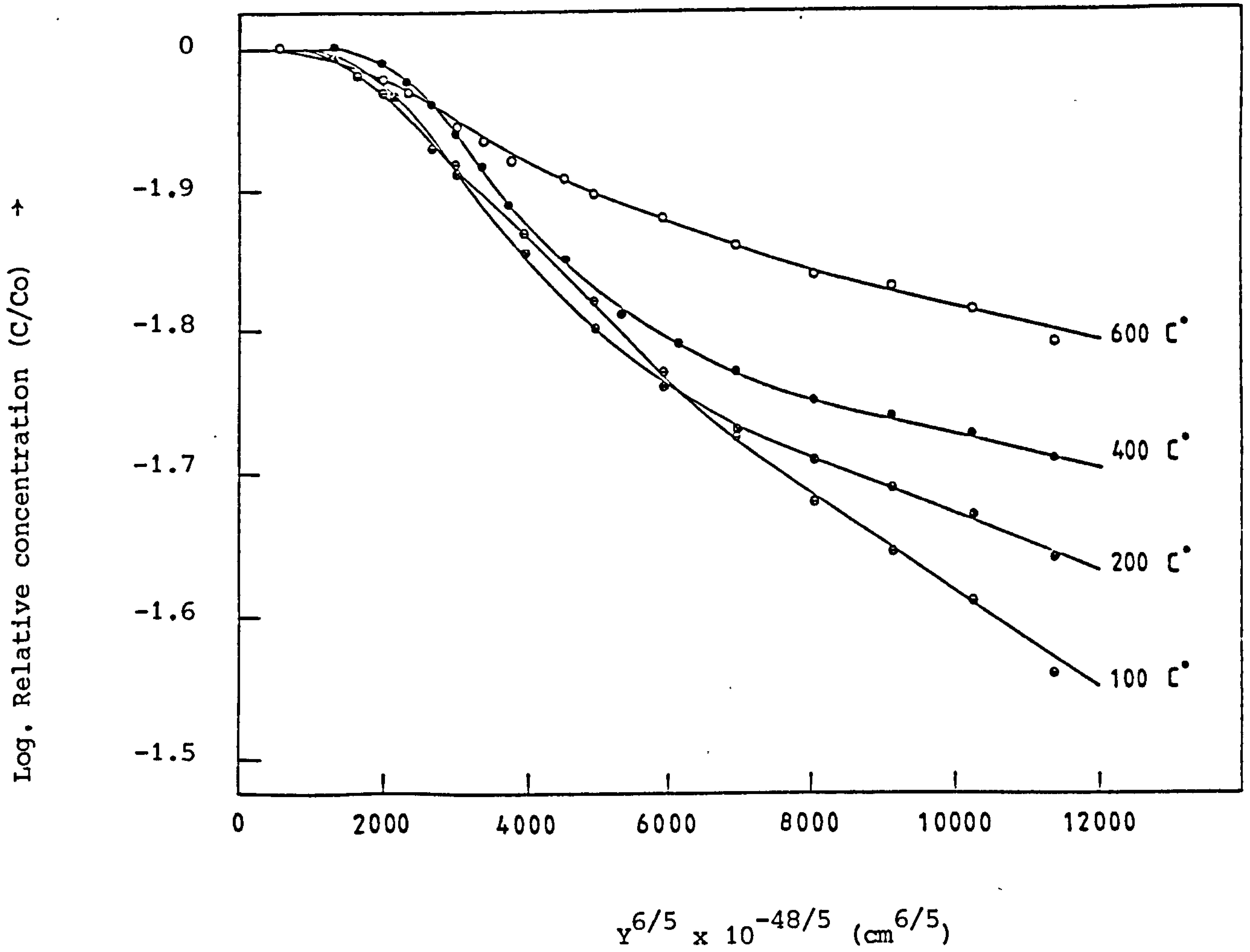


Figure (5-43) Copper concentration plotted as a function of $(\text{depth})^{6/5}$ for the data in figure (5-42).

of figure (5-42) plotted in this form allowing a value for D_{gb} to be calculated from the gradient of the linear tail region of each curve. These curves can also be used in the process of evaluating D_g by extrapolating the grain boundary concentrations C_{gb} in region III back into region II. Subsequently, by subtraction of the extrapolated C_{gb} values from the total observed concentration in region II, the distribution of copper as a function of depth into the grains can be determined. According to equation (3-52), a plot of log C_g against y^2 provides a measure of D_g. Such graphs do indeed yield relatively good straight lines as can be seen in figure (5-44), where in each case y is measured from the CdS-Cu_2S interface (taken to be at a depth of 80 nm). The calculated values of D_g and D_{gb} obtained by this procedure for each of the different annealing conditions are summarised in table (5-17). These values are found to increase with temperature, as would be expected and, from the slopes of the corresponding Arrhenius plots, the calculated activation energies, listed in table (5-17), were obtained. Except in the case of grain boundary diffusion under vacuum these activation energies are subject to rather large errors. As would be expected, the experimental errors associated with the D_{gb} are smaller than those for D_g values due to the additional uncertainty introduced by the extrapolation procedure required in the calculation of D_g.

5.4 Long term stability

While some diffusion of copper from the copper sulphide layer into the CdS is necessary in order to improve the efficiency of a freshly prepared cell, further uncontrolled interdiffusion across this interface leads to degradation of the cell characteristics. In addition to the

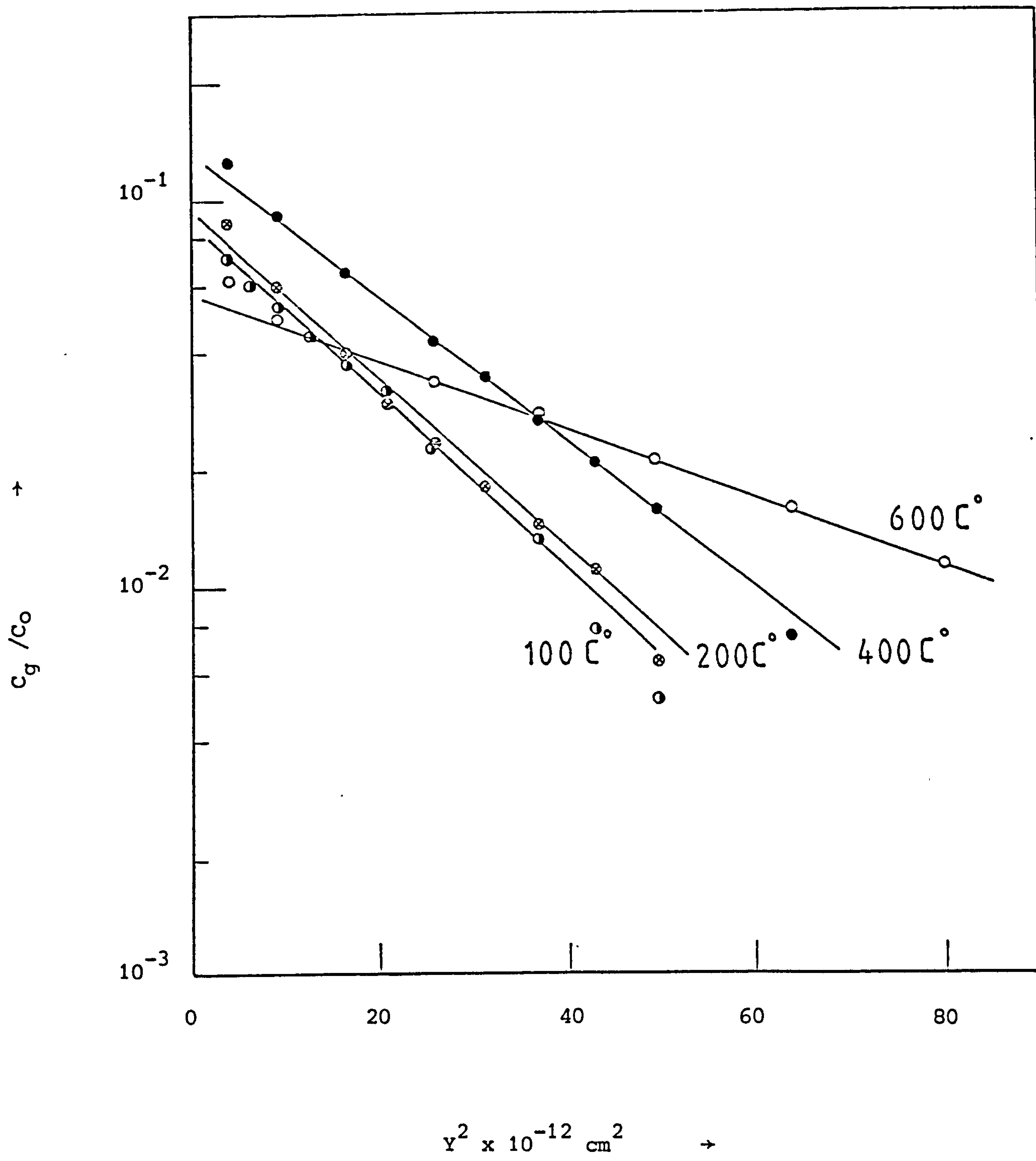


Figure (5-44) Mid-grain concentration of C_g as a function of $(depth)^2$ derived from the data in figure (5-42).

TABLE (5-17). Copper diffusion parameters for polycrystalline $CdS:Cu_2S$ cells under various ambient conditions.

Ambient		Temperature				Activation
atmosphere	Parameter	100°C	200°C	400°C	600°C	energy
10^{-5} torr	D_g cm^2 sec^{-1}	$7.8.10^{-15}$	$8.2.10^{-15}$	$9.6.10^{-14}$	$2.1.10^{-14}$	.05±.03 eV
	D_{gb} cm^2 sec^{-1}	$8.3.10^{-13}$	$1.8.10^{-12}$	$3.6.10^{-12}$	$7.0.10^{-12}$	.11±.01 eV
Air	D_g cm^2 sec^{-1}	$4.4.10^{-15}$	$5.0.10^{-15}$	$6.4.10^{-15}$	$2.0.10^{-14}$	.07±.04 eV
	D_{gb} cm^2 sec^{-1}	$3.3.10^{-12}$	$4.2.10^{-12}$	$2.3.10^{-11}$	$2.0.10^{-10}$	.22±.06 eV
H_2	D_g cm^2 sec^{-1}	—	$9.1.10^{-15}$	$1.1.10^{-14}$	$1.7.10^{-14}$	.05±.03 eV
(0.8 l m^{-1})	D_{gb} cm^2 sec^{-1}	—	$1.2.10^{-12}$	$3.0.10^{-12}$	$2.0.10^{-11}$	.23±.09 eV

effect of the ambient atmosphere, one of the factors which is expected to influence the rate of interdiffusion at the CdS-Cu_2S interface is the stoichiometry of the constituent phases. In order to investigate the significance of this particular factor, cells were constructed using different fabrication conditions and the subsequent degradation was followed by monitoring the short-circuit current or the Cu_xS stoichiometry (using a set of cells prepared under identical conditions). For example, figure (5-45) shows the reduction in X as a function of time for 3 cells. Cell (a) had a copper over layer (~ 100 Å) and was annealed in air for 90 mins., cell (b) was made in the conventional way using a CdS film similar to that in cell (a), and cell (c) had a graded CdS base layer (achieved by reducing the rate of sublimation during deposition of the CdS layer) so that the near junction region was nearer to the stoichiometric composition than the bulk of the layer which, like that in conventionally constructed cells was slightly Cd-rich in order to provide the required high conductivity base for the device.

The etching and the dipping procedures were the same for all three cells but cells (b) and (c) were annealed in hydrogen for 20 mins. at 200°C. As can be seen in figure (5-45), the stoichiometry of the copper sulphide layer in cell (c) is clearly more stable than cell (b), but not so stable as the cell (a) which had the copper oxide over layer. Other observations made during the course of this investigation have indicated that the degradation rate of the Cu_xS stoichiometry is further increased if the CdS layer has a significantly lower electrical resistivity than that used for cell (b).

Corresponding results for the stability of the short-circuit current for cells produced by the same three fabrication procedures are shown in figure (5-46). As expected, the variations in behaviour between

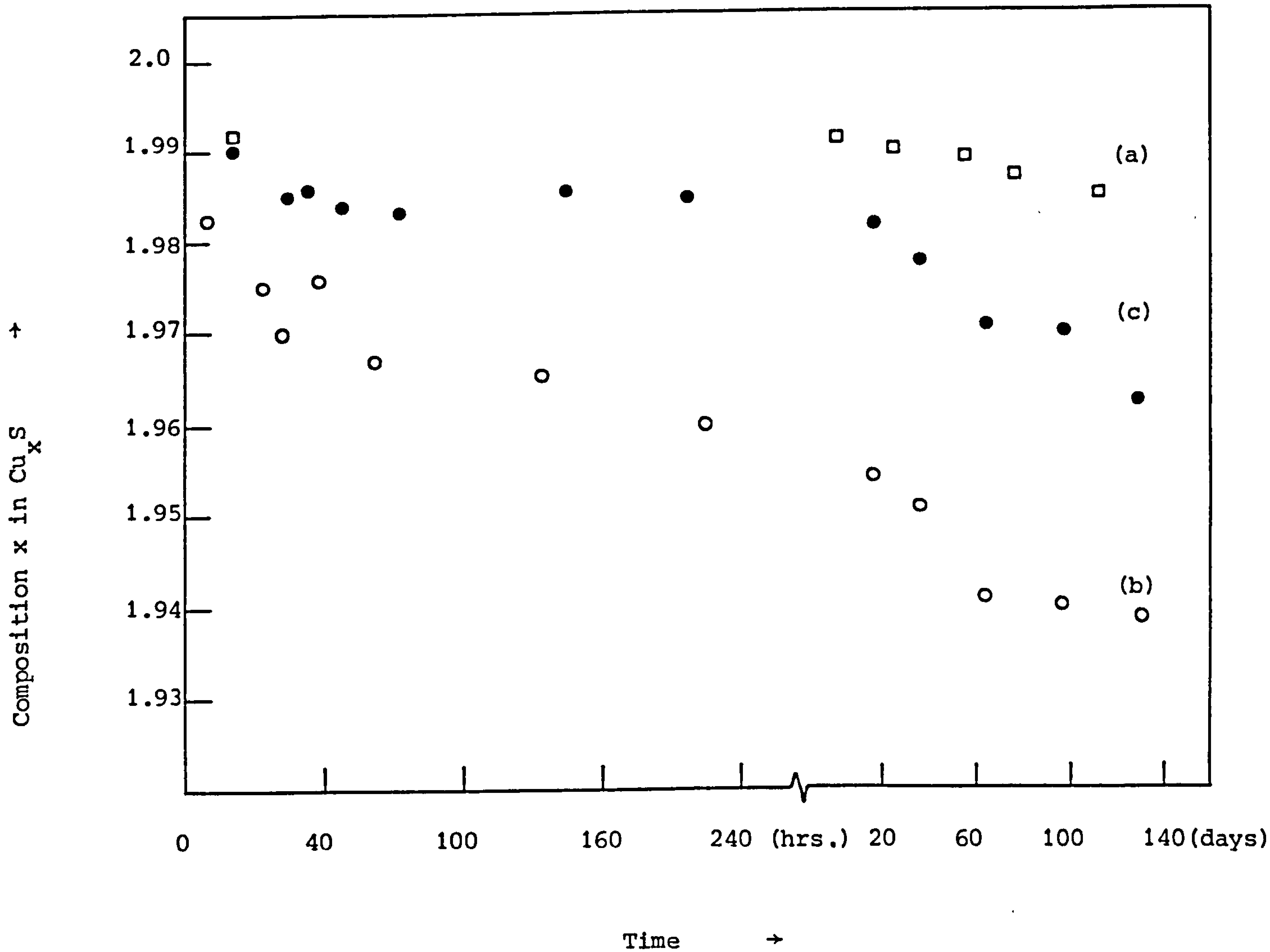


Figure (5-45) Composition x in Cu_xS as a function of time for 3 unencapsulated cells left in air at room temperature. (a) copper coated cell ; (b) conventional cell and (c) cell with graded CdS layer.

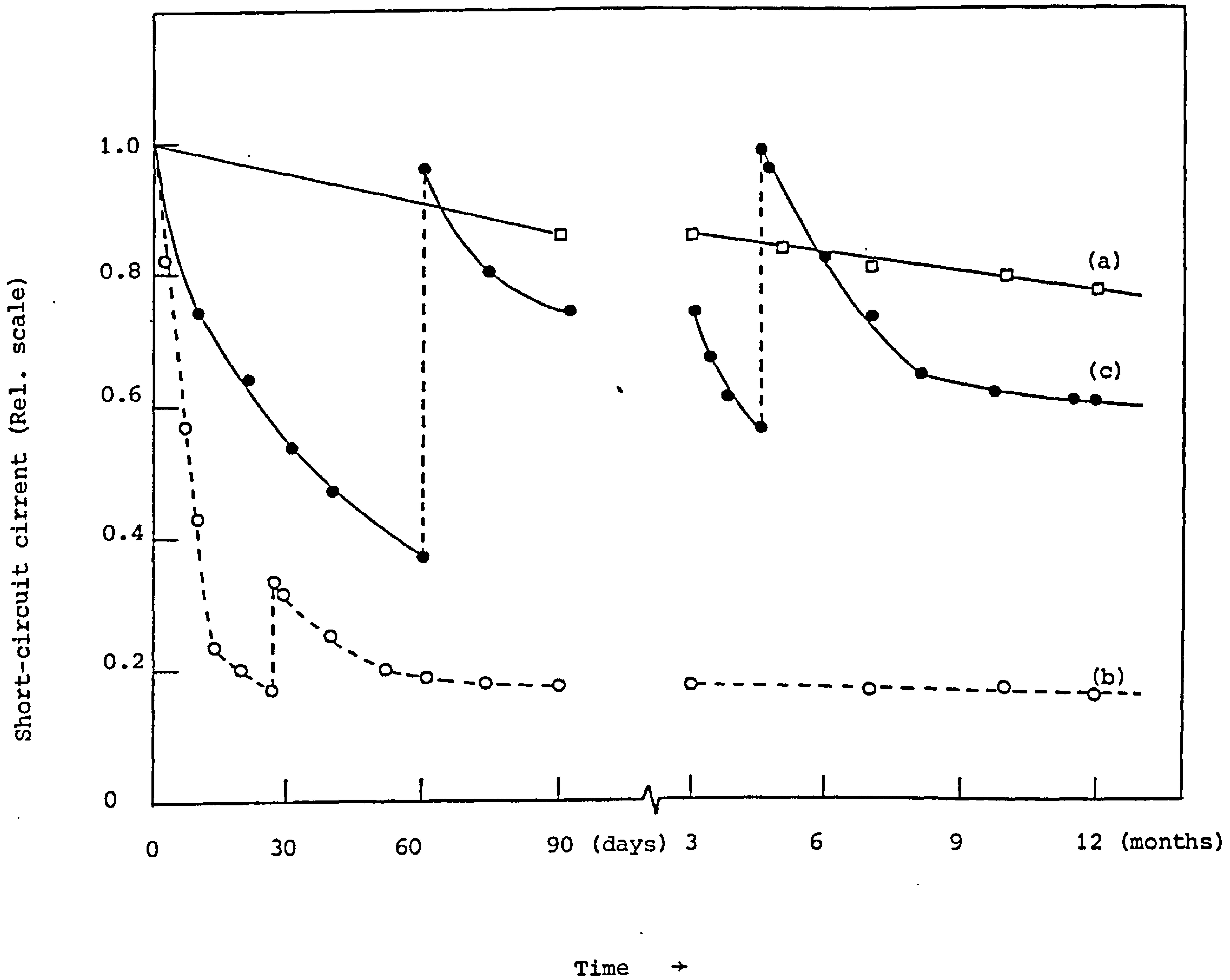


Figure (5-46) Ageing effects for 3 unencapsulated cells in air at room temperature. Point symbols as in figure (5-45).

the 3 different cells during the initial decay periods resembled very closely the form seen in figure (5-45). The irregular saw-tooth features are due to annealing cycles designed to reverse the degradation process as discussed below.

As the cells were unencapsulated and stored in air it was expected that, even in the absence of any interdiffusion processes occurring at the cell interface, the cell efficiency would diminish as a result of oxidation at the front surface and the consequent loss of copper from the copper sulphide. In fact, as is shown in figure (5-46) after 60 d. in air annealing cell (c) in hydrogen for 90 mins. at 200°C restored the short-circuit current to a value close to its initial level. A similar restoration was achieved for the same cell after 136 days, while for cell (b) it was found that hydrogen annealing, at best, leads to only a partial recovery of the initial characteristics. The open-circuit voltage degradation rate, like the photocurrent, was much slower in cell (c) than in cell (b) and, in the case of cell (a), there was no change at all in the open-circuit voltage value after 90 days. Once again the annealing treatment in hydrogen was found to restore the open-circuit voltage for cell (c) to its initial value, but for cell (b) only a slight improvement was obtained.

5.5 The effect of copper ion implantation of CdS thin films

It has been seen previously that diffusion of copper into the upper region of the CdS layer in a CdS-Cu_2S cell is a necessary process in the formation of a high efficiency device. The results in section (5.4) showed that cells fabricated with a graded CdS layer can produce more

stable cells than those having an initially uniform low resistivity CdS film. Cells made using uniform high resistivity CdS layers have a high open-circuit voltage but these cells suffer from the high series resistance associated with the high resistivity CdS layer. Although this problem is avoided to some extent by using a graded CdS film, the final thickness of the high resistivity layer is difficult to control, being dependent on the CdS evaporation process as well as the subsequent HCl etch and copper sulphide plating process.

As an alternative means of establishing the required doping profile, consideration was given to the use of ion implantation. This technique allows great control of both depth and density of doping. It is now widely used in the semiconductor industry and has been successfully used for doping various II-VI semiconductor materials [227].

In order to establish the feasibility of employing this technique for thin film $CdS-Cu_2S$ cells, a short investigation was carried out using monoenergetic copper ions with energy in the range 50-250 keV. The ion implantation was performed on a low resistivity CdS film (0.1 Ω cm) which was first etched in cold concentrated HCl acid for 5 sec. Although some other acceptor-producing dopant might have been used, copper ions (Cu^+) were employed to allow greater comparability of the implanted cell with a conventional cell and also it was considered that the presence of copper in the CdS layer would inhibit the copper sulphide stoichiometry from being degraded by further loss of Cu during the subsequent processing of the cell.

5.5.1. Copper ion implantation at a constant ion energy

To monitor the effect of implanted ions in relation to the damage

caused by the implantation, cathodoluminescence emission measurements were made before and after subsequent annealing treatment of the CdS films. Figure (5-47) shows the cathodoluminescence emission spectrum for an unimplanted film (sample A) and for films implanted with 50 keV copper ions at fluences ranging from 10^{14} to 10^{16} ions cm^{-2} (sample B-F). All the measurements were made at 77K. As already mentioned in section (5.1.1.b), the cathodoluminescence emission spectrum for unimplanted CdS films in figure (5-47) has three peaks a, b and c with a broad infrared emission shoulder over the range from 680 nm to 800 nm. It is clear from figure (5-47) that the cathodoluminescence intensity of all peaks a, b, and c decrease as the ion fluence increases, while a peak developed at about 710 nm.

As the damage which accompanies ion implantation needs to be annealed, the samples in figure (5-47) were annealed in vacuum (~ 10^{-5} torr) for 30 mins. at $300^{o}C$, and the cathodoluminescence emission spectra for the corresponding annealed samples is shown in figure (5-48). As a result of this annealing some partial recovery of the peaks a and c was observed, while the edge emission peak (peak b) diminished, especially for samples implanted using relatively higher ion fluences (samples E and F). It is clear in figure (5-48) that the peak at 710 nm (peak d) is removed by the annealing, while for sample E and F a new peak at about 750 nm developed (peak e).

Independent methods were used to distinguish whether the peaks d and e were due to copper implantation or to the damage which occurred during the ion implantation process. An experiment was carried out using four CdS layers obtained from the same CdS evaporation cycle. Two of the layers were implanted with fluences of 5 x 10^{14} and 10^{16} Ar^{+} ions cm^{-2} at 50 keV ion energy. A thin film of copper (~200 Å) was evaporated on the

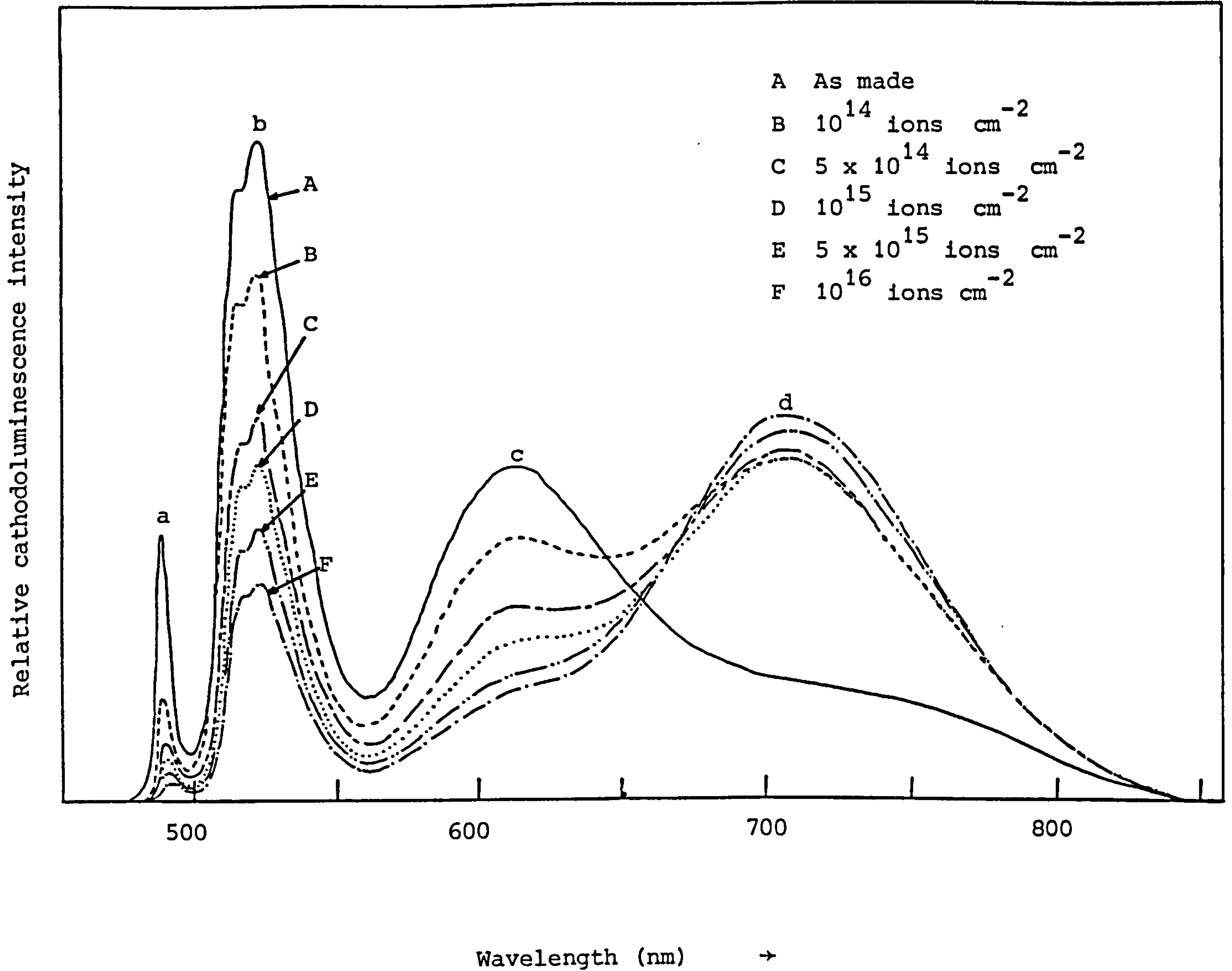


Figure (5-47) Cathodoluminescence emission spectrum of CdS thin films implanted with 50 KeV copper ions at ion fluences ranging from 10^{14} to 10^{16} ions cm^{-2}.

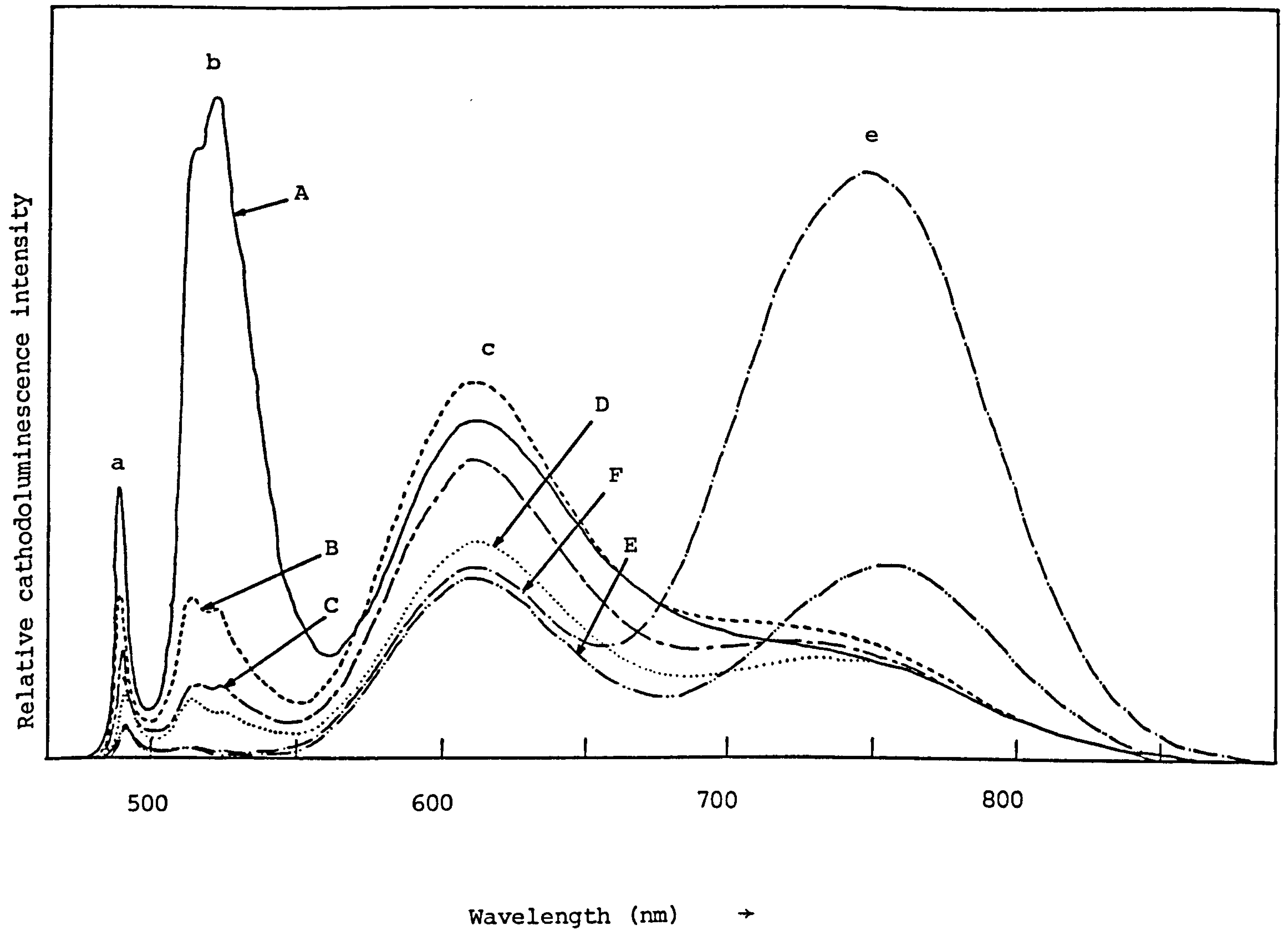


Figure (5-48) Cathodoluminescence emission spectrum for the same samples in figure (5-47) after 30 mins. vacuum annealing at 300°C.

final CdS layer followed by an annealing in vacuum for 30 mins. at 300°C. The cathodoluminescence emission spectrum of these samples is shown in figure (5-49). As can be seen the peak at 710 nm, (peak d) is only obtained after the Ar^+ ion implantation as a result of ion damage, while the peak at 750 nm (peak e) is found for the copper treated CdS layer.

To study the effect of copper ion implantation on the electrical properties, the copper implanted samples were dipped in CuCl for 6 sec and annealed in vacuum for 20 mins. at 200°C. From the I-V measurement at AMI light intensity, the values of the open-circuit voltage, V_{OC}, the short-circuit current, J_{SC}, and the conversion efficiency, η, are obtained and listed in table (5-18). The other characteristics listed in table 5.18 were obtained using similar CdS layers with the same ion implantation and subsequent annealing treatments as used for the original samples (samples A-F). The resistance and the capacitance values were obtained by evaporating a dot of In and Au respectively. It was found that the Schottky capacitance values for samples which had been ion implanted with copper ions were light dependent and therefore the listed capacitance values were taken in the dark. The equivalent thickness $\bar{d}$ and the values of x in the Cu_xS layers were obtained after the above samples had been dipped in the standard CuCl solution and annealed in vacuum. It is interesting to note that, although all the samples were dipped using the same standard CuCl solution and the same time (6 sec) the results in table (5-18) show that, as the copper ion fluence was increased, the stoichiometry of the copper sulphide layer improved while its equivalent thickness diminished. At the same time there was a gradual improvement in V_{OC}, while the short-circuit current had a maximum value of 18.2 mA cm^{-2} for a CdS layer implanted with 5 x 10^{14} ions cm^{-2}. This cell, correspondingly, gave the highest conversion efficiency value for this set

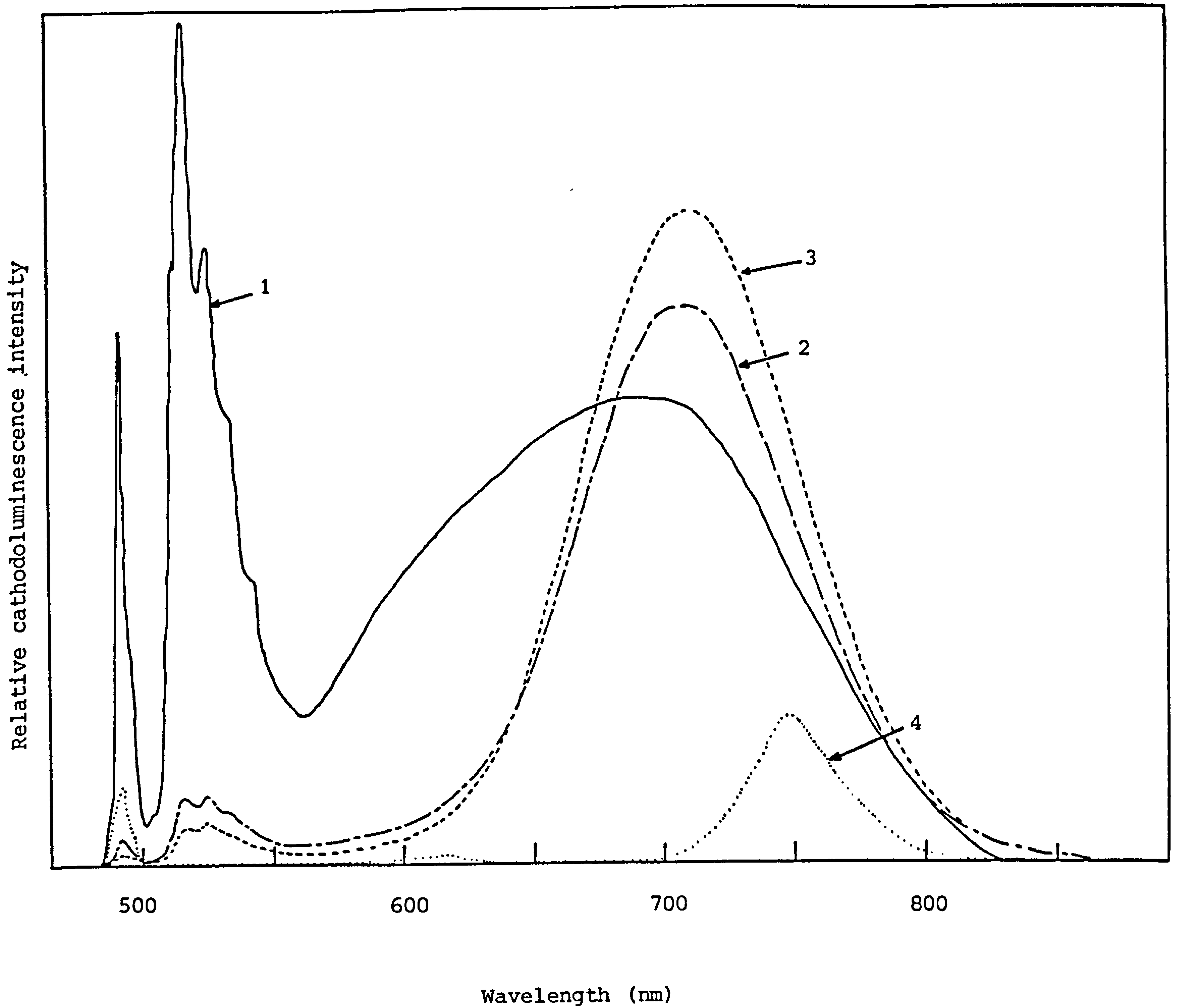


Figure (5-49) Cathodoluminescence emission spectrum of CdS films.
(1) before any treatment, (2) and (3) after Ar^+ ion implantation with $5x10^{14}$ and 10^{16} ions cm^{-2} at 50 KeV and (4) after evaporating a Copper overlayer onto the CdS and annealing in vacuum for 30 mins. at 300^oC.

of samples.

5.5.2. Copper ion implantation at a constant ion fluence

From the above results for 50 keV ion energy, the best efficiency was achieved when the ion fluence was 5 x 10^{14} ions cm^{-2}. Therefore this was the flux used to study the effect of ion energy. CdS films similar to those used in the previous study were first etched and then implanted with copper ions with energies of 100, 150, 200 and 250 keV.

Figure (5-50) shows the cathodoluminescence emission spectrum for these layers at 77K. Curve A is obtained for unimplanted CdS layer. The peaks are found at the same wavelengths as already seen for sample (A) in figure (5-47). After copper ion implantation, the intensity of the three main peaks is seen to reduce as the ion energy increases in a similar way to that obtained in figure (5-47) where the ion fluence was varied. It is clear that a peak at 710 nm (peak d) is again formed as a result of the implantation damage and the cathodoluminescence intensity of this peak is increasing, as expected, with increasing ion energy. It is also noted that there is a slight shift of this peak towards shorter wavelength as the ion energy increases.

Figure (5-51) shows the cathodoluminescence emission spectrum after the implanted CdS layers are annealed for 30 mins. at 300°C in vacuum. The edge emission peak (peak b) appears to be eliminated for all the samples in this figure, while the peak (a) has recovered especially for samples B' and C' which are implanted respectively at 100 and 150 keV ion energy. For peak (c) only a partial recovery is observed for sample B'. It is clear that peak (d) is diminishing after annealing treatment and for samples B' and C' the curves in figure (5-51) show a peak at about 750 nm,

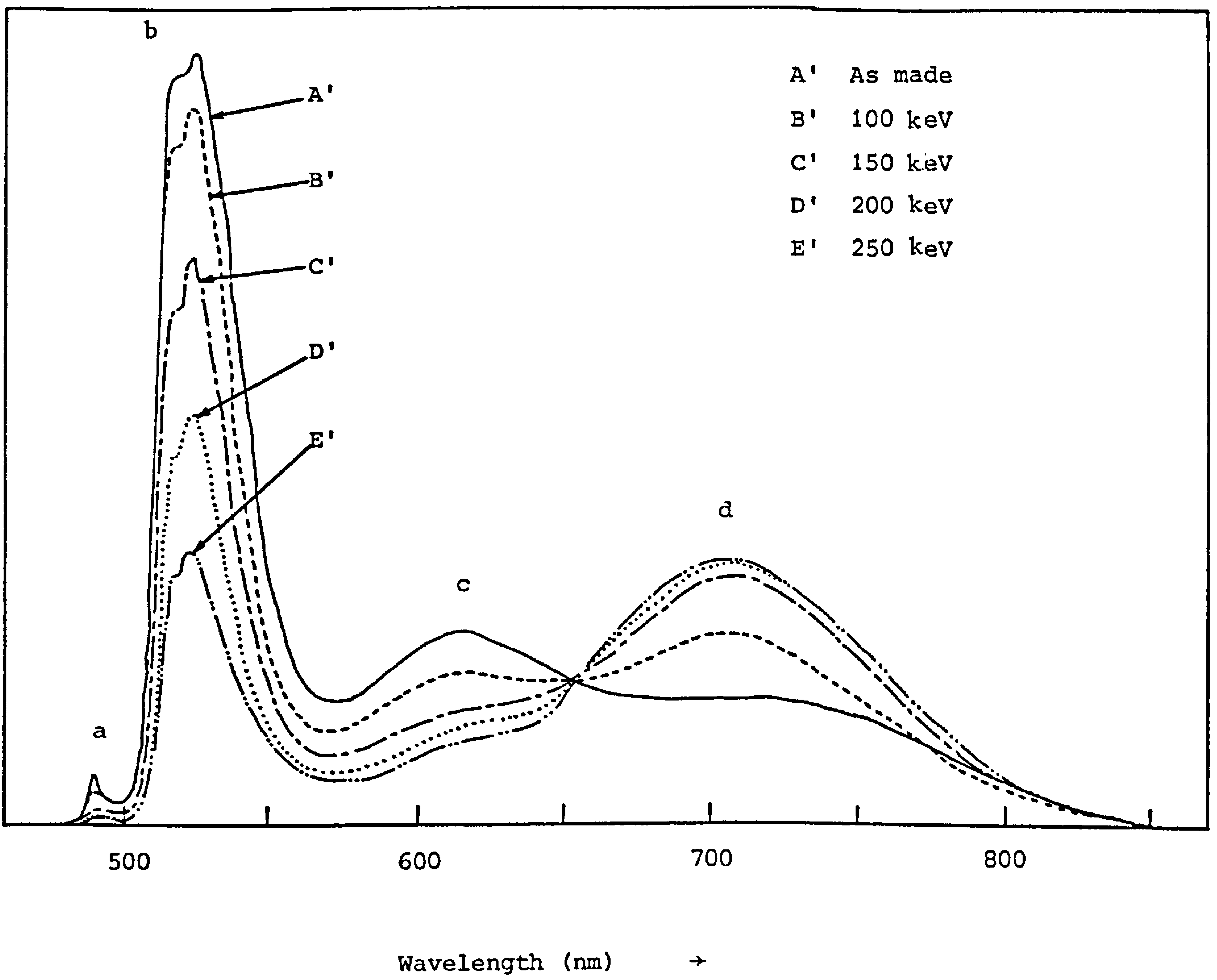


Figure (5-50) Cathodoluminescence emission spectrum of CdS thin films implanted with 5 x 10^{14} copper ions cm^{-2} at ion energies ranging from 100 to 250 keV.

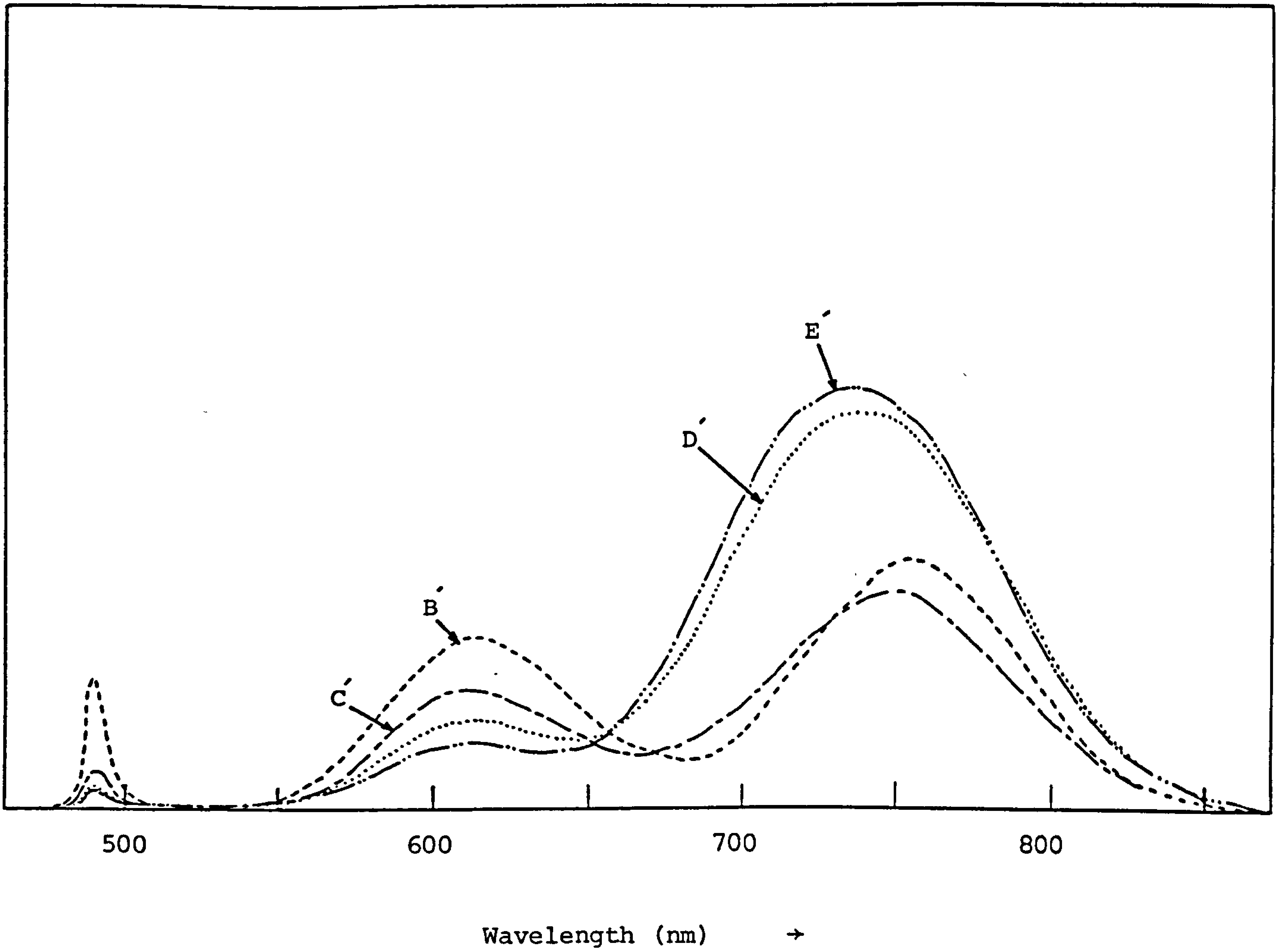


Figure (5-51) Cathodoluminescence emission spectrum for the same samples in figure (5-50) after 30 mins. vacuum annealing at 300°C.

although this is slightly shifted towards shorter wavelength for sample C'. This shift is more noticeable for sample D' and E' where higher ion energies were used.

In order to study the effect of ion implantation on cell parameters such as V_{OC}, J_{SC}, and η, the CdS layers were given the same treatment as described earlier in section (5.5.1), and the resistance and Schottky capacitance values were again obtained on similar layers after identical implantation conditions. Table (5-18) lists these results together with corresponding values of the equivalent thickness $\bar{d}$ and x for the Cu_xS layers obtained by electrochemical measurements. It is clear that V_{OC}, J_{SC}, x and η values for these cells all show a reduction as a result of increasing the ion energy, while the equivalent thickness, $\bar{d}$, appears to be effectively independent of the energy of ions used here.

5.5.3. Depth profile for copper ion implantation of CdS

Figure (5-52) shows the Auger electron spectroscopy depth profile of a copper ion implanted CdS film. This film was implanted with 5×10^{14} ions cm^{-2} at 50 keV, then the experiment was carried out using the same profiling and measurement procedure as described earlier in this chapter.

Curve (i) in figure (5-52) shows the copper concentration depth profile immediately after implantation. This curve seems to drop fairly sharply after about 9 mins. sputtering time (corresponding to a depth of 36 nm). Curve (ii) is obtained for a similarly implanted CdS layer after being heated in vacuum for 30 mins. at 300°C. In this case the concentration seems to drop at slightly greater depth, but the sharpness of both curves in figure (5-52) indicates that the diffusion of copper ions into the grain boundaries of the CdS layer is very small.

TABLE (5-18).

Dose	Energy	V_{oc} (volts)	J_{sc} mA cm^{-2}	η%	X	$\bar{d}$ Å	R Ω	C pF	
unimplanted		0.42	15.3	3.45	1.970	3616	0.1	1950	A
10^{14} ions cm^{-2}	50 kV	0.5	16.5	5.47	1.978	3374	0.18	308	B
5×10^{14} ions cm^{-2}	50 kV	0.5	18.2	6.17	1.986	3012	0.38	279	C
10^{15} ions cm^{-2}	50kV	0.5	15.0	5.15	1.986	2743	0.86	256	D
5×10^{15} ions cm^{-2}	50 kV	0.505	15.1	4.5	1.989	-	28.7	111	E
10^{16} ions cm^{-2}	50 kV	0.505	12.38	4.43	1.992	2323	4100	17	F
5×10^{14} ions cm^{-2}	100 kV	0.48	16	5.3	1.989	3375	3.1	205	B'
5×10^{14} ions cm^{-2}	150 kV	0.47	14.4	4.9	1.976	3255	8.1	174	C'
5×10^{14} ions cm^{-2}	200 kV	0.45	8.88	2.75	1.958	3320	11.2	165	D'
5×10^{14} ions cm^{-2}	250 kV	0.44	6.22	1.88	1.954	3435	12.1	146	E'

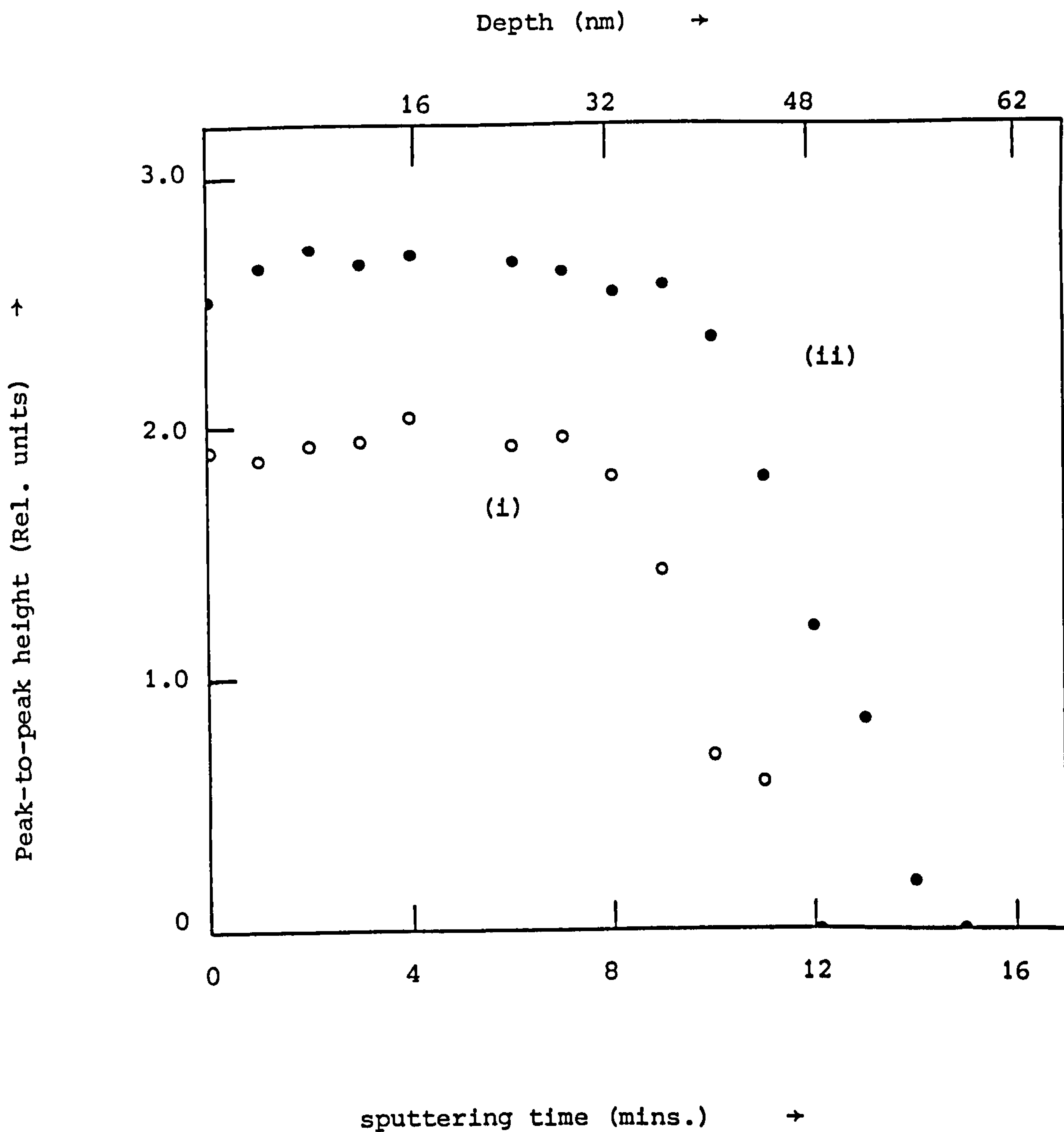


Figure (5-52). Auger electron spectroscopy of copper implanted CdS thin film with 5×10^{14} ions cm^{-2} at 50 keV. (i) before annealing treatment and (ii) after 30 mins. vacuum annealing at $300^{o}C$.

Chapter 6

Discussion

6.1. Introduction

It is clear from the results presented in chapter 5 that the various cell fabrication processes are very much interrelated. As a result, the task of optimising these conditions to achieve the best efficiency has been a difficult one and some problems still remain.

Although each of the different components in this complex multilayer structure must be chemically, electrically and optically compatible with their neighbours the components which have been shown to play a particularly important role are the copper sulphide layer and CdS-Cu_xS heterojunction. The structure of this heterojunction is critically dependent on both the initial fabrication process and, in particular, the post fabrication annealing treatment which also has a strong influence on the copper sulphide phase. The heterojunction itself and the CdS layer adjacent to it play important roles in determining the overall photo-electrical properties of the device, while the stoichiometry of the copper sulphide layer and its thickness are the major factors determining the number of photogenerated carriers available for collection and the long term stability of the cells. These are the major points to be discussed in the following sections.

6.2. Dependence of cell characteristics on material properties

In earlier work on evaporated CdS solar cells there had been some controversy concerning the quality of the CdS required as an evaporation source. Clearly, as an important first step in this project, it was necessary to investigate this problem and to establish the best evaporation

conditions required to achieve the appropriate stoichiometry and associated electrical properties of the resultant CdS films. The results in section (5.1.1b) show that, providing high purity CdS powder is used, the required electrical properties of the CdS thin films can be obtained by adjusting both the substrate temperature and the deposition rate during the evaporation cycle. The optimum range of values of CdS electrical resistivity are a compromise between the need to make it as low as possible, to reduce the series resistance of the device, and to make it as high as possible in order both to improve the stoichiometry and the stability of the copper sulphide (as discussed in section 5.4) and also to ensure that the major portion of the diffusion voltage at the junction occurs in the CdS.

The results in section (5.1.1a) indicate that the CdS-substrate interface can introduce resistance and can, to some extent, affect the short-circuit current. Of course, any resistance at this interface adds to the series resistance of the device and this consequently reduces the fill-factor. Clearly, a low resistance, ohmic contact is required.

A satisfactory CdS-substrate contact has been shown to be accomplished by using zinc coated copper, confirming the earlier findings of Bragagnolo [202]. The added advantage of this substrate is the improvement in the short-circuit current achieved due to the high reflectivity surface of the copper-zinc alloy which is formed. This allows light which is not initially absorbed in the copper sulphide layer to be reflected back to the front surface, thereby increasing the photon absorption factor. This makes it possible to keep the absorbing layer (copper sulphide) thinner than would otherwise be necessary to provide the same photon absorption rate and to achieve a good carrier collection in spite of the short diffusion length.

The CdS film microstructure and surface topography are clearly influenced by the topography of the underlying substrate. However, when the CdS thickness is increased, the CdS surface becomes less dependent on the substrate topography and the CdS columnar structure and the grain size improve. While radiation channelling within the grains increases the absorption probability for the incident radiation, the results described in section (5.2.1) clearly show that the pyramidal texturing of the upper surface, achieved by etching the CdS film in HCl acid, is also very important. This texturing reduces the effective reflectance of the solar cell, by means of multiple reflections and secondary absorption of the scattered incident radiation. This makes the use of an antireflection coating for this device much less necessary.

The other main component of the CdS-Cu_xS device is the copper sulphide layer, in which the x value has been shown to have a critical influence on both the electrical and optical properties of the layer. Since copper sulphide is a defect semiconductor with Cu vacancies acting as acceptors, the carrier density decreases as x approaches 2. Work reported here and by other authors [5,6,42,44,49,52,109] has shown, as expected, that the x parameter is very dependent on the copper sulphide formation conditions and on the post-fabrication annealing treatment. In addition, the work reported here has provided evidence that the stoichiometry of the Cu_xS layer is influenced by the stoichiometry of the CdS layer on which it is formed. Further investigations into the structure of the Cu_xS layer has revealed that under certain annealing conditions, there is a particularly high concentration of cadmium in the Cu_xS layer, especially at the copper sulphide surface. Since cadmium is a donor dopant in the copper sulphide layer, the cadmium concentration would be expected to affect the net carrier concentration as well as influencing the minority

carrier life time and transport properties. It is reasonable to conclude that changes in the surface recombination velocity and improvements of minority carrier diffusion length which were already indicated by Pfisterer et al. [220] as a result of improvements of the copper sulphide stoichiometry may in fact be partly due to the absence of cadmium from the copper sulphide layer. The copper sulphide layers studied by Pfisterer et al. [220] had copper overlayers and had been annealed in air. It has been shown here (section 5.3.5) that this treatment leads to a much reduced concentration of Cd throughout the copper sulphide layer, as well as to an improvement of copper sulphide stoichiometry.

It must be noted that other impurities such as O, C and Cl were not detected within the bulk of the copper sulphide, but it is possible that such impurities are present at concentration levels below the resolution of the Auger measurements.

Another inference that can be drawn from these studies is that the junction is generally a fairly diffuse one. This can be understood in view of the nature of the ion-exchange reaction taking place during the formation of the copper sulphide layer in which interdiffusion of Cu and Cd occurs. It is of course necessary to bear in mind that CdS is in the form of a polycrystalline layer with columnar grains and grain boundaries perpendicular to the substrate surface. Therefore the existence of Cu deep down into the CdS region is due largely to deep grain boundary penetration of the copper sulphide. Hence two types of junction interface are expected in the grain structure model which was shown in figure (5-34). One is at the top of the grains and the other is down between the grains (at the grain boundaries). These interfaces cannot be separated and the Auger depth profile, such as that in figure (5.33), is the resultant of these two interfaces. The structure of the interface is therefore a

complex one which clearly depends on the initial fabrication process and on the post-fabrication annealing conditions.

The final component for cells made in this laboratory is the gold grid contact. This contact affects the cell in two ways. First, in its main role as a contact to the external circuit, it must be designed to minimize the series resistance of the cell and hence maximise the fill-factor as shown in section (5.1.3.). Secondly, the presence of the contact produces some shading of the active region of the cell. This shading must be minimised so that the grid has to have a fine, open structure. Clearly these two design requirements conflict with each other, but in this work no detailed consideration has been given to optimizing the grid design for maximum overall efficiency.

6.3. Junction Model

From a fundamental point of view the CdS-Cu_2S cell is a p-n heterojunction diode. Figure (6-1) illustrates the band diagram of such a heterojunction in the dark. This model is similar in many respects to that suggested by other groups [5,47,52,157] and is consistent with data obtained from I - V, C - V, spectral response and DLTS measurements made during this study. The copper sulphide is almost degenerate with hole concentration equal to the copper vacancy density ($p \sim 10^{22}$ cm^{-3} [157]) and much higher than the electron concentration in the CdS, so that the space charge region occurs almost entirely in the CdS region where traps have been observed to exist, as shown in section (5.2.9). Consideration of the value for the electron affinity difference between the CdS and the Cu_2S (calculated here to be 0.25 eV) and the values of the band gaps yields a valence band discontinuity of 1.45 eV. With the Fermi energy at about

0.15 eV below the conduction band edge in the CdS, the diffusion voltage is about 0.8 volts.

As a result of the lattice mismatch between the Cu_xS and the CdS layers, interface states exist at the heterojunction. Rothwarf [157] has calculated the theoretical interface states density at the junction and found it to be in the order of 10^{13} cm^{-2} for a lattice mismatch of about 4%.

The various dark current paths for charge carriers in a heterojunction are summarized in section (3.3), figure (3-6). In general all these paths may contribute to the total current crossing the junction. In fact the experimental observations may be explained in terms of a multiple diode structure in which the cell is assumed to consist of many different diodes with different dominant current transport mechanisms.

The band-diagram in figure (6-1) shows deep level traps in the CdS side of the junction. According to the results shown in figure (5-31), the density and the electrical parameters of these traps may vary from device to device. This depends on the growth conditions of the CdS film and the later fabrication processes, in particular the annealing treatments. Although a detailed study of these traps has not been attempted in this work, it is clear from the DLTS results for Schottky barriers of Au-CdS made in this laboratory that deep levels exist in the CdS prior to cell formation. This indicates that the defects which cause these traps are due to native point defects or to complex states involving native defects and impurities [98]. During fabrication of the CdS-Cu_2S solar cell, the diffusion of copper into the CdS changes the traps position as well as their electrical properties as clearly shown in table (5-16). Trapping states in CdS associated with Cu^o, Cu^+, Cu^{++} have already been reported by Suda and Kurita [222], while Haines and Bube [223] have shown

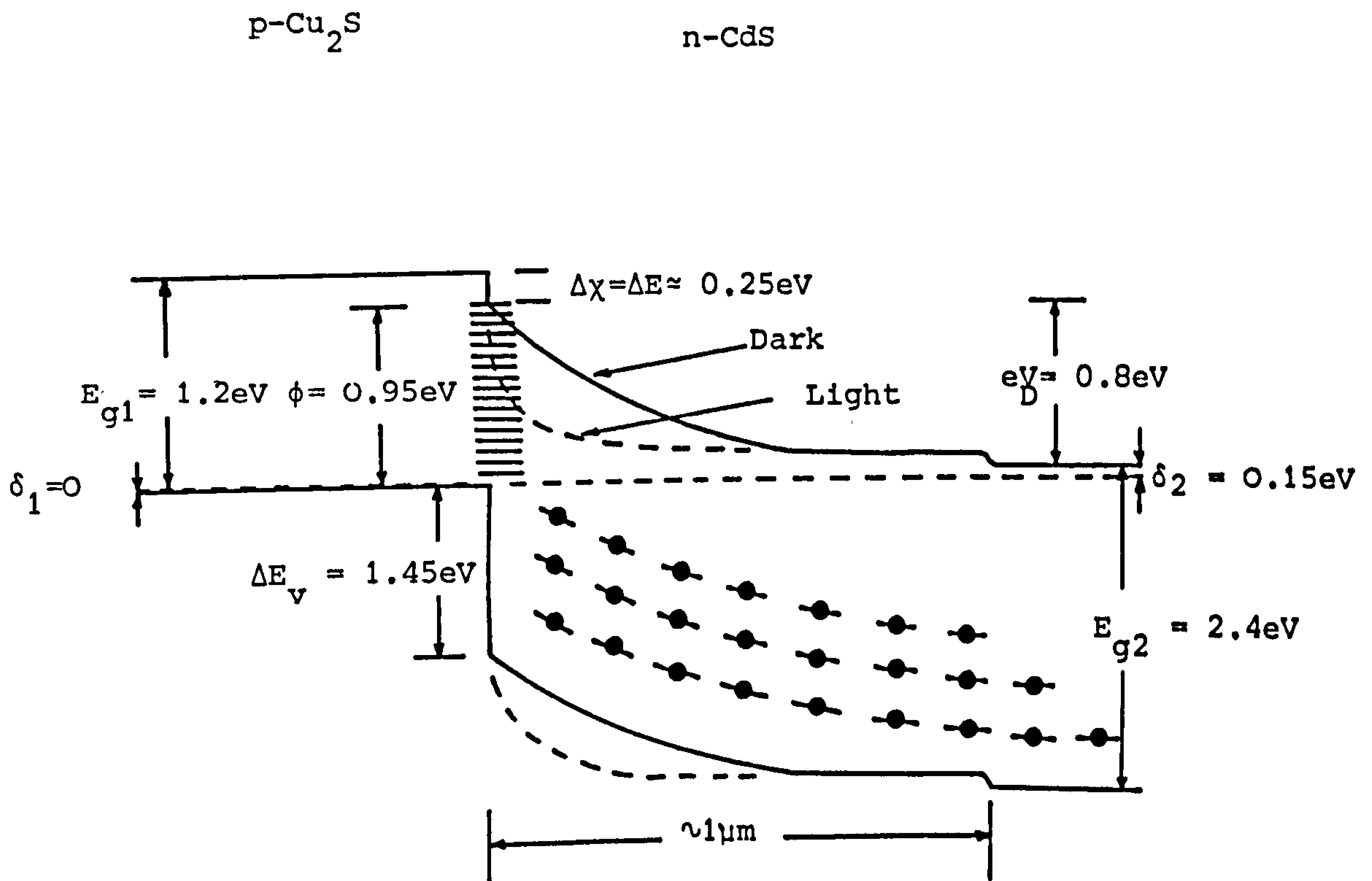


Figure (6-1) Band diagram of the CdS-Cu_2S heterojunction

evidence that acceptor states are generated by the diffusion of copper during annealing treatment. However, the identity of particular levels in the CdS layer and the effect of the annealing treatment on the trap parameters are still not fully known and further research is needed to clarify these matters.

6.4. Junction Structure

As shown in section (5.3.2) the copper sulphide layer grown onto polycrystalline CdS yields a very complicated structure in which the grain boundaries are an important feature. The model described in section (6.3) has not taken into account the effect of grain boundaries and other structural defects which inhibit the achievement of the open-circuit voltage and the short-circuit current expected for the ideal $CdS-Cu_2S$ heterojunction.

Recombination at grain boundaries is expected to be a potential source of carrier losses with corresponding reductions in short-circuit current. Junction area effects related to grain boundaries may also reduce the achievable value of the open-circuit voltage, as discussed in section (5.2.1). As shown in section (5.3), grain boundaries can result in enhanced diffusion of copper and in extreme cases penetration right through the base can completely short circuit the device.

Due to the non-planar structure of the interface, it is expected that some regions will have better diode characteristics than others. When forward bias is applied to the junction, the voltage is distributed unequally among the various grain and grain boundary regions of the interface with the charge carriers preferentially flowing through the poor junction region (probably the grain boundary regions). In fact the dark I - V characteristics in figure (5-21) have shown three distinguishable

regions. Following the ohmic region at low bias voltages (region I) diodic behaviour starts to appear in region II but the high value of the diode ideality factor indicates that tunnelling is the dominant transport mechanism here. Also the barrier height (calculated from the reverse saturation current) is poor even after annealing (see table 5-14). This conductivity region may be associated with the junction at the grain boundaries. In region III the effective barrier height suddenly increases to a value close to that obtained from the plot of V_{oc} versus kT in figure (5-25). Furthermore the diode ideality factor and the reverse saturation current in this region as shown in table (5-14) are much lower than the values in region II. It is assumed that conductivity in region III is associated with the mid-grain areas of the cell. In fact in some cells, a value of diode ideality factor lower than 2 is obtained together with low values of the reverse saturation current giving effective barrier heights up to 0.9 eV. However, the measured reverse saturation currents, diode ideality factors and the barrier heights for region II and III have showed a large variation. This can be explained in terms of differences in the contributions of the mid-grain and grain boundary regions to the total effective area of the cells. It must be noted that, the existence of three distinct regions are only seen for cells fabricated using CdS layers with carrier concentration in the range of 10^{16} - 10^{17} cm^{-3} or after short annealing treatment for cells fabricated using slightly higher conductivity CdS layers.

6.5. Effect of illumination on barrier

Differences between dark ln J versus V characteristics in figure (5-23) and a ln J_{sc} versus V_{oc} plot, obtained by varying the light

intensity as is shown in figure (5-20), reveal a dependence of the reverse saturation current and the diode ideality factor on illumination. This is due to the deep trapping centres at or near the junction which are not in good thermal communication with the conduction or valence bands and can have their occupancy, and hence charge, changed by illumination.

The existence of the traps in the space charge region is very important in relation to the operation of the cell. As argued by Vassilevskii et al. [224] the barrier may shrink as a result of a positive charge transfer within the space charge region. Such a charge transfer is produced by photo-hole trapping at the deep levels in the CdS. The resultant increase in the effective value of the ionized donor density in the space charge layer causes a narrowing of the space charge layer width and thus affects the charge transport process across it.

This photo-induced change in the space charge distribution leads to the frequently observed cross-over between the dark and light characteristics in CdS-Cu_2S cells. The extent of the cross-over has been shown to be closely associated with the density of acceptor centres introduced into the space charge region as a result of the diffusion of copper during annealing. The width of the compensated region in the CdS near the interface increases as the annealing time is prolonged as is clearly seen from the C^{-2} versus V plots in figure (5-29). The high voltage forward bias region of the dark I - V characteristic shown in figure (5-26) confirms the existence of the resistive region in annealed cells. Similar effects have also been observed using copper ion implanted CdS where the results in table (5-18) show that, the capacitance of Au-CdS diodes decreases as the copper ion fluence increases.

It can be noted that the cross-over behaviour is not a necessary feature of the CdS-Cu_2S solar cells since no sign of this behaviour is seen

when the copper sulphide layer is formed on a high conductivity CdS ($\rho < 1\ \Omega\,cm$) provided there has been no annealing treatment.

6.6. Annealing and diffusion processes

One of the major factors which influence the rate of inter-diffusion at the CdS-Cu_2S interface during post-fabrication annealing is the nature of the annealing atmosphere.

The results in section (5.3.4) have shown that the CdS-Cu_2S junction is broadened following very mild annealing treatment in air (10 mins. at 100°C), with a significant concentration of cadmium being distributed throughout the copper sulphide layer. This was very different to the situation following annealing in vacuum or hydrogen. In both these cases, the integrity of the CdS-Cu_2S junction was well maintained after 10 mins. annealing treatment at temperatures up to 400°C, and significant concentrations of cadmium were found throughout the copper sulphide layer only after raising the temperature to 600°C.

In seeking an explanation for the out-diffusion of cadmium in air annealed cells, it is natural to consider oxidation at the front surface of the cell as a possible driving force. Certainly oxide formation is to be expected in air but, although this process had previously been considered to involve copper ions, the observation reported here of cadmium penetration through the copper sulphide layer indicates the probability that the oxidation products are a complex mixture of species including cadmium possibly in the form of CdO. The primary source of cadmium in the copper sulphide layer is the underlying CdS layer and the residual cadmium in the copper sulphide layer due to incomplete exchange during the dipping process or the incompletely removed $CdCl_2$. These findings are in good

agreement with the work reported by Florio et al.,[221] who have shown that the predominant oxidation reaction involves cadmium rather than copper.

Although figure (5-14) shows a close similarity between the vacuum and hydrogen annealing for annealing times up to 20 mins., this similarity was less evident as the annealing time was continued. This is clearly seen in figure (5-17) for cells B and C. It must be noted that the annealing in vacuum was done in this laboratory at 10^{-5} torr so that, for long annealing times (several hours), some oxidation of the copper sulphide layer could be expected to take place.

Of particular concern in relation to efficiency enhancement and degradation processes is the relationship between the grain boundary and mid-grain diffusion rates. Figure (6-2) shows how the ratio D_{gb}/D_g varies as a function of annealing temperature for the three atmospheric ambients studied here. It is quite clear that at temperatures frequently used in post-annealing treatments (150^oC-250^oC), hydrogen annealing provides a significantly lower D_{gb}/D_g ratio than the other two cases and suggests that hydrogen is beneficial in inhibiting the detrimental grain boundary diffusion in thin film CdS cells. It should be noted that, although the experimental data on which figure (6-2) is based (see table 5-17 in section 5.3.6) indicates very clearly the different diffusion behaviour under the different ambient atmospheres, some reservations must be expressed concerning the analysis used to obtain the diffusion coefficients and the activation energies. In Le Claire's[192] analysis the grain boundary diffusion problem was evaluated for a planar surface with the grain boundary sandwiched between two flat grains. Furthermore the grain boundary was represented as a uniform slab of material of width S within which diffusion occurred. This situation does not relate closely to the

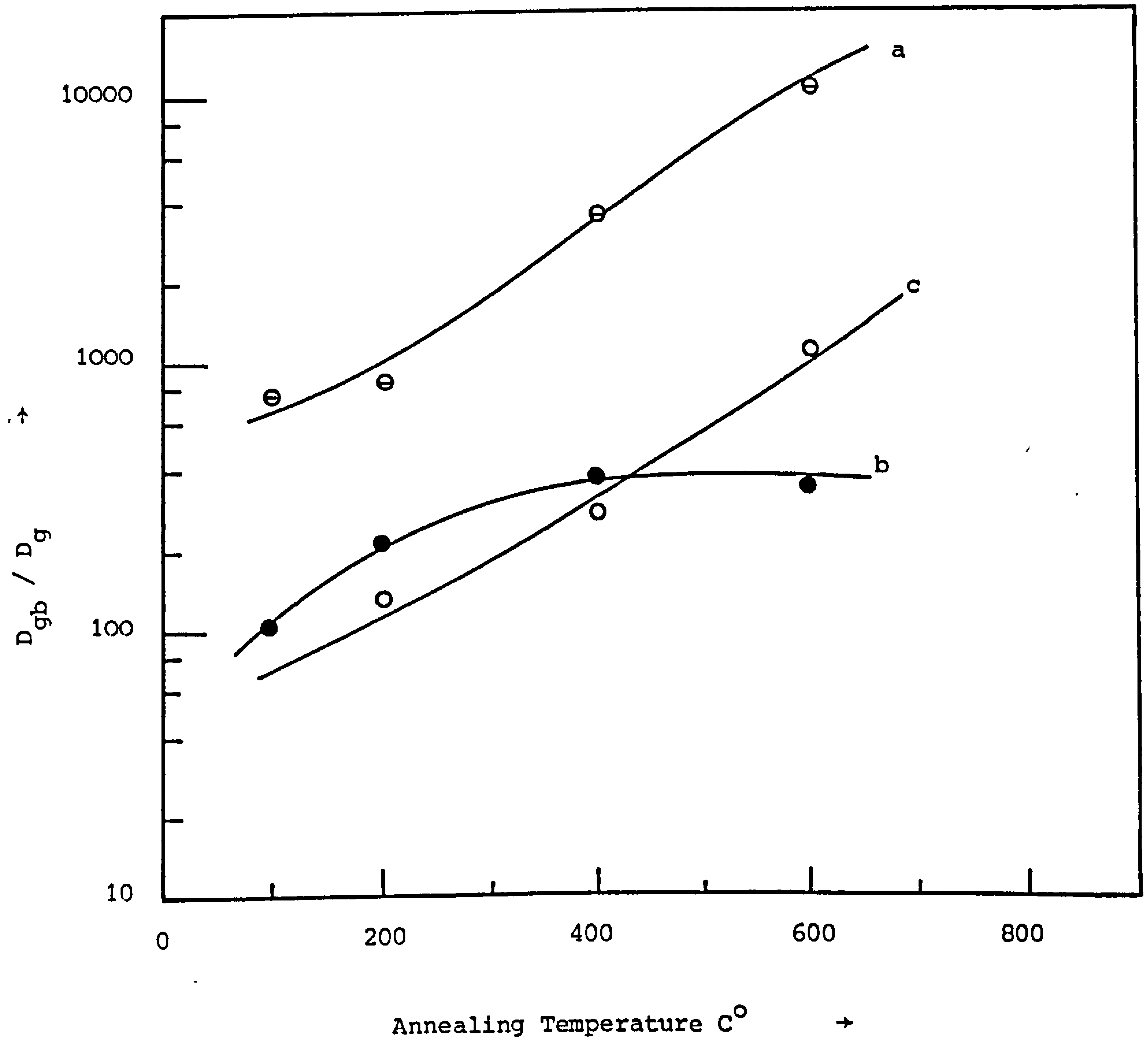


Figure (6-2) Ratio D_{gb}/D_g as a function of annealing temperature for three different conditions (a) air, (b) vacuum and (c) flowing hydrogen.

$CdS-Cu_2S$ system, where the copper exists in the grain boundary regions of non-uniform width, even before any annealing treatment. In fact the results obtained from previous quantitative investigations of copper diffusion into CdS involved single crystal samples and showed widespread disparity. For example, Clark (140), Szeto et al. (141) and Sullivan (142) measured the activation energy to be 0.77 eV, 0.58 eV and 0.96 eV respectively, although it should be noted that these investigations employed different copper detection techniques and, whereas the radioactive tracer method of Clark (140) measured the total copper concentration, the capacitance method of Sullivan (142) measured only the electrically active contribution. However, as Sullivan has shown that dislocations can have a dominant influence on the copper diffusion process, the lack of agreement between the results for different workers could be due, in part, to the use of samples containing different dislocation densities. In view of this observed sensitivity of the diffusion process in single crystals to the structural properties of the crystals, it would not be surprising to find some disagreement between data for single crystals and that for thin films. In fact, the values for the activation energy in table (5-17) are significantly smaller than those cited above for single crystals but, in addition to the different nature of the material involved, it should be noted that, in the previously cited investigations the copper was diffused into the CdS from a metallic layer deposited on the surface rather than a copper sulphide layer as in this study. Diffusion of copper into single crystal CdS from a thick copper sulphide layer has in fact been studied by Purohit et al. (143) who, in spite of observing diffusion coefficients significantly larger than those shown in table (5-17), obtained an activation energy of 0.09 eV, a value of similar magnitude to that found in this study for mid-grain regions.

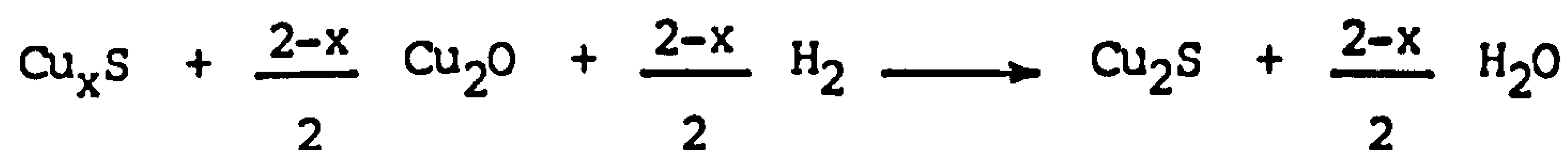
6.7. Operational stability of cells

When left exposed to the atmosphere freshly prepared CdS-Cu_2S solar cells are known to degrade with time. This degradation can be attributed partly to surface environmental contamination effects and partly to inherent problems associated with changes in the structure of the cells. The environmental effects can be overcome to a great extent by suitably encapsulating the cell so that most of the problems associated with the stability of the cells are concerned with structural effects within the cells. For example, the electrochemical decomposition of the copper sulphide can occur during cell operation when electric fields are set up across portions of the copper sulphide layer between grid lines and particularly adjacent to any macroscopic defects. This may cause changes in the stoichiometry of the copper sulphide by field-aided diffusion and in the extreme cases create free copper which may short out the cell especially in the presence of pinholes [225-226]. Zwicker et al. [225] showed that the lateral migration of copper toward the grid lines could occur under load, resulting in changes of the copper sulphide stoichiometry and hence lower values of the short-circuit current.

The effect of different fabrication procedures on the stability of cell characteristics is demonstrated in figures (5-45) and (5-46), which show respectively the variations in x parameters and short-circuit current as a function of time for three unencapsulated cells exposed to the atmosphere at room temperature. Cell (a) indicates very clearly that the copper treatment discussed in section (5.2.4) leads to cells with very stable electrical properties in comparison with cells which have no copper overlayer but are otherwise similar (cell b). The main reason for this stability is due to the fact that the copper sulphide is well protected from the atmosphere, by the copper oxide layer, leading to the maintenance

of a high value of x in the copper sulphide layer. Furthermore, in the presence of a copper overlayer the interdiffusion process at the $CdS-Cu_2S$ junction is significantly inhibited as clearly shown in figure (5-40).

In view of the fact that the diffusion of cadmium across the $CdS-Cu_2S$ interface has been shown to be associated with the degradation processes in this device, one of the several factors influencing the rate of degradation would be the stoichiometry of the CdS in the base layer and in the course of these studies, this has been found to be the case. Cell (c) in figure (5-46) shows the behaviour of a cell which was fabricated with a graded CdS layer. This cell was clearly more stable than the conventional device, although the lifetime was poor in comparison with the copper-treated cell. However, even in the absence of any interdiffusion processes occurring at the $CdS-Cu_2S$ interface, the cell efficiency would be expected to diminish as a result of oxidation at the front surface and the consequent loss of copper from the copper sulphide layer. If this was the main degradation process, then annealing in a reducing atmosphere would be expected to reverse the process and restore the initial electrical characteristics. In fact, as can be seen in figure (4-46), annealing in hydrogen did indeed restore the short-circuit current for cell (c) to a value close to its initial level. The major effect of this is in fact due to improvement of the copper sulphide stoichiometry either by the reduction of any copper oxide as:



$$Cu_xS + \frac{2-x}{2} Cu_2O + \frac{2-x}{2} H_2 \longrightarrow Cu_2S + \frac{2-x}{2} H_2O$$

or, by direct chemical reacton of the non-stoichiometry copper sulphide with the hydrogen as:

$$2\ Cu_xS + H_2 \longrightarrow x\ Cu_2S + H_2S$$

However, for cell (b) which had suffered serious degradation in air, it was

found that hydrogen annealing, at best, leads to only a partial recovery of the initial characteristics. This result is due partly to the deformation suffered by the CdS-Cu_2S interface and partly to the nature of the oxide at the front surface which, as discussed earlier in this chapter, is for these cells primarily cadmium oxide rather than copper oxide. Annealing these cells in a reducing atmosphere has the effect of leaving cadmium on the surface of the cell. This is seriously detrimental to the performance of the device, as has been corroborated directly by depositing a thin layer of cadmium on the surface of a freshly prepared cell.

Chapter 7

Conclusion

The work undertaken during this research project has confirmed that thin film $CdS-Cu_2S$ solar cells can be fabricated with a high efficiency of energy conversion provided that each stage of the fabrication process is carefully optimized. First, it is necessary to choose a substrate material which provides a highly adhesive contact, of low electrical resistance, to the CdS layer. Best results were obtained with zinc coated copper substrates having a zinc layer thickness in the range of 0.2-0.5 μm.

The CdS layer itself obviously plays a very important role in determining the efficiency and the stability of these cells. The required properties of this layer for high efficiency cells can be summarised as:

1. A resistivity of $10 < \rho < 100$ Ωcm, with carrier concentration of ~ 10^{17} cm^{-3}
2. A layer thickness > 20 μm with C axis perpendicular to the substrate
3. Crystallite grain size > 1 μm, with high packing density
4. An absence of defects (e.g. pinholes, particles of CdS powder, cracks or deep pits)
5. A textured surface (as provided by etching in HCl acid for 5-10 sec)

Although there had previously been some controversy concerning the CdS source material and evaporation conditions required to provide the above properties, the study which formed part of the work described here, has shown that a variety of CdS source powders can be used provided that the evaporation conditions are suitably adjusted. There is no universally

appropriate set of evaporation conditions.

The CdS electrical and structural properties have also been found to influence the rate of chemical reaction during the dipping process in CuCl solution. Clearly, much care is required in controlling this process but this alone is insufficient to obtain the desired copper sulphide properties. The results have shown that the required chalcocite phase of Cu_xS with x value as close as possible to 2 can only be obtained either by post-fabrication treatment in hydrogen (for up to 8 hr at 200°C) or by deposition of a copper overlayer (~100 Å thick) followed by air annealing for 90 mins. at 200°C. The optimum real layer thickness of the copper sulphide layer was found to be in the range 0.1-0.2 μm.

During the course of this project, a great deal of consideration was given to the diffusion processes which occur during post-fabrication annealing of the completed $CdS-Cu_2S$ thin film solar cells. Using Auger electron spectroscopy and argon ion etching, the copper concentration - depth profiles indicated that, for samples annealed in a flowing hydrogen atmosphere, the grain boundary penetration of copper at temperatures up to 600°C is significantly smaller than for samples annealed in vacuum or in air. Although annealing in hydrogen was known to have a beneficial effect on the quality of the Cu_xS layer, the fact that it inhibits grain boundary diffusion of copper has not been reported previously. An equally important finding has been that heating in air, even at slightly elevated temperature (approximately 100°C for 10 mins.), causes marked compositional changes at the $CdS-Cu_2S$ interface and the distribution of considerable quantities of cadmium throughout the copper sulphide layer. Under vacuum and in flowing hydrogen, the $CdS-Cu_2S$ junction remains stable at temperatures up to 400°C and only after heating to 600°C was a significant concentration of cadmium found to penetrate through the copper sulphide

layer. These results are consistent with the observation that prolonged heating in hydrogen at moderate temperatures (~200°C) gives rise to a steady improvement in efficiency (due to improved stoichiometry of the Cu_xS) with no accompanied degradation due to excessive interdiffusion at the junction. In contrast, as is well known, there is a rapid deterioration in electrical characteristics of cells which are heated in air and for much shorter times. It has been confirmed that this deterioration is associated with a significant change in the stoichiometry of the copper sulphide layer as well as the interdiffusion across the interface.

The stabilisation of cell characteristics by the technique of deposition of an overlayer of copper followed by annealing in air has been shown to be associated not only with the formation of a "protective" copper oxide layer over the surface but also with the maintenance of a relatively abrupt $CdS-Cu_2S$ junction interface. In contrast to the normal behaviour for air-annealed cells, the presence of a copper overlayer appears to inhibit the diffusion of cadmium across the $CdS-Cu_2S$ interface. Another important feature concerning cell stability was illustrated by the observation that the rate of interdiffusion across the junction is influenced by the stoichiometry of the CdS at the interface. This discovery suggests that further improvements in operational stability of these devices might be developed by suitable control of the physical and chemical structure of the $CdS-Cu_xS$ interface region. For this purpose it is necessary to modify the structure of a very thin layer at the surface of the CdS film. This might be achieved by changing the vapour growth parameters towards the end of the film deposition process (as reported here) or alternatively, by ion implantation. During the course of this project it was shown that this technique could be used successfully to

introduce copper and, thereby to satisfy the electrical requirements of the interface region. A brief study employing different ion fluences and different ion energies indicated that the best conditions were 5×10^{14} ions cm^{-2} at an energy of 50 keV. It is clear that the ion implantation technique provides interesting possibilities and there is clearly room for further investigation.

In chapter 6 of this thesis a band model for a $CdS-Cu_2S$ cell was formulated, based on the observed electrical properties of these devices. In the course of this work, cells with efficiencies of nearly 8% have been fabricated, but it is clear, from the proposed model, that higher efficiencies are possible. Some improvements could be obtained relatively easily. For example, a higher short-circuit current and a better fill-factor could be obtained using a better grid design and an antireflection coating. Less easily achieved improvements include the use of a planar junction (to increase the open-circuit voltage). This would necessitate the suppression of grain boundary diffusion or grain boundary passivation. An increase in the grain size is also expected to provide improved cell performance. This might be achieved using either the quasi-rheotaxy technique or applying a suitable annealing treatment such as laser annealing. With these improvements, $CdS-Cu_2S$ solar cells with efficiency up to 12% seem to be possible.

Pilot investigations on cells in which the CdS layer has been replaced by ZnCdS have revealed the expected increase in open-circuit voltage (as discussed in section 2.4.3.). Hence if the short-circuit current and the fill-factor can be maintained at values similar to those for $CdS-Cu_2S$ solar cells, then the efficiency of $ZnCdS-Cu_2S$ cells might reach 15-16%. Although the development of $ZnCdS-Cu_2S$ cells will undoubtedly raise some new problems, it is expected that this development

work would be aided significantly by the experience gained through the work with $CdS-Cu_2S$ cells.

Finally, it can be said that the work done during the course of this project has encouraged the view that, with continued development, thin film solar cells could be produced as relatively low cost, large area units and could, therefore, provide a significant source of energy, particularly in those developing nations which are blessed with high levels of solar radiation.

References

1. G.W. Rhodes and M.R. Reilly, 5th E.C. Photovoltaic Solar Energy Conference. Proceedings of the International Conference, held at Kavouri (Athens), Greece. 17-21, October 1983, p.321.

2. A.L. Fahrenbruch and R.B. Bube, "Fundamentals of Solar Cells", Academic Press, Inc. (1983).

3. M. Prince, J. Appl. Phys., 26, (1955) 534.

4. J.J. Loferski, J. Appl. Phys., 27, (1956) 777.

5. A.M. Barnett and A. Rothwarf, IEEE Transactions on Electron Devices, ED-27, (1980) 615.

6. J.A. Bragagnolo, A.M. Barnett, J.E. Phillips, R.B. Hall, A. Rothwarf and J.D. Meakin, IEEE Trans. Electron Devices, ED-27, (1980) 645.

7. A. Catalano, R. D'Aiello, J. Dresner, B. Faughnan, A. Firester, J. Kane, Z.E. Smith, H. Schade, G. Swartz and A. Triano, Proc. 16th IEEE Photovoltaic Specialists Conference, held at San Diego (California), USA, 27-30, Spetember (1982), p.1421.

8. S.S. Chu, T.L. Chu, F.S. Zhang, W.J. Chen and Q. H. Wang, Proc. 16th IEEE Photovoltaic Specialists Conference (1982) p.1149.

9. R.A. Michelsen and W.S. Chen, Proc. 16th IEEE Photovoltaic Specialists Conf., (1982) p.781.

10. R.B. Hall, R.W. Birkmire, J.E. Phillips and J.D. Meakin, Proc. 15th IEEE Photovoltaic Specialists Conference held at Kissimmee, Florida, USA, 12-15 May (1981), p.777. or in Appl. Phys. Lett., 38 (1981) 925.

11. Y.S. Tyan and E.A. Perez-Albuerue, Proc. 16th IEEE Photovoltaic Specialists Conf. (1982),p.

12. L. L. Kazmerski, Univ. of Mine, Orono, Second Quarter Report to NSF-RANN and ERDA, NSF/AER 75 - 19576/OR/77/2 (1977) p.13.

13. J.L. Shay, S. Wagner, M. Bettini, K.J. Bachman and E. Buehler, IEEE Trans. Electron Devices, ED-24 (1977), 483.

14. R.A. Mickelsen, W.S. Chen, Y.R. Hsiao and V.E. Lowe, IEEE Transactions on Electron Devices, ED-31, (1984) 542.

15. M. Bhshan, Appl. Phys. Lett., 40, (1982) 542.

16. E. Becquerel, Compt. Rend., 9, (1839) 561.

17. W.G. Adams and R.E. Day, Proc. R. Soc. London Ser. A, 25, (1877) 113.

18. R. Appleyard and J. Telegraphic, Electrical Review, 28, (1891) 124.

19. B. Lang, Zeit. Phys. 31, (1930) 139.

20. L.O. Grondahl, Rev. Mod. Phys., 5, (1933) 141.

21. W. Schottky, Zeit. Phys. 31, (1930) 913.

22. R.S. Ohi, U.S. Patent, 2, (1941) 402.

23. J. Stariewicz, L. Sasnowski and O. Simpson, Nature (London), 158, (1946) 28.

24. L. Sosnowski, Phys. Rev.,72, (1947) 641.

25. S. Benzer, Phys. Rev.,72, (1947) 1267.

26. M. Becker and H.Y. Fan, Phys. Rev., 78, (1950) 301.

27. D.M. Chapin, C.S. Fuller and G.L. Pearson, J. Appl. Phys., 25, (1954) 676.

28. D.C. Reynolds, G. Leies, L.L. Antes and R.E. Marburger, Phys., Rev., 93, (1954) 533.

29. P. Rappaport, Phys.,Rev., 93, (1954) 246.

30. P. Rappaport, J.J. Loferski and E.G. Linder, RCA, Rev., 17, (1956) 100.

31. A.E. Van Aerschodt, J.J. Capart, K.H. David, F. Fabbricotti, K.H. Heffels, J.J. Loferski and K.K. Reinhartz, IEEE Trans. Electron Devices, ED-18, (1971) 471.

32. R.H. Bube in "Solar Materials Science", Ed. Lawrence E. Murr, Chapter 17, Academic Press, (1980).

33. P. Rappaport and J.J. Loferski, Proc. 11th Annual Battery Rand, D. Conf. p.96 (U.S. Army Signals Eng. Lab. Fort Monmouth, N.J., USA 1957).

34. Proc. Int. Conf. Phys.and Chem. Semicond. Heterojunctions and layers structures, Akademia Kiado, Budapest (1971).

35. Proceeding of 1st to 12th Photovoltaic Specialist Conf. Reports published by IEEE (New York).

36. D.A. Cusano, Sol. St. Electron, 6 (1963) 217.

37. D. Bonnet, M. Selders and H. Rabenhorst, Fest Kor per problems, XVI (1976) 293.

38. D. Bonnet and H. Rabenhorst, Solar Cells, Proc. Int. Colloq., Toulouse, 6-10 July 1970, Gordon and Breach, London (1971) p.155.

39. H.J. Hovel, "Solar Cells", Semiconductors and Semimetals., Vol.11, Academic Press, New York, ed. R.R. Willardson and A.C. Beer (1975).

40. C.E. Backus, ed. "Solar Cells", IEEE Press, New York, (1976).

41. A.G. Stanley, Appl. Solid State Sci., 5, (1975) 251.

42. R. Hill, Active and Passive Thin Film Devices, Ed. T. J. Coutts, Academic Press, London, p.487.

43. F.A. Shirland and I. Rai-choudhury, Rep. Prog. Phys., Vol., 41, (1978) 1839.

44. M. Savelli and J. Bougnot, Problems of the Cu_2S/CdS cell. In "Solar Energy Conversion - Solid-State Physics Aspects", Ed. B.O. Seraphin, Topics in Applied Physics, Vol. 31, (1979), p.213.

45. A.L. Fahrenbruck and J. Aranovich, Heterojunction Phenomena and Interfacial Defects in Photovoltaic Converters, ref.44, p.257.

46. L.L. Kazmerski, Electrical Properties in Polycrystalline Semiconductor Thin Films, Academic Press, New York, (1981).

47. A. Rothwarf, Solar Cells, 2, (1980) 115.

48. L.C. Burton, Solar Cells, 1, (1979/80) 159.

49. W.H. Bloss and H.W. Schock, CdS-Cu_xS Thin Film Solar Cells, In Photovoltaic and Photoelectrochemical Solar Energy Conversion, Ed. F. Cardon et al. Plenum Press, New York, (1981) p.117.

50. W.G. Townsend, Schottky Barrier Solar Cells, ref.49, p.67.

51. R.N. Hall, Solid-State Electronics, 24, (1981) 595.

52. S. Martinuzzi, Solar Cells, 5, (1982) 243.

53. L.D. Massie, Space-Aeronautics (1964) p.60.

54. F.A. Shirland, Adv. Energy Conv.,6, (1966) 201.

55. P.A. Crossley, G.T. Noel and M. Wolf, Final Rep. Contract BASW-1427, RCA Astro-Electron Div., Hightstown, New Jersey (1968).

56. D.M. Perkins, Adv. Energy Conversion, 7, (1968) 265.

57. A.E. Carlson, L.R. Shiozawa and J.D. Finegan, U.S. Patent, 2, (1958) 820.

58. D.A. Gorski, U.S. Ptent, 3, (1965) 186.

59. T. Avignon, J.P. Sorbier, F. Cabane-Brouty and M. Martinuzzi, vide 141, (1969) 196.

60. F.A. Shirland, F. Augustine and W.K. Bower, 2nd Quart. Rep. Contract NAS3-6461, NASA-CR-54413, Clevite Corp. (1965).

61. J.C. Schaefer, E.R. Hill and T.A. Griffin, Final Rep. Contract NAS3-7631, Harshaw Chem. Co. (1966).

62. F.A. Shirland, J.R. Hietanen, F. Augustine and W.K. Bower, 3rd Qart. Rep. Contract NAS3-6461, Clevite Corp. (1965).

63. H.E. Nastelin, J.R. Hietanen and F.A. Shirland, Final Rep. AF33 (615)-3253 Clevite Corp. (1967).

64. J.P. David, S. Martinuzzi, F. Cabane-Brouty, J.P. Sorbier, J.M. Mathieu, J.M. Roman and J.F. Bretzner, Proc. Int. Colloq. Solar Cells, (1971) p.81.

65. J.I.B. Wilson and J. Woods, J. Phys. Chem. Solids, 34, (1973) 171.

66. R.R. Araya, R. Beaulieu, Y. Kwietniak and J. Laferski, American Vacuum Society, (1982) p.306.

67. R.J. Miller and C.H. Bachman, J. Appl. Phys. 29, (1958) 1277.

68. IEC, Quarterly Report XS-9-8309-1-03, Nov. 1980 (Univ. of Delaware, USA) 1980.

69. IEC, Quarterly Report XS-9-8309-1-04, Dec. 1980 (Univ. of Delaware, USA) 1980.

70. R.R.Addiss, Nat. Symp. Vac. Tech. Trans., 10th (1963) p.354.

71. B.D. Golkin, N.V. Troitskaya and R.D. Ivanov, Kristallografiya, 12, (1967) 878, Sov. Phys. Crystallogr., 12, (1968) 766.

72. F. V. Shallcross, Trans. AIME, 236, (1966) 309.

73. J. De Klerk and R.F. Kelly, Rev. Scient. Inst., 36, (1965) 506.

74. K.V. Shalimova, A.F. Andrushko, V.A. Dmitriev and L.P. Pavlov, Kristallografiya, 8, (1963) 774, Sov. Phys. Crystallogr., 8, (1964) 618.

75. M. Bujatti, J. Phys. D., 1, (1968) 983.

76. J. Dresner and F.V. Shallcross, J. Appl. Phys., 34, (1963) 2390.

77. C. Wu and R.H. Bube, J. Appl. Phys., 45, (1974) 648.

78. Y. Terasaki, T. Murakami and H. Toyoda, Rev. Elec. Comm. Lab., 14, (1966) 425.

79. N.F. Foster, J. Appl. Phys., 38, (1967) 149.

80. R.B. Hall, International Workshop on CdS Solar Cells and other Abrupt Heterojunction, University of Delaware, New York, USA, (1975) NSF-RANN AER75-15858, p.284.

81. N. Remeo, Mater. Chem., 4, (1979) 571.

82. N. Remeo, J. Crystal Growth, 52, (1981) 692.

83. K.H. Norian and J.W. Edlington, Proc. 14th IEEE Photovoltaic Specialists Conference, Jan. 7-10, California, USA, 1980, p.701.

84. R.R. Addiss, Nat. Symp. Vac. Tech. Trans., 10th (1963) p.354, and also in Rept. No. ASD-TR-61-11, RCA Corp. Princeton, New Jersey, (1961).

85. H. Berger, Phys. Status Solidi, 1, (1961) 739.

86. C.A. Escoffery, J. Appl. Phys., 35, (1964) 2272.

87. H. Berger, E.Gustsche and W. Kahle, Phys. Stat. Solidi, 7, (1964) 679.

88. M.G. Miksic, E.S. Schlig and R.R. Haering, Solid-State Electron, 7, (1964) 39.

89. A.S. Esbitt, Phys. Stat. Solidi, 12, (1965) K35.

90. J.M. Gilles and J. Van Cakenberghe, Nature, 182, (1958) 862.

91. A. Vecht and A. Apling, Phys. Stat. Solidi, 3, (1963) 1238.

92. K.W. Boer, J. Appl. Phys., 37, (1966) 2664.

93. IEC Quarterly Report, XS-9-8309-1-08 (University of Delaware, USA) Feb. (1982).

94. F.A. Shirland, Solar Cell, 1, (1979/80) 183.

95. K.W. Boer, C.E. Birchenall, I. Greenfield, H.C. Hadley, T.L. Lu, L. Partain, J.E. Phillips, J. Schultz and W.F. Tsen, Proc. 10th IEEE Photovoltaic Specialists Conference, New York, (1973) p.78.

96. L.F. Donaghey, J.A. Duisman, T.M. Peter and P.R. Ryason, 14th IEEE Photovoltaic Specialist Conference, (1980) p.728.

97. H.W. Brandhorst, F.L. Campora and A.E. Potter, J. Appl. Phys., 39, (1968) 6071.

98. J. Oualid, D. Sarti, J. Gervais and M. Martinuzzi, J. Phys. C: Solid-State Phys., 12, (1979) 2313.

99. P. Besomi and B. Wessels, J. Appl. Phys.,51, (1980) 4305.

100. F.A. Shirland, J. Appl. Phys., 50, (1979) 4714.

101. J.J. Loferski and J. Shewchun, ref.80, p.318.

102. E. Castel and J. Vedel, Analusis, 3, (1975) 487.

103. W.R. Cook, L.R. Shiozawa and F. Augustine, J. Appl. Phys., 41, (1970) 3058.

104. S. Djurle, Acta Chem. Scand., 12, (1958) 1415.

105. E.H. Roseboom, J. Econ. Geol., 61, (1966) 641.

106. C. Manolikas, P. Delavignette and S. Amelinckx, Phys. Stat. Solidi (a), 33, (1976) K33.

107. G.J. Russell and J. Woods, Phys. Stat. Solidi (a), 46, (1978) 433.

108. J. Dieleman, Ref.80, p.92.

109. W. Palz, J. Bessan, D.T. Nguyen and J. Vedel, Proc. 9th IEEE Photovoltaic Specialists Conf. (IEEE, New York, 1972), p.91.

110. T.S. TeVelde and J. Dieleman, Philips Res. Rep., 28, (1973) 573.

111. H. Rau, J. Phys. Chem. Solids, 28, (1967) 903.

112. B.J. Mulder, Phys. Stat. Solidi (a), 18, (1973) 633.

113. R.W. Glew and F.J. Bryant, Thin Solid Films, 29, (1975) 269.

114. A. Rothwarf and H. Windawi, IEEE Trans. Electron Devices, ED-28, (1981) 64.

115. W.D. Gill and R.H. Bube, J. Appl. Phys., 41, (1970) 1694.

116. B.J. Mulder, Phys. Stat. Solidi, (a), 13, (1972) 79.

117. L.D. Partain, J.J. Oakes and I.C. Greenfield, ref.80, p.346.

118. F. Guastavino, H. Luguet and J. Bougnot, Proc. Int. Conf. "The Sun in the Service of Mankind", Paris, (1973) (CNES, Bretigny Sur Orge, 1973).

119. J. Bougnot, F. Guastavino, S. Couve-Duchemin and M. Savelli, ref.80, p.327.

120. H.M. Windawi, ref.80, p.177.

121. J. Schewchun, J.J. Loferski, A. Wold, R. Arnote, E.A. Demeo, R. Beaulieu, C.C. Wu and H.L. Hwang, Proc. 11th IEEE Photovoltaic Specialists Conference, (IEEE, New York 1975) p.482.

122. K.W. Boer and J. Phillips, Proc. 9th IEEE Photovoltaic Specialists Conf. (IEEE, New York, 1972) p.125.

123. F. Pfisterer, G.H. Hewig and W.H. Bloss, Proc. 11th Photovoltaic Specialists Conf. (IEEE, New York, 1975) p.461.

124. S. Duchemin, F. Gustavino and C. Raisin, Solid-State Commun., 26, (1978) 26.

125. S. Salkalachen, S. Jatar, A.C. Rastogi and V.G. Bhide, Solar Cells, 3, (1981) 341.

126. R. Hill and I.A.S. Edwards, Vacuum, 27, (1977) 277.

127. M.K. Mukherjee, F. Pfisterer, C.H. Hewing, H.W. Schock and W.H. Bloss, J. Appl. Phys.,48, (1977) 1538.

128. A.N. Casperd and R. Hill, Proc. 1st Comission of European Communities Conference on Photovoltaic Solar Energy, Luxembourg, Sept. 27-30, (1977) p.1131.

129. G.H. Hewing and W.H. Bloss, Proc. 12th IEEE Photovoltaic Specialists Conf. (IEEE, New York 1976) p.483.

130. W.D. Gill and R.H. Bube, J. Appl. Phys.,41, (1970) 3731.

131. T.S. TeVelde, Solid State Electron, 16, (1973) 1305.

132. B.G. Caswell and J. Woods, Phys. Stat. Solidi, (a) 44, (1977) K.47.

133. B. Baron, A.W. Catalano and E.A. Fagen, Proc. 13th IEEE Photovoltaic Specialists Conf. (IEEE, New York, 1978) p.496.

134. R.B. Hall and J.D. Meakin, Thin Solid Films, 63, (1979) 203.

135. W.E. Devaney, A.M. Barnett, G.M. Storti and J.D. Meakin, IEEE Trans. Elec. Dev., ED-24 (1979) 205.

136. IEC Quarterly Reports XS-9-8309-1-06 University of Delaware, (1981).

137. W. Palz, J. Bessom, N. Duy and J. Vedel, Proc. 10th IEEE Photovoltaic Specialists Conference, (IEEE, New York, 1973), p.69.

138. K. Bogus and S. Mattes, Proc. 9th IEEE Photovoltaic Specialists Conf. (IEEE, New York, 1972) p.106.

139. W.H. Bloss and G.H. Hewing, 14th IEEE Photovoltaic Specialists Conf. (IEEE, New York, 1980) p.287.

140. R.L. Clarke, J. Appl. Phys., 30, (1959) 957.

141. W. Szeto and G.A. Somorjai, J. Chem. Phys.,44, (1966) 3490.

142. G.A. Sullivan, Phys. Rev., 184, (1969) 796.

143. R.K. Purohit, B.L. Sharma and A.K. Sreedhar, J. Appl. Phys.,40, (1969) 4677.

144. K.J. Matysik and F.G. Ramos, J. Vac. Sci. Technol, 18, (1981) 372.

145. V.G. Bhide, S. Salkalachen, A.C. Rastogi, C.N.R. Rao and M.S. Hegde, J. Phys. D., 14, (1981) 1647.

146. J.D. Meakin, ref.80 p.75.

147. M. Iwami, S. Kim, I. Matsuo and A. Hiraki, J. Cryst. Growth, 45, (1978) 467.

148. J. Morimato, Jap. J. Appl. Phys., 19, (1980) L.296.

149. N. Takagi, H. Yamada, M. Tanaka and K. Tasai, Jap. J. Appl. Phys., 17, (1978) 1155.

150. P.N. Keating, J. Appl. Phys., 36, (1965) 564.

151. J. Woods and J.A. Champion, J. Electron and Control, 7, (1959) 243.

152. H.G. Grimmeiss and R. Memming, J. Appl. Phys., 33, (1962) 2217.

153. R. Williams and R.H. Bube, J. Appl. Phys., 31, (1960) 968.

154. L.R. Shiozawa, G.A. Sullivan and F. Augistine, Proc. 7th IEEE Photovoltaic Spec. Conf. (IEEE, New York 1968) p.39.

155. R.J. Mytton, Brit. J. Appl Phy.,1, (1968) 721.

156. P.F. Lindquist and R.H. Bube, J. Appl. Phys., 43, (1972) 2839.

157. A. Rothwarf, ref.80, p.9.

158. S. Martinuzzi, O. Mallen and T. Cabot, Phys. Stat. Solidi (a), 36, (1976) 227.

159. H. Luquet, L. Szepessy, J. Bougnot, M. Savelli and F. Guastavino, Proc. 11th Photovoltaic Specialists Conf. (IEEE, New York, 1975), p.445.

160. S. Martinuzzi and O. Mallem, Phys. Stat. Solidi, (a), 16, (1973) 339.

161. A.R. Riben and D.L. Feucht, Int. J. Electron, 20, (1966) 583.

162. L.C. Burton and T.L. Hench, Appl. Phys. Lett., 29, (1976) 612.

163. N.C. Wyeth and A. Rothwarf, J. Vac. Sci. Tech., 16, (1979) 1402.

164. S.M. Sze, "Physics of Semiconductor Devices", 2nd Edition by John Wiley & Sons, Inc. (1981).

165. A.G. Milnes and D.L. Feucht, Heterojunction and Metal Semiconductor Junctions, Academic Press, New York (1972).

166. B.L. Sharma and R.K. Purohit, Semiconductor Heterojunctions, Pergamon, London (1974).

167. H.C. Casey and H.B. Panish, "Heterojunctions Lasers", Academic Press, New York, (1978).

168. S.J. Fonash, "Photovoltaic Devices", C.R.C. Critical Reviews in Solid State and Materials Sciences, (1980).

169. M.P. Shaw, Handbook on Semiconductors, Vol.4, Ed. C. Hilsum, North Holland Publishing Co., Chapter 1, "Properties of Junctions and Barriers", (1981).

170. R.J. Anderson, Solid-State Electron, 5, (1962) 341.

171. U. Dolega, Z. Naturforsch, 18, (1963) 653.

172. C.J.M. Van Opdorp, Proc. Int. Conf. Phys. and Chem. Semicond. Heterojunction and layers structures (Akademia, Kiado, Budapest) (1971) p.58.

173. R.H. Rediker, S. Stopek and J.H.R. Ward, Solid-State Electronics, 7, (1964) 621.

174. P.C. Newman, Electronics Letters, 1, (1965) 265.

175. R.L. Anderson, Proc. Int. Conf. Phys. and Chem. Semicond. Heterojunction and layers structures (Akademia, Kiado, Budapest) (1971), p.55.

176. N.F. Mott, Cambridge Phil. Soc., 34, (1938) 568.

177. J. Bardeen, Phys. Rev., 71, (1947) 717.

178. E.H. Rhoderick, "Metal Semiconductor Contacts", Oxford University Press, Oxford (1978).

179. R.F. McQuart and D.L. Pulfrey, J. Appl. Phys., 47, (1976) 2113.

180. L.C. Olsen and R.C. Bohara, Proc. 11th IEEE Photovoltaic Specialists Conf. (IEEE, New York, 1975) p.381.

181. Y.M. Yeh and R.J. Strirn, Proc. 11th IEEE Photovoltaic Specialists Conf. (IEEE, New York, 1975), p.391.

182. D.R. Lillington and W.G. Townsend, Appl. Phys. Lett., 27, (1976) 978.

183. S.J. Fonash, J. Appl. Phys., 46, (1975) 1286.

184. S.J. Fonash, J. Appl. Phys., 47, (1976) 3597.

185. R.B. Hall and V.P. Singh, J. Appl. Phys., 50, (1979) 6406.

186. L.V. Hmurcik and R. A. Serway, J. Appl. Phys.,53, (1982) 3830.

187. H.C. Carslow and J.C. Jaeger, in Conduction of Heat in Solids, 2nd ed., Oxford University Press, London (1959).

188. W. Jost, in Diffusion in Solids, Liquids, Cases, Acad. Press, New York (1952).

189. W.R. Runyan, in Silicon Semiconductor Technology, McGraw-Hill, New York (1965).

190. J. Fisher, J. Appl. Phys., 22, (1951) 74.

191. T. Suzoka, Trans. Jap. Inst. of Metals, 2, (1961) 25.

192. A.D. LeClaire, Brit. J. Appl. Phys., 14, (1963) 351.

193. R.T.P. Whipple, Phil. Mag., 45, (1954) 1225.

194. H.S. Levine and C.J. Maccalum, J. Appl. Phys., 31, (1960) 595.

195. G. A. Somorjai and D.W. Jepsen, J. Chemical Phys., 41, (1964) 1389.

196. For example, J.W.S. Hearle, J.T. Sparrow and P.M. Cross, The Use of Scanning Electron Microscope, (1972).

197. P. Auger, J. Phys. Radium, 6, (1925) 205.

198. C.C. Chang, Surface Science, 25, (1971) 53.

199. K.P. Sinha and M. Didomenico, Phys. Rev., (1970) 2623.

200. R.W. Glew, Ph.D Thesis, University of Hull, (1975).

201. F. Pfisterer, G. Bilger, H.W. Schock and W.H. Bloss, Sun-Energy Conference, New Delhi, (1978) (Oxford:Pergamon) p.670.

202. J.A. Bragagnolo, 13th IEEE Photovoltaic Specialists Conference, (IEEE, New York, 1978) p.412.

203. J.D. Meakin, International Electron Devices Meetings, 4-6 Dec. 1978 (New York, IEEE 1978) p.235.

204. R.E. Halsted, Physics and Chemistry of II-VI Compounds, ed. M. Aven and J.S. Prener, North Holland Publishing Co., Amsterdam, (1967), Chapter 8.

205. D.I. Dimova, M.S. Lakova, M.G. Kalitsova and D.G. Ivanova, Bulg. J. Phys., 6, (1979) 544.

206. W. Palz, G.C. Solal, J. Vedel, J. Fremy, D.T. Nguyen and J. Valerio, Proc. 7th IEEE Photovoltaic Spec. Conf. (IEEE, New York, 1968) p.54.

207. P.F. Lindquist and R.H. Bube, J. Electrochem. Soc., 119 (1972) 936.

208. A. Rothwarf, Proc. 12th IEEE Photovoltaic Spec. Conf. (IEEE, New York, 1976) p.488.

209. T. Singer and P.A. Faeth, Appl. Phys. Lett., 11, (1967) 130.

210. R.W. Buckley and J. Woods, J. Phys. D., 7, (1974) 663.

211. IEC Quarterly Report XS-9-8309-1-06, April (1981) (University of Delaware, U.S.A.)

212. IEC Quarterly Report XS-9-8309-1-07, August (1981) (University of Delaware, U.S.A.)

213. M.J. Robertson and J. Woods, Proc. 2nd E.C. Photovoltaic Solar Energy Conf. (Dordrecht:Reidel), 1979 p.909.

214. W.H. Bloss and G.H. Hewing, Proc. 14th IEEE Photovoltaic Solar Energy Conf. (New York, IEEE) (1980), p.287.

215. A. Rothwaf and A.M. Barnett, IEEE Trans. Electron Dev., ED-24 (1977) 381.

216. K.W. Boer, Phys. Rev., 13, (1976) 5373.

217. D.V. Lang, Appl. Phys., 45, (1974) 3023.

218. D.V. Lang, Thermally Stimulated Relaxations in Solids, Chapter 3, Ed. E.P. Braunlich, Springer-Verlag, Berlin (1979).

219. E. Eser, Quarterly Report "Critical Studies in Materials and Durability", Subcontract XS-9-8310-1 (Prime Contract EG-77-C-01-4042) September (1979).

220. F. Pfisterer, H.W. Schock and G.H. Hewing, Proc. 2nd E.C. Photovoltaic Sol. Energy Conf., Berlin (1979) p.352.

221. J.V. Florio, K.J. Matysik and F.G. Ramos, Proc. 15th IEEE Photovoltaic Specialists Conf. (IEEE, New York, 1981) p.793.

222. T. Suda and S. Kurita, J. Appl. Phys., 50, (1979) 483.

223. W. Haines and R. Bube, 14th IEEE Photovoltaic Spec. Conf. (IEEE, New York, 1980) p.718.

224. D.L. Vassilevskii, V.V. Serdyuk and G.G. Chemeresyuk, Sov. Phys. Semicond., 9, (11) (1975) 1351.

225. H.R. Zwicker, L.A. Brickman, H.C. Hadley and K.J. Matysik, 15th IEEE Photovoltatic Spec. Conf. (IEEE, New York, 1981).

226. W. H. Bloss and F. Pfisterer, 5th E.C. Photovoltaic Solar Energy Conf. (1983), p.728.

227. F. J. Bryant, Radiation Effects, 65, (1982) 81.