

**THE UNIVERSITY OF HULL**

**Conformability Analysis for the Control of Quality Costs in  
Electronic Systems**

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**by**

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## **Abstract**

The variations embodied in the production of electronic systems can cause that system to fail to conform to its specification with respect to Critical to Quality features. As a consequence of such failures the system manufacture may incur significant quality costs ranging from simple warranty returns up to legal liabilities. It can be difficult to determine both the probability that a system will fail to meet its specification and estimate the associated cost of failure. This thesis presents the Electronic Conformability Analysis (*eCA*) technique a novel methodology and supporting tool set for the assessment and control of quality costs associated with electronic systems. The technique addresses the three main elements of production affecting quality costs associated with electronic systems which are functionality, manufacturability and testability. Electronic Conformability Analysis combines statistical performance exploration with process capability indices, a modified form of Failure Modes and Effects Analysis and a cost mapping procedure. The technique allows the quality costs associated with design and manufacture induced failures to be assessed and the effectiveness of test strategies in reducing these costs to be determined. Through this analysis of costs the technique allows the potential trade-offs between these costs and those associated with design and process modifications to be explored. In support of the Electronic Conformability Analysis technique a number of new analysis tools have been developed. These tools enable the methodology to cope with the specific difficulties associated with the analysis of electronic systems. The technique has been applied to a number of analogue and mixed signal, safety critical circuits from automotive systems. These case studies have included several different levels of system complexity ranging from relatively simple transistor circuits to highly complex mechatronic systems. These case studies have shown that the technique is effective in a commercial design and manufacturing environment.

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## **Definition of Terms**

$\sigma$  - Sigma, 1 standard deviation of the normal (Gaussian) distribution

$6\sigma$  - Six Sigma

ANOVA – Analysis of Variance

C – Capacitor

CA – Conformability Analysis

CDF – cumulative distribution function

CoQ – Cost of Quality

$C_p$  – Process Capability

$C_{pk}$  – Process Capability Index

CTQ – Critical to Quality

CV – Control Variates

DFM – Design for Manufacture

DFQ – Design for Quality

DFSS – Design for Six Sigma

DFT – Design for Test

DMADV – Define Measure Analyse Design Verify

DMAIC – Define Measure Analyse Improve Control

DOE – Design of Experiments

DPMO – Defects Per Million Opportunities

eCA – electronic Conformability Analysis

FMEA – Failure Modes and Effects Analysis

Gauge R & R – Gauge Repeatability and Reliability

IC – Integrated Circuit

LSL – Lower Specification Limit

MC – Monte Carlo

Mean – the arithmetic average of a sample

NSL – Nearest Specification Limit

PCA – Principle Component Analysis

PCB – Printed Circuit Board

PDF – probability distribution function

$P_p$  – Process Performance

$P_{pk}$  – Process Performance Index

PPM – Parts Per Million

**QMS – Quality Management System**

**R – Resistor**

**R<sub>A</sub> – Region of Acceptability**

**R<sub>T</sub> – Region of Tolerance**

**SIPOC – Supplier Input Process Output Customer**

**SPC – Statistical Process Control**

**SPICE / HSPICE / PSPICE – Circuit Simulators**

**TP – Test Point**

**TQM – Total Quality Management**

**USL – Upper Specification Limit**

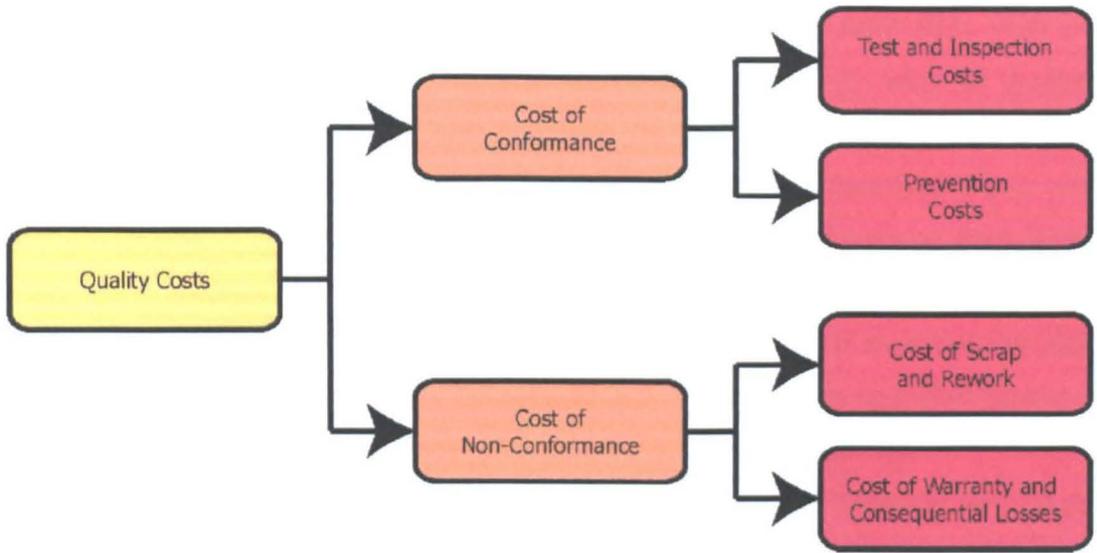
**VOC – Voice of the Customer**

# **1 Introduction**

The development and manufacture of new electronic products is both a competitive and expensive process. New designs must reach production faster than ever before whilst at the same time attaining higher standards of reliability over longer lifetimes with lower production costs. The movement from the traditional linear approach to design to concurrent engineering systems has in many ways helped to ease the problems of product development and manufacture. By its very nature concurrent engineering facilitates and to a certain extent requires communication between different engineering teams dealing with different aspects and phases of design and production. At the same time running alongside the general transfer to concurrent engineering systems has been the development, introduction and wide scale corporate acceptance of modern quality engineering tools. This has been partly in an effort to support the transfer to new methods of working as well as serving the more general aim of improving product quality.

## **1.1 A Definition of Quality**

Before continuing it is necessary to provide a definition of quality as quality means different things to different people. However for the purpose of this work and with regard to engineering products, quality may be defined as the level of customer satisfaction with regard to a specific process or product. We must also distinguish between quality and grade, for example consider a train journey, the class of ticket purchased defines the grade of the experience whilst the Quality of the experience is defined by the Critical to Quality factors such as time of journey and promptness of service. Further to this consider that the level of quality of a particular manufacturing process is a function of the proportion of defect free products produced by that process. In association with this idea of quality is the concept of the 'Cost of Quality'. The Cost of Quality may be defined as those costs experienced by an organisation in ensuring its customers have both a high perceived and actual level of quality. Such costs of quality may be due to a number of factors including, for example, extended development times, cost of process control, cost of test implantation and the cost of scrap and rework this is illustrated below in Figure 1-1, a detailed discussion of the components of each of these costs may be found in [B1].



**Figure 1-1 Illustration Demonstrating the Various Manifestations of Quality Costs**

The potential benefits brought by the knowledge of quality costs associated with an electronic system at the various stages of its development are wide ranging and include:

- Providing a driving force for the development of a more robust design
- Making engineers aware of the impact of design decisions
- Reducing production lead times
- Reducing both internal and external failure costs
- Allowing the comparison of different designs

## **1.2 The Development of Quality Management**

Quality management and engineering techniques have been developed over the last century and stem largely from the work of Deming and Juran [B2], and the introduction of Statistical Quality Control (SQC) tools in America during World War Two (WWII). Initial SQC techniques were introduced to ensure the quality of the mass manufactured weapons systems. The adoption of SQC was a necessary part of the weapons production regime which forced the ultimate producers of the end product to use numerous different suppliers and contractors in order to compress the effective time to production, this was the first large scale adoption of a vertically integrated manufacturing strategy. Significant advances were made towards modern quality management techniques during this period and they contributed greatly to the war effort in general. In the post war years American corporations forgot or discarded the lessons in quality they had learned during the war years and returned to the horizontal strategies they had pursued during the pre-war years. At the same time the economies of the defeated nations had to be rebuilt and in an effort to help the territories under his control General McArthur

took some of the now underused SQC experts from the America to Japan [B3]. With the Japanese cultural predisposition to product improvement, Deming's ideas of product quality and quality improvement spread quickly. The impact of Deming's work is now obvious; from a standing start after WWII with its industries destroyed Japan was producing cheap high quality goods by the 1970's. The growth did not stop there, it has continued to increase. The general opinion of Japanese products is now extremely good with most people agreeing that they are very desirable and of an exceptionally high quality. This is in direct contrast to the position only a few decades ago when Japanese produce was considered of extremely poor quality and highly undesirable.

Against this backdrop the semiconductor industry emerged and started to develop in America with Silicon Valley companies producing the very first Microprocessor devices. Despite the excellence of engineering of many of the aspects of the new semiconductor industry, companies still did not have good quality management systems and many of the manufactured devices would fail immediately on or soon after delivery to a customer. As Japanese companies began to catch up with the American semiconductor manufactures the first improvements they made were not in the functionality of devices but in the quality of the produce. Hence companies purchasing the microprocessors had a simple choice either purchase, a device from American companies and look on whilst many of the final products failed or switch to Japanese supplies whose devices experienced failure rates of up to 1000 times less than the American competitors. In a direct reaction to this throughout the 1980's American companies performed numerous studies of Japanese Quality practices and attempted to re-learn the techniques they had lost to Japan [B2]. From these studies US companies realised that a holistic strategy was necessary, covering all aspects of company operations. It was within this atmosphere of a desperate search for a new quality improvement methodology that Motorola developed the Six Sigma Strategy in the early 80's [B4] after a visit to Japan by Motorola's director of quality Richard Buetow. Since the development of the technique by Motorola the resulting success caused it to be adopted by other leading manufacturing and service companies including G.E. Citicorp, Allied Signal, Dupont and Black & Decker the result of this has been a surge in interest for the technique and a wide spread adoption by other companies.

### **1.3 What Is Six Sigma?**

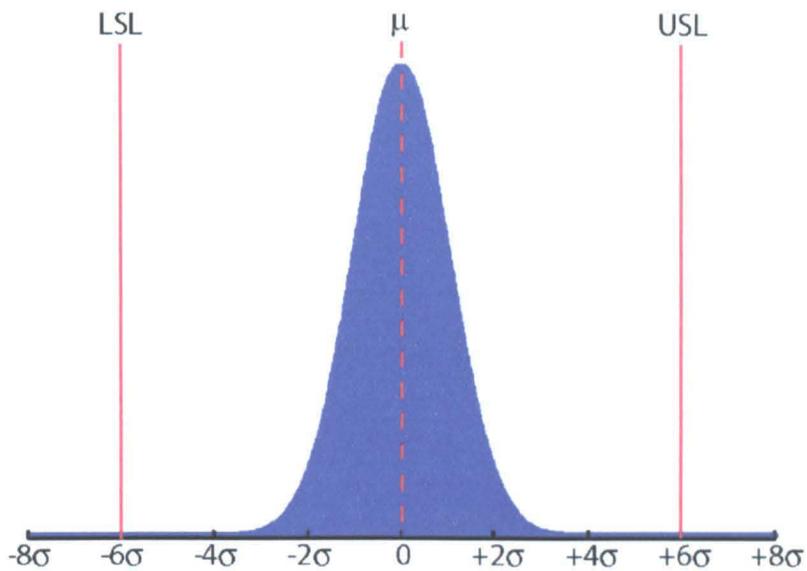
Six Sigma is a structured, statistical data driven methodology which is focused on improving business performance by increasing the quality of processes. Six Sigma provides a number of different things to its users including:

- A symbol ( $6\sigma$ )
- A metric ( $6\sigma$ )
- A goal (zero defects)
- A vision
- A philosophy
- A methodology

Many people believe Six Sigma to be similar to or the same as Total Quality Management (TQM), however this is not correct as TQM is a circular process with no clearly defined goal whilst Six Sigma is a spiralling process with the clear goal of achieving zero defects and hence total customer satisfaction [B5;B6]. Six Sigma does make use of previously developed quality tools including those used by TQM and SPC however it adds to these through the addition of a clear idea of customer satisfaction. Further descriptions of the Six Sigma methodology may be found in the literature. Good general overviews are given in [B7], [B8] & [B6]. It is important to note that Six Sigma is not an entirely new concept, instead it is a development of previous strategies and methodologies including TQM. We should also note that a large part of the success Six Sigma has achieved is due to the success of its branding and its general focus upon the 'bottom line' which appeals to company management.

### **1.4 Where does 'Six Sigma' come from?**

The Six Sigma methodology was named by Bob Galvin Motorola Corp. CEO [B4] after both the process metric and goal used by the technique. The name is a reference to the standard deviation ( $\sigma$ ) of the Gaussian or Normal distribution. It describes a situation in which process specification limits are set at +/- six standard deviations of an optimal process from the mean ( $\mu$ ) of that processes. This may be visualised with the aid of Figure 1-2.



**Figure 1-2 Normal Distribution and Specification Limits at Six Sigma (LSL - Lower Specification Limit, USL - Upper Specification Limit)**

The figure shows a normal probability density function (PDF) together with its mean and specification limits at  $\pm 6\sigma$ . The significance of this configuration is the extremely low portion of the distribution which is to be found outside of the specification limits. The two tails of the distribution do in fact continue until infinite points from the mean of the distribution and will never meet the axis, yet despite this fact 99.999998% of the distribution is to be found between these limits. This would imply that if we could design a process which had a similar probability distribution to that shown in Figure 1-2 a defect rate (the number of parts produced falling outside the specification limits) of only 2 parts per billion (0.002ppm) would be experienced. This would truly be a desirable situation for any process. However maintaining a process in this condition would be an extremely difficult if not impossible task. Any process will in general experience a number of changes due to operational factors, for example personnel changes and equipment aging. Whilst developing the Six Sigma methodology Motorola realised this and accounted for this fact by allowing for shifts of up to  $1.5\sigma$  by the process mean, which would increase the expected defect rate to 3.4ppm (further details of this calculation may be found in 2.1.3.1) a still considerable achievement which serves as the target for the Six Sigma methodology.

## **1.5 The application of Six Sigma**

The previous section introduced the metric and source of Six Sigma's name, these are central parts of the Six Sigma technique forming its core and ultimate goal. The methodologies for the application of the technique form the substance around this core. Six Sigma may be applied in two different variants depending upon the target which may be either an existing product or a totally new product or product variation. When applying Six Sigma to an existing product the DMAIC [B9;B10] methodology is used, this acronym stands for:

- Define
- Measure
- Analyse
- Improve
- Control

Alternatively when applying Six Sigma for a new product or process, which is known as Design for Six Sigma (DFSS) [B11], the DMADV methodology should be applied, in this case the acronym stands for:

- Define
- Measure
- Analyse
- Design
- Verify

The details of these methodologies and their application are discussed in chapter 1. When applied correctly to suitable projects both of these methodologies are able to produce substantial quality cost savings [B12]. Despite this the penetration of such tools into many companies is a slow process with the job of applying the tools to a process often being seen as the job of external quality experts rather than the job of the process owner. This detached view of operations often leads to poor quality products with associated high quality costs.

## **1.6 Design / manufacturing Interface**

The traditional view of the design / manufacturing interface is a typical example of process detachment. Electronic design engineers traditionally view their job as producing a specification and design for a functional product, and assume that it is the job of production engineers to manage the manufacture of the product and ensure its

quality. Some inroads against this attitude has been made with the general corporate adoption of Six Sigma methodologies, however as of yet many companies have not experienced the significant quality cost reductions they expected with reference to other companies (notably Motorola and GE [B12]) who had adopted the methodologies earlier. This gap between expected and experienced quality cost reduction is due to poor penetration of quality methodologies at the process owner level. To achieve significant quality cost savings in an engineering company the quality methodologies must be adopted by both design and production engineers, and hence bridge the design / manufacture interface. Although current quality methodologies do provide tools to bridge this interface many engineers perceive or find them to be difficult to understand and apply. Due to this lack of confidence in current quality tools penetration at the basic and middle engineering levels has been slow, with little enthusiasm from busy engineers to take up methodologies that will, in the long term, reduce workloads and improve product quality.

### ***1.7 Problem Statement and Aim of the Research***

A corporate will to implement Six Sigma methodologies for the design of electronic products is not enough. To fully experience the benefits of Six Sigma engineers must be willing to take part in the quality processes themselves. To achieve this goal an analysis methodology and supporting tools are required which are easily used and understood with minimal training and which also present results in an accessible and clear manner. Such a methodology and tools should not require significant new knowledge to operate and any mathematical basis should not prove obstructive to its adoption and use by team members. The methodology and tools should fit within the established quality frameworks particularly Six Sigma, however this must not prohibit its use as an independent analysis tool. In response to this need the aim of this research was the development of a new quality methodology addressing the identified issues.

## **1.8 Summary**

Through the use of appropriate quality analysis techniques, particularly Six Sigma, it is possible to significantly reduce the quality costs experienced by an organisation. The large scale success experienced by a small number of companies in applying Six Sigma has prompted a general acceptance of the technique and firmly focused corporate interests on the quality costs associated with poorly considered products. However if process owners either do not understand, use or have time to apply the techniques themselves little benefit can be gained from the methodology. The slow take up of Six Sigma at the process owner level which has been experienced by many companies is due to a general lack of understanding and will to operate complex quality tools. This lack of acceptance may be combated through the introduction of a new methodology which is both compatible with existing methodologies and also suitable for independent use. Any new methodology must also be able to simplify the analysis process in general and present results in an accessible manner.

## **2 Design for Quality Methodologies and Contemporary Tools**

This chapter introduces, compares and contrasts a selection of Design for Quality (DFQ) methodologies and analysis tools. At this point it is convenient to provide a definition of the differences between a methodology and a tool. A methodology may be seen as the overall way of carrying out a strategy for implanting a DFQ project; it provides a specification for the steps to be taken, what should be achieved by each step and tools which may be used at each step. Analysis tools are those things used within the methodology which are used to gather and process the available data, from which conclusions may then be drawn.

### **2.1 Quality Systems, Standards and Methodologies**

#### **2.1.1 ISO9000**

ISO9000 is not a method for implementing quality changes but rather a series of standards through which a corporate quality system may be assessed and accredited. Once accredited as an ISO9000 organisation a company may use the ISO9000 logo on its documents in order to publicize its certification. Although strictly speaking ISO9000 is not a quality methodology it does have a significant impact upon quality methodologies in use within an organisation as it requires that all systems in use encompass certain accountability principles [B13]. This accountability is the key feature of ISO9000 as a Quality Management System (QMS). The standard is concerned with keeping a formal record of an organisations methods for managing the quality of its products [B14]. ISO9000 has been broadly adopted with some organisation refusing to deal with non accredited bodies but its take-up has not been without criticism. The main complaints levelled at ISO9000 is the amount of paperwork involved and that in itself it does little to improve quality. Further to this the records kept by those implementing the QMS may often be forged [B14]. In summary ISO9000 and other QMS do little to directly improve quality instead they provide a process and system to facilitate the application of a quality improvement program, therefore as QMS basically form accountability routes they lie at the very periphery of this work.

## **2.1.2 Total Quality Management**

Total Quality Management (TQM) may be defined as a structured approach to producing an environment which is focused upon customer satisfaction and continuous process improvement. There are numerous different variations upon this definition of TQM to be found in the literature [B15;B7;B16], many of which will embellish the definition with other attributes, but all have the common factors of customer satisfaction and continuous process improvement. Despite these common themes which run through the various possible definitions of TQM it is obvious that there is no true formal definition for the methodology [B17], which often makes it difficult to implement and successfully apply. This disparity between different definitions of the methodology is largely due to its organic development from Japanese methods which was carried out by numerous different quality consultants. Despite the obvious problems caused by the lack of a standardised definition for TQM, the methodology has provided significant quality gains for a number of companies. The implementation of TQM is supported by seven principle tools [B18;B7;B19]

- Cause and Effect Diagrams (fishbone plots)
- Check Sheets
- Pareto charts
- Control Charts
- Histograms
- Scatter Diagrams
- Run Charts

These tools, which aid the user in identifying the causes of process failure and facilitate subsequent process control, are well documented in the literature [B20;B21] which should be consulted for further details. TQM has in the past and is still currently widely practiced with a number of companies experiencing considerable success [B22] in quality improvement and the reduction of quality costs through its application. However numerous TQM projects have also failed. Often failures can be attributed to the extremely empirical approach TQM takes and also to its lack of a definite realisable target for the process being managed. Instead TQM has only the general aim of achieving zero defects [B13] an often unrealisable goal which may cause the TQM methodology to fail. Further to this in a final breakdown of TQM it essentially implements quality for quality's sake. In summary TQM is a highly structured, empirical system generally aimed at improving existing products and processes which applies a number of standard tools to solve quality problems, towards a final and

unachievable goal of zero defects. Also within TQM, accountability and traceability are provided through the use of good documentation though not to the extent advocated by QMS. With reference to this work TQM provides both useful quality assessment tools and ‘lessons learnt’ regarding its aims and structure. However besides this TQM, as a falling star within the arena of quality improvement, will remain on the periphery of this work.

### 2.1.3 Six Sigma

As TQM is falling in popularity with quality practitioners and organisations, Six Sigma is rising to replace it as the most popular quality methodology. Six Sigma is, as was stated in the introduction, a “structured, statistical data driven methodology which is focused on improving business performance by increasing the quality of processes”. The methodology originally developed by Motorola [B23;B9] spread quickly to other organisations [B24;B9] who saw its value in terms of the quality cost savings it allowed Motorola to make. Six Sigma has now been widely adopted and applied, achieving large quality cost savings along the way [B24]. Despite this it is frequently argued that, as Six Sigma uses many if not all of the quality tools employed by other quality movements and TQM in particular, it brings nothing new except perhaps branding. This is however untrue Six Sigma is fundamentally different from previous quality movements due to its emphasis upon realising business gains and not just quality for its own sake [B5;B6;B24;B25]. The methodology is implemented through one of two different frameworks depending upon the task at hand. These are DMAIC and DMADV [B26] as shown in Table 2-1, and explained below in section 2.1.3.1.

D	Define	D	Define
M	Measure	M	Measure
A	Analyse	A	Analyse
I	Improve	D	Design
C	Control	V	Verify

**Table 2-1 The definition of DMAIC and DMADV**

The crucial Define stage, of which the first step is to produce a project charter [B27], present in both variants of the Six Sigma methodology provides the strong emphasis upon achieving business gains in the real terms of cost savings which differentiate the Six Sigma method from previous quality movements. Further to this Six Sigma is differentiated from other older quality movements through the organisational changes it prescribes, particularly through the Six Sigma training scheme which requires a large

scale adoption of the techniques and appointment of Black Belts and Master Black Belts who serve as leaders and consultants for the application of Six Sigma within an organisation [B23]. This is fundamentally different to other methodologies which in general rely upon a 'Quality Department' to provide quality leadership within a company or organisation.

Six Sigma is also differentiated by its use of metrics which allow for the provision of target values for the processes under study. The original and perhaps the most controversial six sigma process quality metric is process sigma. When using this metric the goal of the methodology is to achieve and sustain a  $6\sigma$  process, this aspect of the methodology was briefly discussed in the introduction but will be further explored at this point.

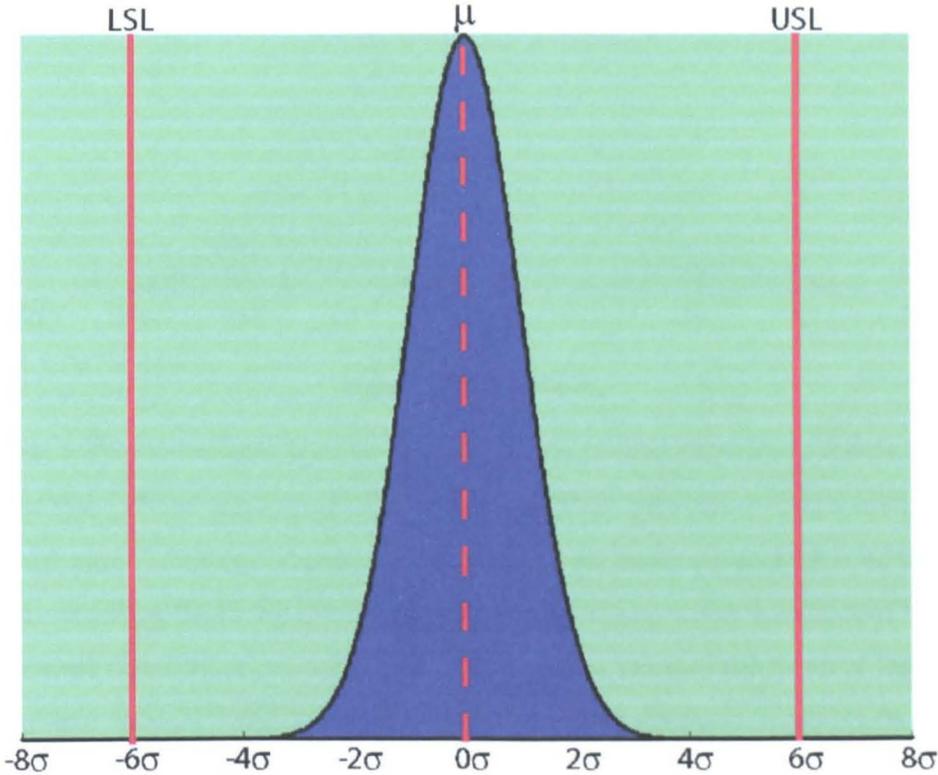
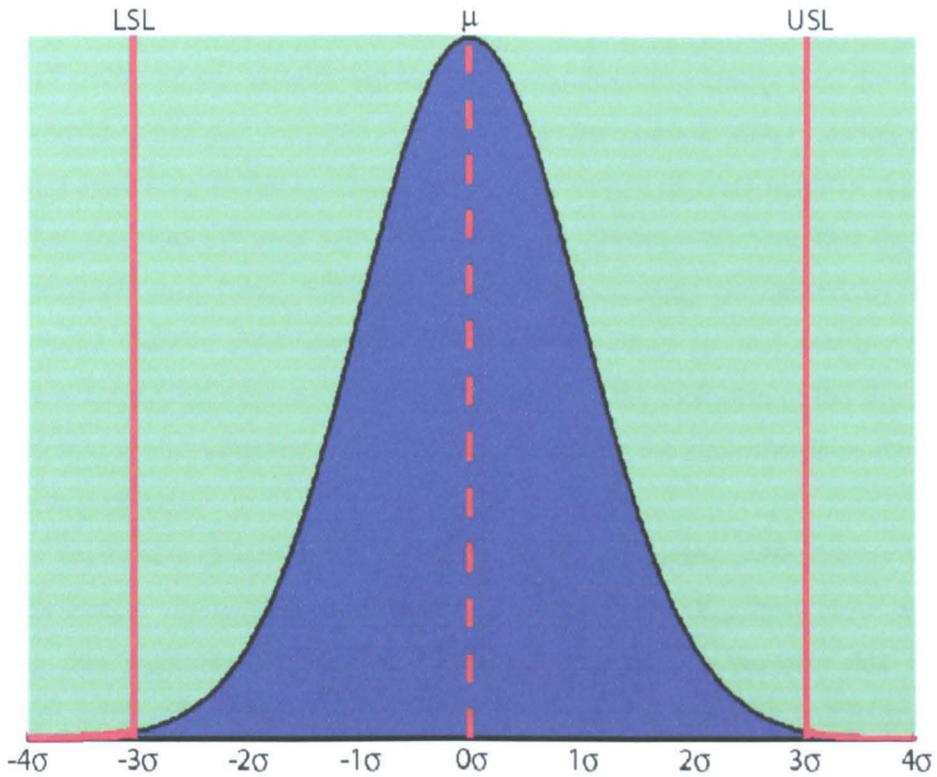


Figure 2-1 A Centred Six Sigma Process

Figure 2-1 shows a  $6\sigma$  process as defined by the ratio of the standard deviation of the process variance to the specification limits. Consider the traditional goal of operating a process at a  $3\sigma$  quality level. To meet this goal the standard deviation ( $\sigma$ ) of the process must be small enough so that the process distribution fits within the specification limits (LSL & USL) when the mean of the process distribution ( $\mu$ ) equals the nominal value

for the process. Hence the maximum allowable variation ( $\sigma$ ) for such a process is  $\sigma = \frac{(USL - LSL)}{6}$ , Figure 2-2 shows a process operating in such a mode.

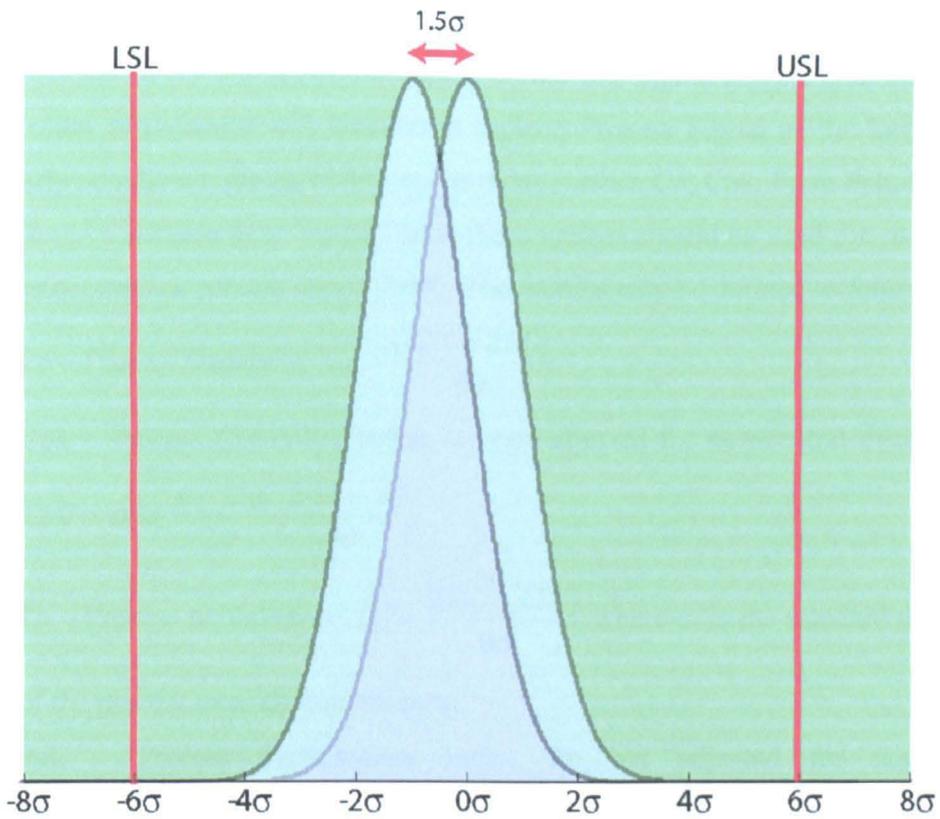


**Figure 2-2 A 3 $\sigma$  Process**

A process with the configuration seen in Figure 2-2 would experience a defect rate of 2700ppm (99.73% of the normal distribution is found between  $\pm 3\sigma$ ) which may be split down into 1350ppm exceeding the specification limits on each side of the mean (the area exceeding the limits is highlighted in red). Now consider the effect of the mean of the process distribution moving away from its target value, if the mean of the process were to drift by only  $1.5\sigma$  then this would cause a massively increased defect rate of around 66,800 ppm. Six Sigma seeks to rectify this problem either by allowing the specification limits to be moved further from the mean to  $\pm 6\sigma$  or by improving the process to reduce the standard deviation to achieve the same situation, as demonstrated in Figure 2-1. The effect of this change is to reduce the expected defect rate for an “on target” process to only 2 ppb, and, for the same process drift of  $1.5\sigma$ , to only 3.4ppm: a significant improvement which leads to significantly lower quality costs [B4]. Numerous further explanations of this effect may be found in the literature [B8;B28;B7;B12;B29]. Of particular interest at this point is to note the use of the  $1.5\sigma$  adjustment in the specification of a Six Sigma process. Motorola, the initial developers

of the Six Sigma methodology, included this shift based upon historical data describing the average process shift experienced by their own supply chains [B8;B30]. The inclusion of this adjustment factor is seen by some as just a fudge factor with no real scientific basis. However, if we consider that the  $6\sigma$  process specification is essentially a model of reality which, as with any model, vastly simplifies reality then the  $1.5\sigma$  shift may be considered as just a further simplification. An example simplification made by the process modelling is that it effectively captures only a discrete mode of the process distribution and does not take into account the significant variations that the process may experience over time. Typically such variations may be caused by seasonal environmental change, shift changeover, process 'bedding in' and supplier changes. When these considerations are taken into account then the inclusion of the shift may be explained as a useful adjustment which compensates for the simplifications included in the modelling process.

Now that we have a description of the goal of the Six Sigma methodology we must define the metric which provides us with information regarding how close we are to achieving this goal. Six Sigma uses Process Sigma [B7] to perform this function. Calculation of process sigma may be achieved in two ways. Firstly and perhaps most popularly it may be calculated from the defect rate of a process using standard tables [B29;B31], through a simple calculation [B32] or alternatively using a simple computer program [B33]. This method is simple and generally effective, however for low defect rates the method becomes inaccurate and it is necessary to use an alternative calculation technique [B7]. Alternative techniques are based upon direct use and analysis of the statistical properties of the normal distribution rather than tables describing them.



**Figure 2-3 Example Process Distribution Showing a  $1.5\sigma$  Mean Shift**

Such a technique will now be outlined. With reference to Figure 2-3 we may calculate Z for each of the specification limits, as shown

$$Z_{LSL} = \frac{(LSL - \mu)}{\sigma} \quad (1)$$

$$Z_{USL} = \frac{(USL - \mu)}{\sigma} \quad (2)$$

Now using suitable software (e.g. Matlab, Excel) calculate the probability of the process producing an outcome between the specification limits

$$P_{sl} = \text{normcdf}(Z_{usl}, 0, 1) - \text{normcdf}(Z_{lsl}, 0, 1) \quad (3)$$

Now convert this probability into a single sided Z value

$$Z_{ss} = \text{norminv}(P_{sl}, 0, 1) \quad (4)$$

Process sigma may now be calculated by adding 1.5 to this number

$$PS = Z_{ss} + 1.5 \quad (5)$$

Process Sigma is a key metric for the Six Sigma methodology; it allows objective decisions to be made regarding the viability and suitability of a process. Despite this,

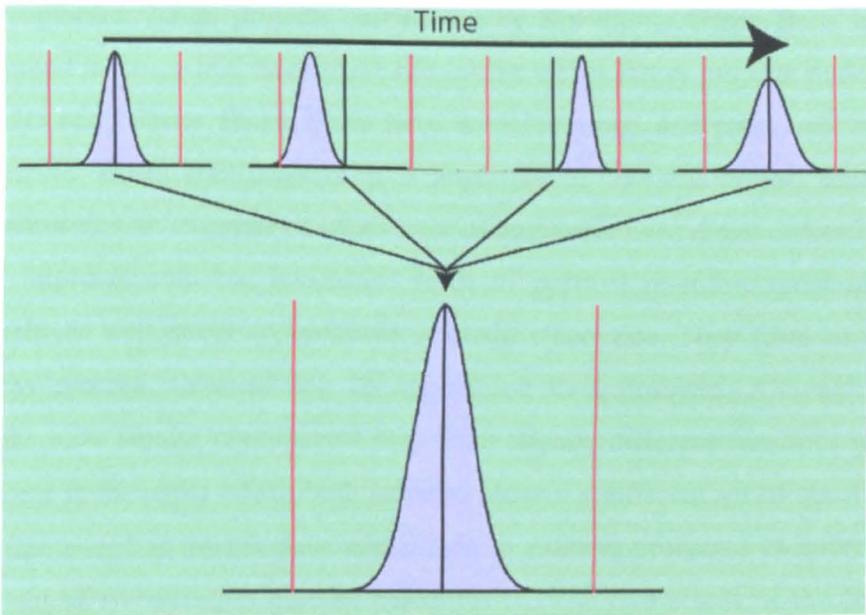
due to the somewhat controversial nature of the previously discussed  $1.5\sigma$  adjustment, alternative metrics are also commonly used within Six Sigma [B4]. These alternative metrics often complement and sometimes replace Process Sigma as the key metric. Particularly popular are the capability and process metrics  $C_p$ ,  $C_{pk}$ ,  $P_p$  &  $P_{pk}$ ; however there is some confusion as to exactly what these indices should be used for and if they can or cannot replace process sigma [B34]. The metrics may be defined as follows:

- $C_p$  – Process Capability  $C_p = \frac{(USL - LSL)}{6\sigma}$
- $C_{pk}$  – Process Capability Index,  $C_p$  but adjusted for non-central distributions  

$$C_{pk} = \min\left(\frac{\mu - LSL}{3\sigma}, \frac{USL - \mu}{3\sigma}\right)$$
- $P_p$  – Process performance  $P_p = \frac{(USL - LSL)}{6\sigma_i}$  where  $\sigma_i$  is the standard deviation of the process over all time till now.
- $P_{pk}$  – Process Performance Index,  $P_p$  but adjusted for non-central distributions  

$$P_{pk} = \min\left(\frac{\mu - LSL}{3\sigma_i}, \frac{USL - \mu}{3\sigma_i}\right)$$

The interpretation of these definitions is aided by consideration of Figure 2-4.  $C_{pk}$  the process capability index is the  $6\sigma$  range of a processes spread with reference to customer specifications and it indicates what a process is able to achieve given that it remains in statistical control. In contrast  $P_{pk}$  the process performance index, measures current process performance based upon current or historical data and should only be used to compare with  $C_p$  or  $C_{pk}$  to define what changes should be made to a process to ensure that it meets its potential capability [B35;B36;B37;B38;B39].



**Figure 2-4 The Difference Between Ppk and Cpk, Cpk Relates to the Current Process Distribution as Shown by the Small Distributions Whilst Ppk Relates to the Overall Distribution which is an Amalgamation of all of the Data**

Now that the meaning of these metrics has been established the question of using them in place of process sigma must be considered. Process sigma is the original metric for use in Six Sigma however as already stated many consider that the  $1.5\sigma$  adjustment and hence the use of this metric may be unsound for that reason alone. Secondly, the  $1.5\sigma$  adjustment also implies that a process may never be optimized past this point. As an alternative metric Cpk suffers from neither of these problems and in fact has the advantage that it may be used to encourage suppliers to improve their processes. Further to these points it is worth noting that it is an established fact that older more established processes suffer from less variability than new processes. Often this is due to a “bedding” down of the process, process sigma would make no allowance for this fact whilst Cpk can. Further discussion of the conflicts between process sigma and process capability may be found in the literature [B8], however for now the balance of opinion is in favour of the Cpk measure not only due to its greater flexibility than process sigma but also as it is more widely understood, and in general allows the same decisions to be made regarding a process as would be made using process sigma.

### 2.1.3.1 DMAIC and DMADV

DMAIC and DMADV provide the frameworks for the application of the Six Sigma methodology to both existing and new products. The pattern of application for Six Sigma is project based and each project is taken up by a Six Sigma trained engineer or

team of engineers. Initial projects carried out by Six Sigma Green Belts tend to be tightly limited in scope and have short life cycles whilst larger projects undertaken by Black Belts and Master Black Belts have a wider scope and may well encompass several smaller Green Belt projects. It is important to note this project based system which ensures that an engineer or small team of engineers have direct ownership of any proposed improvements and successes, leads to positive re-enforcement of the Six Sigma cycle, as well direct appointment of credit where due. They form an important part of the process, standardising its application to a problem. Although the two frameworks have similar components they form slightly different functions within the two different frameworks which both serve to answer a different set of questions. The DMAIC framework is intended for application to existing processes to improve them, reducing out of specification process performance. The five stages of the framework may be defined as follows [B40;B9;B10]:

- **Define:** The aim of this stage is to set out the scope and goals of the project whilst gaining background information on the process, its owners and customers. Two main tools are used during the definition stage; these are Supplier Input Process Output Customer (SIPOC) charts to help define the process and Voice of Customer (VOC) forms to define the Critical to Quality (CTQ) functions.
- **Measure:** During this stage the aim is to focus the process improvement by gathering information about its current state. A number of different tools and techniques are used during this stage including the following: data funnelling, Gauge R & R and process capability studies.
- **Analyse:** This stage identifies the causes of process failure and confirms them through structured data analysis. Again a number of tools and techniques are used at this stage of the framework for example Process & Data Doors, Cause and Effects analysis, Regression Analysis, Design of Experiments (DOE) and Hypothesis Testing.
- **Improve:** Here solutions are developed, tested and implemented to address the root cause of the process problems identified during the previous stages.
- **Control:** The final stage of the framework has multiple aims to evaluate and validate any solutions implemented, maintain any gains by standardizing process improvements and finally to define future steps for on going process improvement.

Alternatively DMADV is a Design for Six Sigma (DFSS) framework used not for the analysis, improvement and control of existing products and processes but for the development, analysis and design of new products and processes. The five stage framework and the actions undertaken at each stage may be defined as follows:

- **Define:** Develop process plans and a project charter outlining the business case for the project, its expected benefits and any risks.
- **Measure:** determine the VOC and translate it into a number of CTQ's which should then be prioritised using a technique such as Quality Function Deployment (QFD) (Stage 1) and finally the risks identified during the define stage should be reassessed.
- **Analyse:** identify the key functions and prioritise them (QFD stage 2) generate concepts, using techniques such as brainstorming, and review and evaluate the proposed process and design concepts.
- **Design:** this stage has two sub stages firstly high level design using tools such as QFD stage 3 and secondly detailed design with the aid of QFD stage 4.
- **Verify:** here pilot processes are planned, process management schemes should be defined, pilots should be implemented and verified and finally controlled.

DMADV is not intended to replace the product development and introduction scheme currently in use at an organisation but to strengthen and improve it through the use of an additional structured methodology which brings both a suite of tools and techniques and a strong goal. For example within TRW automotive DMADV is used in combination with the established Global Development and Product Introduction Management (GDPIM) system for product and process design and implementation.

Both of the outlined frameworks are circular, not linear, allowing iterations through the frameworks to take place until the aims of the project set out in the project charter, written in the define stage, are achieved.

Six Sigma applied through the new design and design improvement frameworks can be a highly effective tool for building in quality to new products and adding quality to existing products. The Six Sigma methodology provides both procedural guidance in the form of the application frameworks and quality targets with the process sigma and capability metrics. The main criticism that may be levelled at the Six Sigma methodology and that may also be levelled at TQM and other methodologies is that the techniques require a significant knowledge of statistical tools and techniques to successfully complete a quality assessment and improvement. Even for mathematically literate engineers the statistical tools and level of interaction required by contemporary

quality programmes can seem daunting and obstructive. Six Sigma does go some way to combat this program with its tiered training and support program.

## **2.2 Contemporary Design Assessment Tools**

This section gives an overview of the design quality assessment tools traditionally used during the design of electronic products. Normal practice is for these tools to be applied in isolation of each other and without the explicit aim of decreasing the Cost of Quality (COQ) for the current design. Instead the aim of application often runs parallel to reducing COQ with typical aims being increased yield, better performance, general robustness of design and the derivation of process control limits.

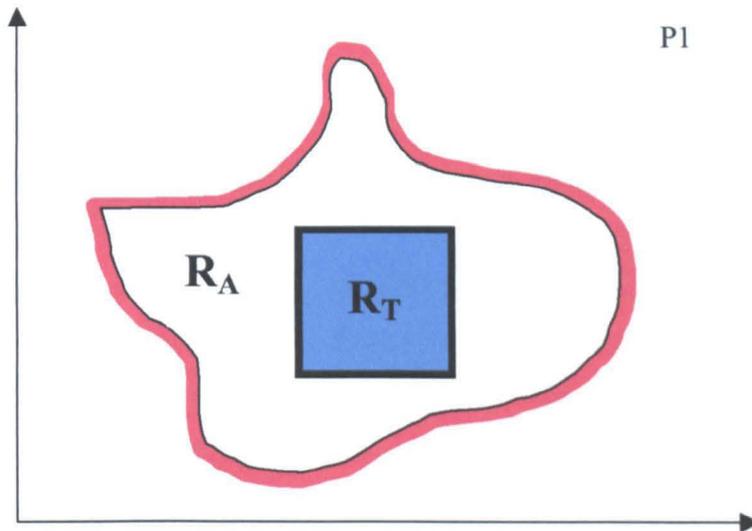
## **2.3 Tolerance Analysis**

Tolerance analysis is an extremely popular form of circuit analysis [B41], the aim of which is to produce designs that are robust against the inevitable statistical variations which occur during the manufacture of a product and hence to prevent the occurrence of parametric failures. In the field of integrated circuit manufacture where tolerance design techniques are mature and widely used these statistical variations may be easily visualised as they take the form of errors such as mask misalignment, variable dopant levels and processing time inaccuracies; whilst in the case of PCB manufacture, where tolerance design techniques although widely used are less mature, we may attribute the majority of parametric failures to performance variations introduced by the statistical variations already present in the commodity parts used to construct a product. This distinction between the almost complete control over process variations in IC manufacture compared to the only partial control existing in PCB manufacture explains the differing levels of maturity of tolerance design techniques between these two areas of electronic design. As already stated the data developed during tolerance analysis is generally targeted at the reduction of parametric faults due to statistical process and component variations however the analysis may also be driven to provide information which allows a design to be optimised for specification conformance and manufacturing yield. Due to the flexibility and power of even basic tolerance design techniques they often take a key role in the development of a new product.

### **2.3.1 Basic Concepts**

Perhaps the most important concept with regard to tolerance design techniques is the relationship between the performance space and the parameter space of a product; the

performance space of a design is the multi-dimensional area specified by the ‘customer’ which defines the bounds of operational acceptability for the product in question. Whilst the parameter space of a product is the multi-dimensional area controlled by the components of a circuit that represents all of the possible outputs for a given circuit. The significance of the relationship between these areas is immediately obvious and if the performance space and parameter space were to be transformed such that they could be represented in the same general space then they might take the form shown in Figure 2-5, where  $R_A$  represents the performance space or Region of Acceptability and  $R_T$  represents the parameter space or Region of Tolerance [B42]. These two regions may or may not overlap. If, as shown in Figure 2-5,  $R_T$  lies wholly within  $R_A$  then the possibility of parametric failures is very low; however if as commonly occurs the two areas do not completely overlap then the possibility of parametric failures will increase to a maximum of one when the two areas are completely non-coincidental.



**Figure 2-5 Example of 2-D Parameter Space**

Hence manufacturing yield can be derived from the relationship between the two regions  $R_A$  and  $R_T$ . As the area of the overlap between the two regions represents the likely fraction of the manufactured circuits that satisfy customer’s specifications, i.e. the percentage of circuits that lie within the performance space. A good definition of tolerance analysis would be that it is the study of the relationship between these two regions, and at the same time tolerance design techniques may be defined as those techniques which aim to ensure that the  $R_T$  exists completely within  $R_A$ .

Figure 2-5 illustrates the simplest form of parameter space, more complex forms exist. Three or more dimensions are the norm for parameter space rather than the simplistic

two dimensional form shown in Figure 2-5. Also disconnected regions may occur when the parameter space is split into 2 or more separate and isolated regions. It is also possible for 'Black Holes' (areas within the performance space that the circuit may not operate within) to exist within the parameter space.

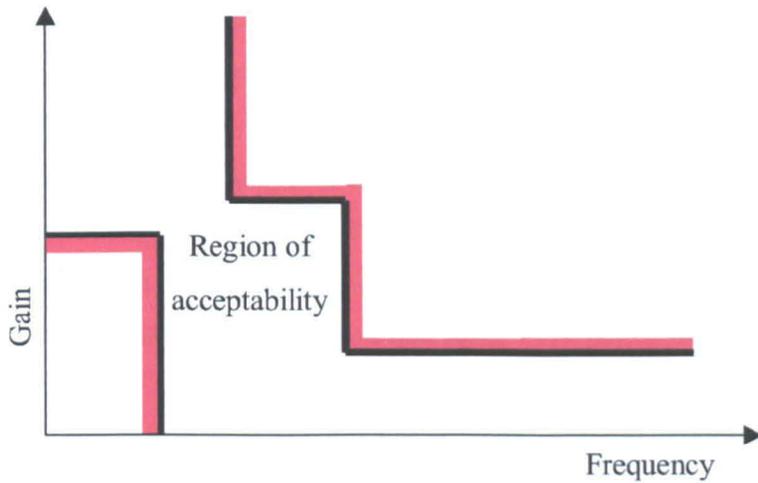


Figure 2-6 Performance Space of a Low Pass Filter

The performance space of a product may be specified in a number of different ways. One possible and popular method often used for the definition of frequency or time dependant performance is graphical and takes the general form illustrated in Figure 2-6. The diagram gives the definition of the acceptable limits of the performance space of a low pass filter. The region of acceptability limits the area into which the output of the filter must fall. However the output may take any form and lie anywhere within this region. For more complex products it is common for the performance space definition to be made using a range of techniques including graphical ones along with numerical descriptions, allowing a more precise definition to be created.

### 2.3.2 Worst Case Tolerance Analysis

Worst case tolerance analysis is, perhaps, conceptually the simplest form of tolerance analysis. Firstly, it does not rely upon complex statistical techniques which attempt to examine all possible component and performance points and secondly the user of the technique is not required to know the shape of a components probability density function. Worst case analysis is carried out by locating the points at which the extremes of circuit operation lie (the vertices). After locating these points the circuit is analysed or simulated at each point. The data collected from these analyses is then examined to determine if the circuit will perform correctly in each of the worst case situations. If this

is found to be the case then it is assumed that the circuit will perform as desired throughout the performance space. If the circuit does not perform correctly at one or more of the vertices then design improvements should be made.

The first step in the worst-case analysis process also provides the most challenging step, actually identifying the worst case vertices and the parameter values required to reach these [B43], although techniques have been proposed to combat this problem [B44;B45]. The simplest technique for the derivation of the location of the worst case vertices assumes that they correspond to the extreme values of circuit component tolerance ranges. Hence in order to assess the performance of the circuit at the worst case vertices we must simply analyse it at the extremes of all parameters as defined by their tolerance ranges. However it is entirely possible that the worst case performance of the circuit does not occur at these extreme parameter values. It may also be computationally expensive to analyse a circuit in this way, since the parameter space for a circuit with  $N$  parameters has  $2^N$  vertices. An alternative method to locating each vertex and carrying out  $2^N$  analyses is to determine, using sensitivity analysis, at which vertices the most extreme performance of the circuit will occur and then only simulate the circuit operation at these points. Sensitivity analysis involves altering all circuit parameters by a small amount a limited number of times and each time analysing the operation of the circuit whilst noting the effect upon set performance measures, these results may then be used to determine those circuit parameters which have the greatest effect upon circuit operation. A good discussion of this technique is given in [B46].

Other techniques have been proposed to locate the worst case points, and the majority view is that the easiest method takes the form proposed by [B43] for use in the design of integrated circuits. They proposed that in order to successfully establish the worst-case component parameters, we must look earlier in the life cycle and establish the worst case process parameters. This data can then be used to model the process and hence derive the worst-case component parameters, which can in turn be used with circuit simulators to obtain the performance points based upon a reduced number of components. The problem with this approach is that it is limited to IC level design where engineers have explicit control over all of the processes used to manufacture the circuit and are able to obtain detailed data and knowledge of circuit characteristics and is of little use to PCB level designers; since due to the discrete nature of the components used in PCB level designs, the process parameters relevant to one component will be of no relevance to another.

[B47] also propose that we should use process parameters to establish a worst case model, using statistical methods for the extraction of model parametric information. The proposed technique is intended to simplify the crucial first step in worst case analysis. [B47] first defined a suitable model of the MOSFET device under study, this was a modified form of a previously published model, the modifications where necessary to allow the best possible calculations of several device parameters to be made. The parameter sets where extracted from specially manufactured wafers ( $2\mu\text{m}$  CMOS technology), which had been deliberately manufactured in less than ideal conditions, using the newly specified device model. These parameter sets where then screened to remove extreme values (greater than  $\pm 4\sigma$ ), also any parameters found not to have Gaussian normal distributions where transformed so that they could be represented by such a distribution. The parameter sets where then analysed using principle component analysis (PCA) to reduce the number of correlated parameters to a smaller number of non-correlated 'principle components' which are generally easier to manipulate due to the smaller number of parameters in the set, in this case 81% of the variance of the model parameters could be accounted for by the first 7 principle components. The principle components where then processed again to allow the model parameters to be expressed as a linear relationship of independent components which had been normalised to have a mean of zero and a standard deviation of unity. The un-correlated process related components where then used to generate 128 worst-case 'corners' ( $2^7$ ) which where finally reduced to 2 worst case models. Worst case values for several device characteristics where then calculated and these where compared to measurements of the characteristics taken from the fabricated devices. The proposed methodology provided an accurate way in which worst case models can be constructed and verified, the models are also fairly simple due to the use of PCA in order to reduce the large number of initial parameters to a significant few which describe the majority of device operation. Although the initial model development is complex and requires a non-trivial understanding of device operation, once this has been carried out the model could be reused, possibly in a library of worst case device models.

Several problems exist in the proposed technique. Firstly, the need to fabricate a large number of devices in order to extract parametric data. Although this kind of operation may be possible when dealing with relatively simple and inexpensive silicon based systems, for more complex devices and non-silicon based systems the cost of doing so would be prohibitive. Secondly the technique relies on parameters having Gaussian distributions or at least the possibility of transforming the real distribution to such a

form. This, however, is not possible in all cases. Hence the technique will exclude some circuits and devices. Further to this the technique also makes some assumptions about the linearity of the response surface of the circuit under study.

Worst case analysis is of particular use to the IC designer where full control and knowledge of all the processes used in the manufacture of the circuit exist. Difficulties arise when attempting to apply similar techniques to PCB level designs due to both a lack of knowledge of the processes used in the construction of the components in use, and the lack of correlation between the circuit characteristics caused by the discrete nature of the components. Despite these shortcomings worst case analysis is still commonly applied to PCB level designs relying upon the possibly doubtful convergence between worst case component value vertices and performance vertices to allow the application of the technique. Further to this, due to the nature of component tolerance distributions worst case parameter sets will in general have a very low probability of occurrence. Hence the technique will not be cost effective, and can provide little more than binary information regarding the likely occurrence of parametric failures. Due to this lack of detailed post analysis information, it is difficult firstly to make cost of quality estimation based upon worst case analysis and secondly to estimate the likely effects of design modifications.

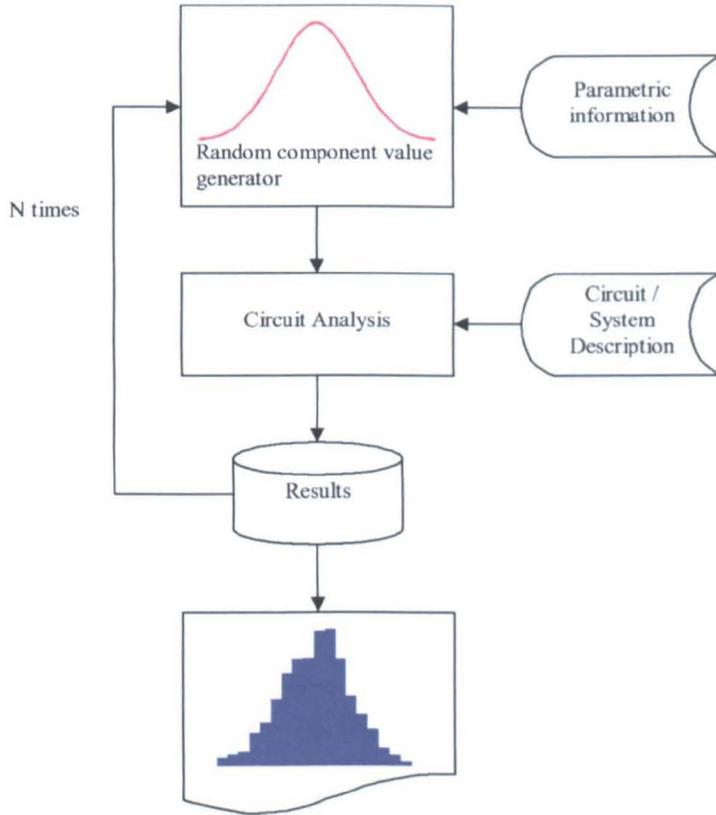
### **2.3.3 Non worst case tolerance analysis**

Non worst case tolerance analysis relies upon statistical sampling techniques to ensure that an accurate analysis of a circuit's operation is carried out, instead of attempting to capture the entire spectrum of performance as worst case analysis does. Non-worst case techniques attempt only to capture the most probable situations. Techniques range in complexity from the simple but popular techniques such as Monte Carlo analysis to more complex techniques such as Simplicial Approximation.

### **2.3.4 Monte Carlo**

Monte Carlo (MC) analysis is perhaps conceptually the simplest non worst case tolerance design technique. The procedure aims, using statistical simulation, to produce a 'picture' of a circuit's performance space using the minimum of computation. The technique (Figure 2-7) uses a pseudo random set of data from within the parameter space of the circuit in question to give good statistical coverage of the circuits most probable performance space. The quality of the coverage between the true circuit performance space and the MC approximation of the performance space is dependent

only upon the number of samples taken from the parameter space of the circuit and not the number of components.



**Figure 2-7 Monte Carlo Analysis Procedure**

Hence it is when simulating complex circuits that a significant advantage of MC analysis over other techniques comes to light. That is that for a given accuracy of performance space estimation the number of samples required by the technique is independent of the number of variables in the circuit, hence MC analysis may be used to model extremely complex circuits with only a small amount of the computing cost due to the simulation strategy applied. Further to this MC analysis provides us with a good model of the physical world as the model parameters used for any single sample can be seen to be a good analogue to the physical world, another important advantage of the MC method is that it is applicable to any circuit, and is parameter distribution independent making it a most flexible technique.

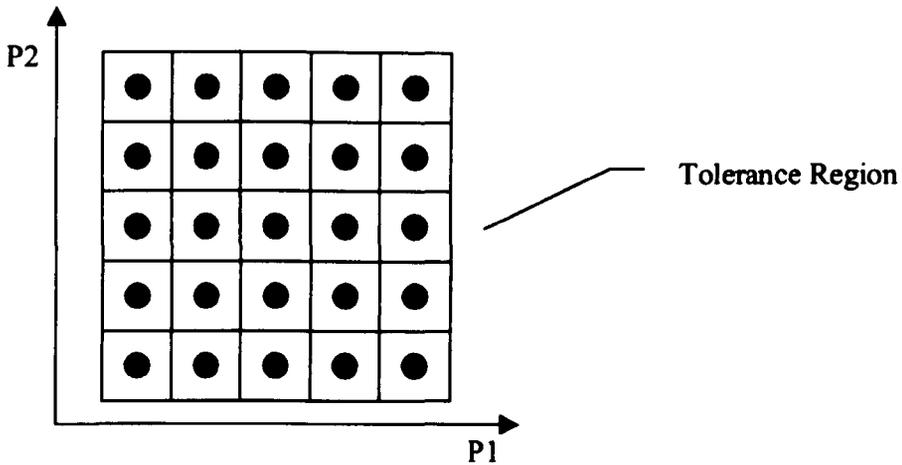
### **2.3.5 Control Variates**

Due to the dependency of MC analysis upon the number of samples taken from the performance space of a circuit (i.e. the greater the number of sample the better the coverage) MC analysis may be computationally expensive. Even with fast modern computers of the type often available to electronics designers the computation of a large

number of complex circuit simulations may take a long time, however despite this the computational cost is still often less than for worst case based techniques and the statistical coverage provided is normally much greater for lower sample sizes. Further to this, techniques such as the Control Variates method (CV) [B48;B43;B49] do exist to help reduce the computational costs of the analysis. The CV method works by using a second 'shadow' model of the circuit, which accurately models the performance and yet is a simple and therefore faster system to model, in parallel with the main 'realistic' model. The first step is to carry out a small control run simulating both models using the same random parameters, the results from both models are then compared and the differences noted. Next a large run is carried out using only the shadow circuit and the results transformed, using the data from the control run, to represent the real circuit. As the shadow circuit is much simpler than the real circuit the computational cost will have been significantly less. The main problem with this technique comes from the development of the shadow model as it may be very difficult to accurately model complex circuits using a simplistic system. Further to this the CV comparison may not be capable of detecting non-linear circuit behaviours such as those experienced during transistor saturation. Despite this, CV or similar functional modelling systems are used especially during the concept development stages of design. The developers of the technique state that with experience surprisingly accurate results may be obtained using this technique. However if the effort required to gain this experience would be usefully expended is uncertain, as from a certain point, of view the CV technique is a strange technique to apply to a MC simulation. As although the technique does reduce the number of parameters included in a model it will not necessarily reduce the computational cost sufficiently to justify the associated loss of quality in the analysis.

### **2.3.6 Regionalization**

Regionalization is the practice of splitting the multi-dimensional parameter space of a circuit into a number of equally sized 'regions' [B50] and then performing a circuit analysis at the centre of each region, the result of this analysis is assumed to represent the entire unit [B50].

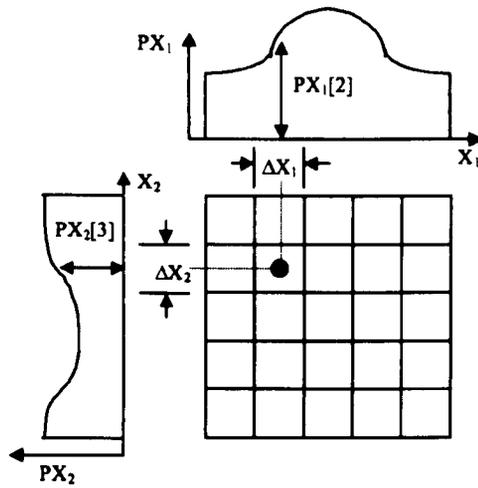


**Figure 2-8 Circuit Performance Regionalization [B46]**

The main disadvantage presented by this technique is the rate of increase in cost of analysis with the number of component parameters. The number of analyses required can be represented by  $R^P$  where  $R$  is the number of regions each parameter will be divided into and  $P$  is the number of parameters. For even small numbers say, 5 regions per parameter and only 10 parameters, large numbers of simulations would be required, 9,765,625 in this case.

In order to combat this problem [B50] proposed an algorithm to identify which regions should be examined. It was suggested that weights could be assigned to regions by generating points in the parameter space based upon the probabilities of component values; and then counting the number of points in each region to determine the appropriate weight. Only the regions above a particular weight would then be simulated thus reducing the computational cost.

[B51] proposes a new methods for the assignment of the weights, instead of generating points in the parameter space by a random process based upon the probability of parameter values and 'counting' the number of points in a region to assign a weight, it is proposed that the weights are calculated directly from the component probability density functions without the use of a random distribution generation, this is a more robust technique although possibly more complex to implement.



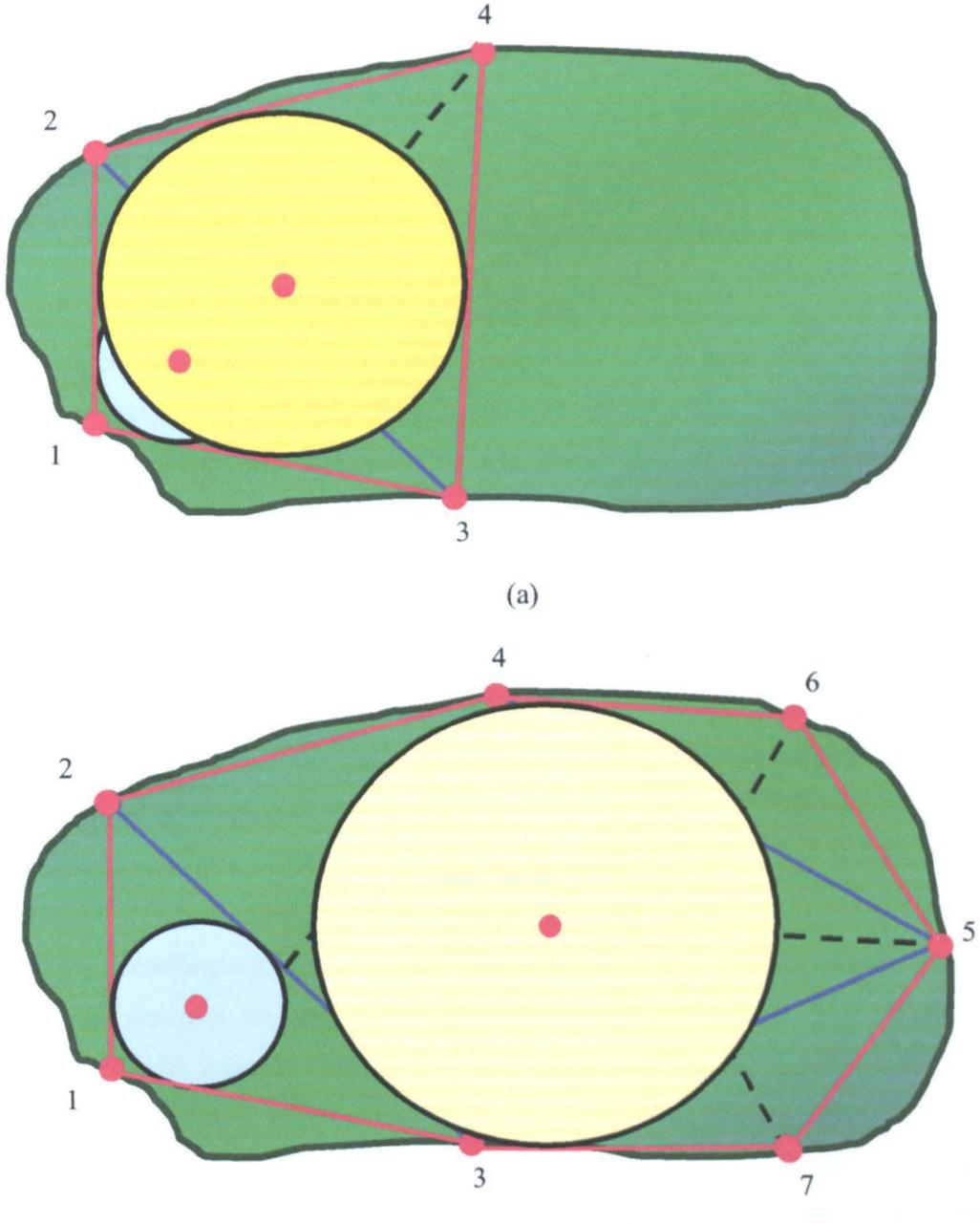
**Figure 2-9 Idealized Statistical Model [B51]**

If the two PDF's shown in Figure 2-8 are independent then the weight of the point  $(X_1[2], X_2[3])$  may be approximated by the product  $PX_1[2].\Delta X_1 * PX_2[3]. \Delta X_2$ . This weight is then used in the same manner as the earlier technique to streamline the simulation process. The paper presents examples of the application of this method showing that the results obtained are comparable to those of Monte Carlo analysis. However as the technique will only produce good results in a specific case (circuit performance is linear) this prevents it being applied to circuits in general, it is never the less a useful technique.

### **2.3.7 Simplicial Approximation**

Simplicial approximation is essentially a method for producing a polyhedral approximation to the parameter space of a given circuit [B52]. The technique proposed in [B52] involves approximating the boundary of the acceptable region  $R_A$  by a polyhedron. First, any  $m$  points must be located on the boundary of  $R_A$ . A convex hull is then constructed from these points. The design centre is then located by finding the largest hyper sphere; which can be fitted into the polyhedron, and locating its centre. The next step is to refine the approximation by finding the largest face of the polyhedron (as this is likely to be the worst estimate of the boundary) and then splitting it into multiple segments to create a more accurate representation. Figure 2-10 illustrates this technique. Initially the polyhedron is the triangle 123. The longest face 23 is bisected by a normal line along which a search is carried out to locate the next point on the boundary of  $R_A$ , as shown in Figure 2-10a. The polyhedron 1234 is then expanded in the same manner to 1234567.

The technique can be applied to any circuit linear or non-linear, and is considered to be more computationally efficient than the regionalization method, however, as with regionalization as the number of parameters in a given circuit rises the number of simulations required to produce the simplex also rises.



**Figure 2-10 Application of Simplicial Approximation to find the Parameter Space and Design Centre, (a) Shows the Initial Polyhedron (1,2,3) and the Line Breaking the Largest Face to give (4) and (b) Shows the Polyhedron after 4 Iterations [B52].**

This dimensionality problem has been addressed, in [B53]. A technique is proposed which can usually be used to reduce the dimensionality of simplex models of IC

designs. Rather than taking into account circuit parameters [B53] proposes that manufacturing parameters are used to create the simplex, hence vastly reducing the dimensionality problem. However, it is at once obvious that this method ensures the dimension reduction technique is only applicable to integrated circuits and is of no use in the more general field of PCB level circuit design.

Simplicial approximation has two further major drawbacks firstly that it requires the parameter space to be convex and simply connected and secondly that it cannot cope with black holes in the parameter space, which may occur in practical circuits, the Sallen Key filter for example [B46].

### **2.3.8 Design of Experiments and Taguchi**

Design of Experiments (DOE) and Taguchi are highly structured techniques which employ established statistical techniques, particularly analysis of variance (ANOVA) and linear regression, to explore the parameter space of a product or process often with the aim of producing a centred or robust design [B54]. DOE uses systematic analysis techniques which are applied to a process in order to obtain the maximum amount of information about that process with regard to the factors affecting it with the minimum number of experimental observations [B10]. This kind of technique is especially popular in industry with regard to the analysis of manufacturing processes as it may be used in order to reduce the cost of carrying out an experiment [B55] whilst maintaining a good level of experimental coverage.

The basic principle of DOE is the use of an experimental procedure based around a factorial design; this is essentially a scheme for the manipulation of a number of the factors controlling a process. The advantage of such an experimental design is two fold, firstly it provides an efficient vehicle for the exploration of the parameter space associated with a product especially when compared to simpler “one factor at a time strategies”. Secondly as multiple factors are manipulated at any one time it allows the effect factor interactions to be observed. This is a key strength of DOE style experimentation and it is made more attractive through the use of statistically designed experimental schemes which allow the effects of a single factor, or a specific combination of factors upon a process, to be separated from the effects of other factors. Several different kinds of factorial design exist with differing levels of complexity, coverage and associated experimental cost dependant upon the number of levels at which the effects of each factor is assessed, the number of factors and the level of factor confounding that may be accepted. The most popular form of the factorial experiment is

the two level fractional factorial design, such designs increase the efficiency and hence reduce the cost of experimentation by making two main assumptions, firstly that factor effects are linear and secondly that high order factor interactions have only a minimal effects and hence that interactions above a level decided upon by the experimenter may be discarded. Immediately obvious from this is that considerable care and attention must be paid when applying factorial designs in order to avoid violating these assumptions and potentially carrying out a worthless experiment. Detailed discussion of the development of such designs may be found in the literature e.g. [B56]. A general idea of an experimental design may be gained from Figure 2-11, the figure shows a four factor resolution IV design. This reference to experimental resolution is an expression of the level of factor interaction confounding associated with a design. In the case of a resolution IV design it means that no main effects or two way interactions are confounded with any other interactions whilst interactions of an order greater than two are all confounded and hence the influence they exert over a process may not be determined.

	<b>Factor</b>			
<b>Order</b>	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
<i>1</i>	-1	-1	-1	-1
<i>2</i>	+1	-1	-1	+1
<i>3</i>	-1	+1	-1	+1
<i>4</i>	+1	+1	-1	-1
<i>5</i>	-1	-1	+1	+1
<i>6</i>	+1	-1	+1	-1
<i>7</i>	-1	+1	+1	-1
<i>8</i>	+1	+1	+1	+1

**Figure 2-11 A Four Factor Resolution IV Fractional Factorial Experimental Design (One Half Fraction)**

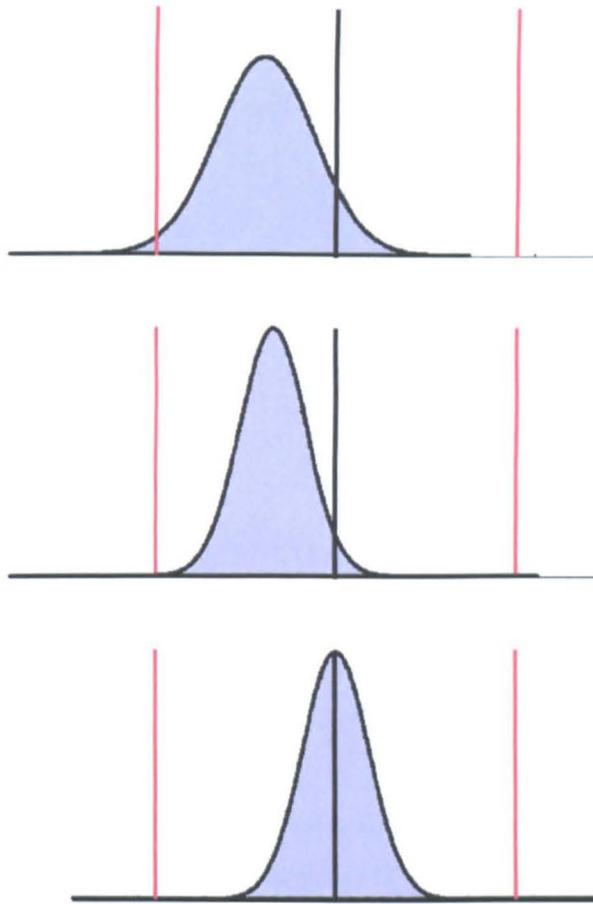
Figure 2-11 shows a standard representation of a fractional factorial design, each of the factor columns contains a series of +/-1's which represent the two different levels associated with an individual factor. These two levels may be any appropriate values of a process factor and are commonly set to the design limits of a particular parameter, however as previously noted care must be taken to ensure that the process under study is linear over this range. Also it should be recognised that linearity cannot be assumed valid results may be gained from setting them around a particular point of interest. Where linearity is not certain statistical tools do exist that allow this assumption to

tested as part of the normal post experimental analysis procedure, and it is also possible to include extra experiments which place additional 'centre' points into the experiment [B55] to assist in the detection of curvature.

Once such an experiment has been carried out the results may be analysed with common statistical procedures such as ANOVA [B57;B56;B55] which allow the determination of the extent of influence a particular parameter has over a process. Such information maybe of use in order to improve a process by 'tuning' or controlling the most influential process parameters. Engineers applying the DMAIC framework [B58;B10] frequently apply DOE within the Analysis stage to determine the significant parametric influences upon and process or product and the results are then passed on to the Improve stage of the framework where the results are acted upon. Effectively DOE is a general form of tolerance analysis, exploring the performance space of a process, commonly this is the worst case performance space but this is not necessarily true; it allows the impact of process parameters to be assessed.

The Taguchi techniques also known as the robust design methodology is a collection of ideas and analysis methodologies developed by Dr. Genichi Taguchi. The basic premise of the methodology is that through consideration of the desired system performance together with noise factors and an appreciation of the cost of failure product quality levels may be increased [B59].

It is widely accepted and understood that once of the key factors involved in improving the quality of a product is to reduce the effect of parametric variation upon the desired product performance, hence producing a robust design. The Taguchi approach to improving the level of robustness associated with a product is based around careful modification of the nominal parameter values associated with a product to decrease its sensitivity to parametric variation supplemented with a centring procedure which shifts a process mean to be co-incident with the nominal process output. This two stage optimization procedure is illustrated in Figure 2-12.



**Figure 2-12 The Two Step Taguchi Process**

The Taguchi approach employs five main tools to achieve this goal, these are described below.

The parameter diagram (P-Diagram) [B10], is used to classify the parameters (variables) associated with the product (system) into one of four groups:

- Control Factor
- Noise Factor
- Input Signal Factor
- Output Signal Factor (response)

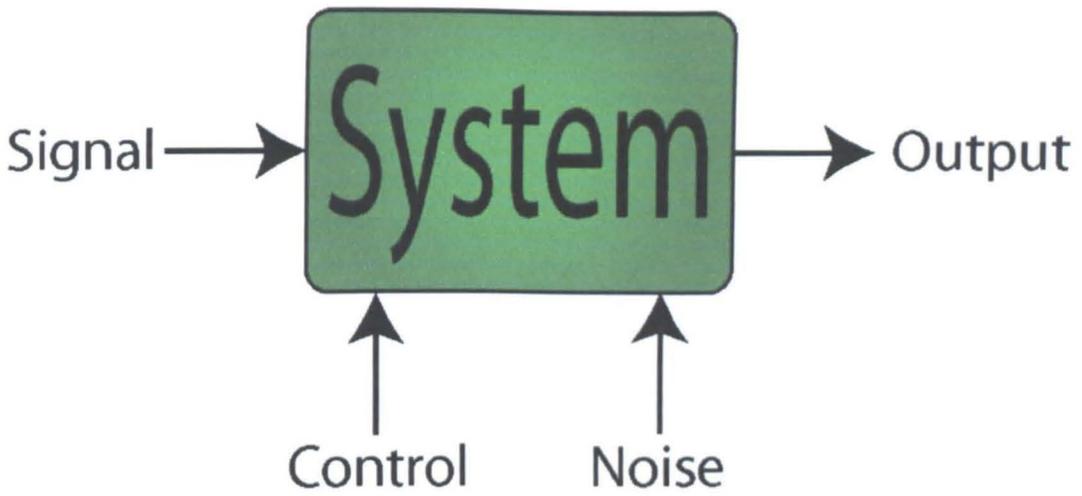


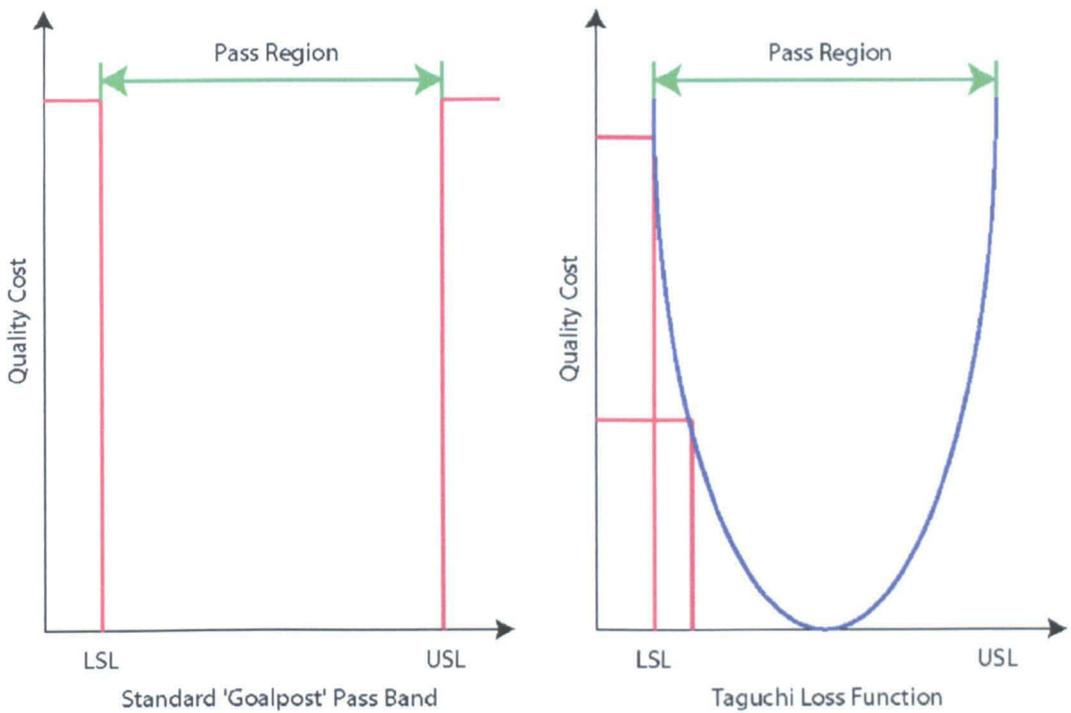
Figure 2-13 A P-Diagram

Once the P-Diagram has been completed the systems ideal function may be derived this should be of the form given below:

$$Output = Signal * Control$$

However as we know the system is not ideal and contains noise, this allows us to use the standard Signal to Noise ratio calculation to define the robustness of the system. Hence the design should be optimized such that the signal to noise ratio is maximised. The Taguchi techniques use an analysis technique based upon standard DOE procedures to drive the systems analysis, testing each of the factors at a number of different levels. This ensures that the parameter space occupied by the signal, control and noise factors is well covered and enables us to determine the effect of the control parameters upon the Signal to Noise ratio. Once this relationship has been derived using factor effects analysis similar to ANOVA we may choose the parameter set which maximises the Signal to Noise ratio. The interested reader is directed to the following texts for further information, [B8;B60;B61].

Once a design has been made robust the second stage of the Taguchi quality engineering technique is to optimise a design to achieve its target system response. The aim of this stage is embodied by the Taguchi 'Quality Loss Function' [B54] which provides expression to a customers desire to have a product which is consistent on a part to part basis and the manufacturers desire to minimise the cost of production. This idea of a quality loss function which implies increasing quality costs as the inherent result of moving away from the target value this is opposed to the standard view that any product falling within a customers tolerance pass band incurs no cost and one falling outside incurs maximum cost, these two alternative view of quality cost functions are illustrated below in Figure 2-14.



**Figure 2-14 Standard Tolerance Band and the Taguchi Quadratic Quality Loss Function**

The purpose of the quality loss function is to illustrate the effect of output variation as defined by the tolerance bands associated with the control parameters. Hence we may use the quality loss function to evaluate the variability in the output signal for a given set of control parameter tolerances against a different set of tolerances. This kind of evaluation allows the cost trade off between differently tolerated components and the resulting system response to be assessed in monetary terms.

The Taguchi analysis technique is successful when used to optimise relatively straightforward systems and processes however it is less effective when dealing with complex systems with a large dependence upon second order or higher factor interactions commonly found within electronic systems. This is due to the disregard for these interactions caused by the use of a Resolution III Array which is not capable of supplying sufficient detail of factor interactions. One potential solution to this problem may be to partition complex systems and then analyse each segment independently. However, this would introduce additional work into an already laborious and potentially complex analysis process along side introducing the potential for misleading or contradictory results.

### 2.3.9 Summary of Tolerance Analysis

This section has described only a few of the numerous tolerance analysis techniques available to an engineer. Only a selection of these techniques are commonly

implemented within CAD packages. Those most commonly found are Monte Carlo analysis and Worst Case analysis, the more esoteric techniques, Simplicial approximation for example, are not normally found in commercial packages but only as additions by specialist teams. However, some tools do include variations upon the basic techniques, for example the SABER circuit analysis tool includes Worst Case Monte Carlo analysis, a technique which attempts to rectify some of the shortcomings of the basic Worst Case analysis technique by applying Monte Carlo analysis around each of the selected Worst Case positions. This technique has the advantage of extending the capabilities of both Worst Case and Monte Carlo analysis by effectively widening the coverage of the simulation, however it also brings together the worst features of both techniques as it tends to be very computationally expensive.

## **2.4 Testability Analysis**

Testability analysis is a key component of any DFQ program. The aim of any testability analysis program is firstly to estimate fault coverage and the likely occurrence of false passes and fails and secondly to improve fault coverage and reduce likely test errors as required. Testability analysis is often implemented as a component of a Design for Test (DFT) strategy [B62] and its contribution to product quality is well recognised [B63]. However its greatest use is in integrated circuit manufacture rather than PCB manufacture, despite the potentially larger fault spectrum, and as a result of this the vast majority of the literature reflects this trend [B63]. A significant aspect of any testability analysis program is the use of test metrics, such metrics aim to give a clear indication of a circuits testability [B64;B65;B66;B67;B68;B69]. Testability analysis requires the use of sophisticated statistical modelling techniques which both explore the parameter space of a product and its response to the potential defect spectrum [B70;B71;B72;B68;B73;B62;B74]. When implementing such a statistical analysis a critical aspect is the realism of the 'fault dictionary' [B73] employed. This is a database of circuit models which may be 'injected' into a perfect circuit in order to simulate the effects of a defect. In summary it should be noted that there is a considerable amount of literature available upon the subject of testability analysis and the vast majority exceeds the scope of this thesis. However knowledge of the subject is required and an ability to use testability analysis software [B75;B76] does fall within the scope of the thesis. The need for testability analysis is evident due to the relationship between the defect levels experienced by a customer and the capability of a testing procedure.

## **2.5 Manufacturability Analysis**

Manufacturability analysis under the guise of Design for Manufacture (DFM) is well established in mechanical engineering fields where Boothroyd and Dewhurst are leading proponents [B77]. They also propose models for use in PCB manufacture but techniques are in general less established in the electronics field. DFM models attempt to quantify the 'manufacturability' of a design and popular models such as that used by [B77] do this relative to factors such as the number of parts and assembly complexity, hence it follows that fewer parts and less complex assembly sequences will produce more manufacturable products. In [B78] a DFM technique using a Knowledge Based System (KBS) is presented, the technique discussed is aimed at improving the quality levels achieved by a particular wave soldering method, but it would be possible to adapt the technique for use in other processes. The technique is however limited in two ways. Firstly by its reliance on a KBS, which the authors acknowledge will be difficult to maintain and secondly by its lack of economic feed back. The lack of economic information is a serious flaw and could lead to significant product cost increases due to design modifications made on the basis of information provided by the technique. The method for PCB design assessment presented in [B77] addresses this lack of economic feedback by assessing a design in terms of the total operational cost which includes such factors as the cost of auto insertion, rework and replacement parts. A similar system is presented in [B79] which notes that economic information is important as 'product design and redesign are driven by cost reduction'. [B79] presents a method for assessing the total manufacturing cost of a product in a quantifiable way, hence allowing a designer to find the impact of design modifications in monetary terms. The system described by [B79] was implemented in software for use by engineers working for Motorola. [B80] also presents a methodology for a cost based PCB design evaluation, this time aimed at surface mount components. Once again the technique has been implemented in software and an example analysis using the software is presented. A detailed discussion of the development of manufacturability analysis software is given in [B81]. The paper presents an object orientated system for design assessment and includes example code representing manufacturability rules. It also discusses the important issue of manufacturing yield and the software is shown to be able to estimate manufacturing yield for a given design. All of the discussed techniques have a common theme in that they rely upon the development of a rule base for the analysis of designs. Such rules are also used in commercial DFM software such as Valor Trilogy 5000 which, given the schematic data for a PCB layout, allow the adherence to design rules at

several different levels to be analysed and highlights board areas which may cause problems during manufacture and assembly.

### 3 Conformability Analysis

#### 3.1 Introduction

This chapter provides an introduction to the Conformability Analysis (CA) methodology developed by Batchelor and Swift. CA is a mechanical engineering technique which was developed to address specific Design for Quality (DFQ) issues relating to the effects of process variability upon product quality. CA provides a structure and tool set for the analysis of process capability associated with component manufacture and product assembly. Using an impact assessment and cost mapping procedure CA relates the predicted level of process capability to an estimated failure cost (cost of quality).

The technique is intended for use by design and process engineers to allow an early estimate of the cost of quality implied by a specific design and process route to be made, and hence minimise the quality costs associated with a design. CA uses process variability analysis, carried out through the application of a series of simple maps and charts to a design. This is combined with Failure Mode and Effects Analysis (FMEA) [B82;B83] and a quality cost mapping system to derive an estimate of the quality costs Figure 3-1 associated with the particular design.

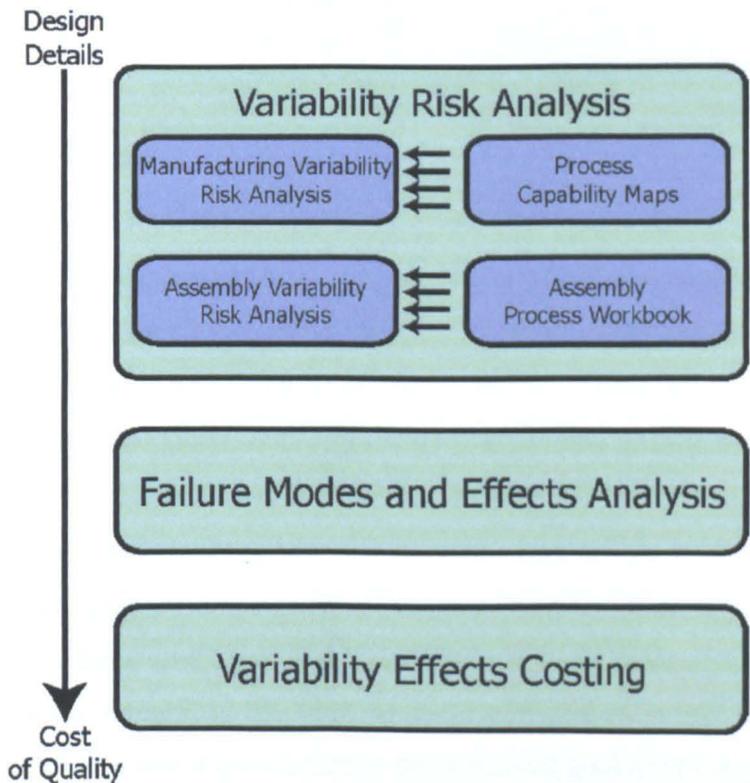


Figure 3-1 The Components of Conformability Analysis

### 3.2 Design for quality

The basic issues of Design for Quality (DFQ) are addressed by several different sources, and a good general review is given in [B84]. From this review a general DFQ model is developed which may be used as part of a system to determine those critical to quality aspects of a design which will impact upon the cost of quality. [B85] advances the previously proposed model and presents the conformability analysis methodology which is a DFQ technique for predicting potential process capability problems and the quality costs associated with these variability dependent effects.

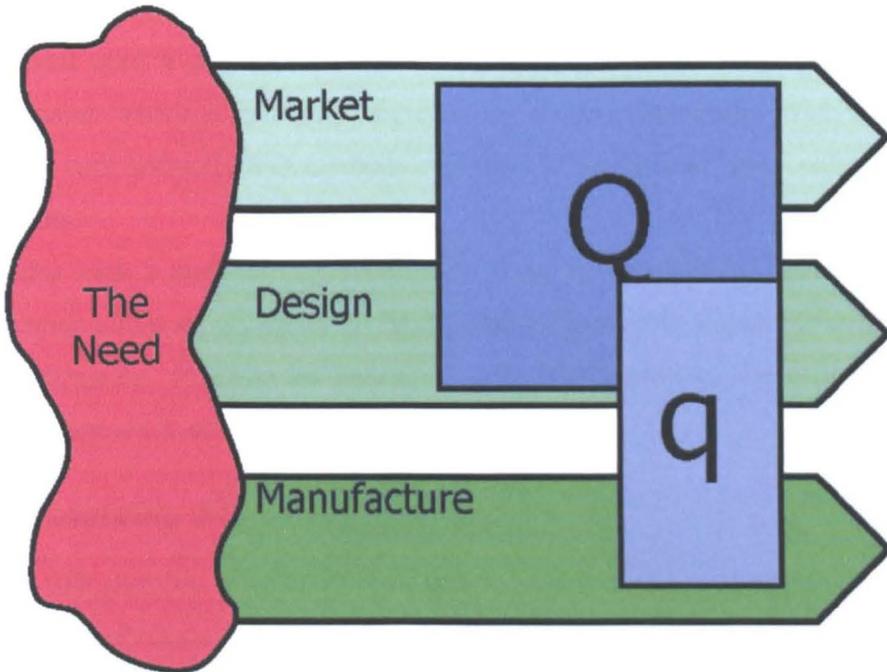


Figure 3-2 Q and q in Integrated Product Development [B84]

To enable a better understanding of the aims of DFQ it is helpful to consider Figure 3-2, which effectively provides a graphical description of the DFQ model presented in [B84]. The diagram shows two identifiable areas of quality. These are:

- 'Q' (big q) is the customers perceived level of product quality, this relates to all of the aspects of a product which affect a customer.
- 'q' (little q) which is the quality of the engineering efforts made in achieving a better level of Q.

This diagram provides a useful tool and framework for the analysis of the DFQ model. We can at once see through to the heart of the model and its corner stone principle which is that to achieve any improvement in the perceived quality of the product, Q, we must improve the quality of the underlying engineering effort, q. It may be helpful to

consider that Taguchi analysis which provides us with a 'Voice of the Customer' would effectively assess Q, that is the quality level as seen by the end user. This analysis is reinforced by [B85] where we are told that *'The maintenance of Q relies upon the ability of a business to understand and control the variability which might be associated with the process of product realisation'*. As discussed above, this statement captures an essential element of DFQ, in that if we can control process variability we can maintain Q, given the understanding that the design is suitable for manufacture by the chosen manufacturing route and the processes which comprise that route.

However the matter is somewhat more complex than simply controlling process variations, as each Q element (build quality, performance, life etc) of a given design is not dependent upon a single factor but has a number of contributory q elements. It is this relationship which is generally neglected by engineering teams, who without the support of a well defined DFQ methodology tend to concentrate upon only a few key design factors.

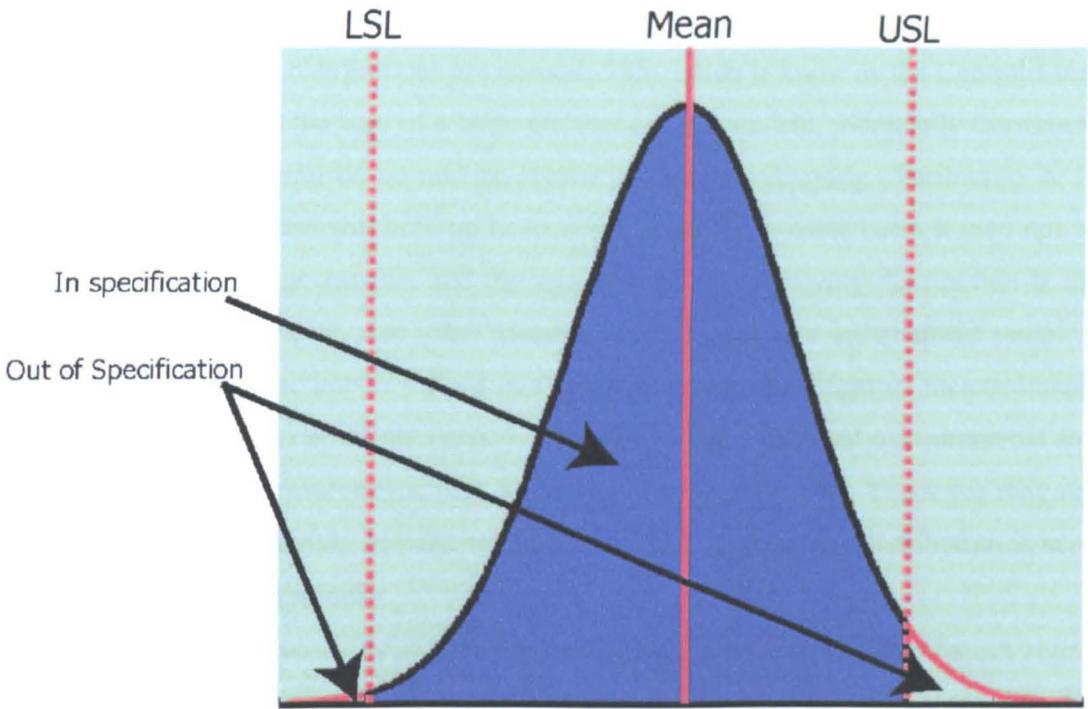
CA provides such a methodology along with a suitable toolset for the assessment of these q elements in a supply chain focused manner. Hence this allows the overall effect of design decisions on Q to be measured, and in response to these measurements appropriate corrective actions may be made as required.

### **3.3 Variability Risk Analysis**

Variability risk analysis is a key component of the CA tool set. It allows engineers to analyse a design to discover when a manufacturing or assembly process is being pushed to the limits of its capability, and hence indicates the need to either implement design changes or where appropriate monitor and control the process using Statistical Process Control (SPC).

### **3.4 Process Variability**

Process variability may be derived from a number of different sources ranging from badly optimised manufacturing processes to poor design features, particularly those which do not take sufficient account of the capabilities of the manufacturing process.



**Figure 3-3 A Typical Process Distribution with Example Specification Limits**

Process capability indices (PCI's) allow process variability to be assessed, which in turn allows engineering judgement to be applied to the performance of a process.

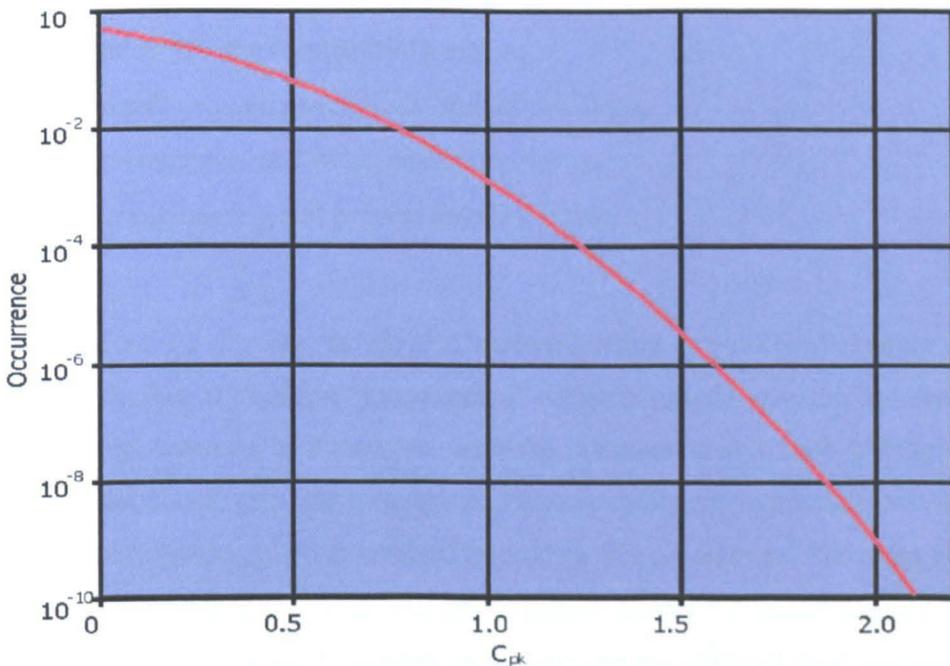
The most popular PCI due to its versatility and ability to cope with none centralised distributions is the  $C_{pk}$  index, it provides us with an easily applied technique which allows us to assess the ability of a process to produce products that meet the given specification. If it is assumed that the variation in a characteristic is normally distributed with mean,  $\mu$ , and standard deviation,  $\sigma$ , and that the acceptable range of performance is from the lower specification limit ( $LSL$ ) to the upper specification limit ( $USL$ ) then  $C_{pk}$  may be written as in equation 6.

$$C_{pk} = \min\left(\frac{|\mu - LSL|}{3\sigma}, \frac{|USL - \mu|}{3\sigma}\right) \quad (6)$$

Thus the greater the distance between the mean and the specification limits, relative to the standard deviation, the higher value  $C_{pk}$  and the less likely the process will be to produce events out side the specification limits. The reliance on the standard deviation,  $\sigma$ , of the process and hence the assumption of a normal or at worst close to normal process distribution demonstrates a possible weakness of the CA methodology in that there is no provision for non-normal process distributions.

This lack of provision is due to a general reliance upon the belief that given large enough samples most distributions are normal. This notion is known as the Central Limit Theorem. It states that the sum of a large number of independent, identically distributed variables will in general be normal no matter what the underlying distribution is. In many cases this theorem will hold up to scrutiny, however in some cases it may not be possible to take a large sample, and the less normal an underlying distribution is the larger the sample must be, also some measurements do not give independent samples; consider measuring the impurity level in a semiconductor, five separate measurements would not yield five independent variables. Further to this individual measurements and not the average of measurements may be in or out of specification, hence we may not generate accurate capability indices unless the underlying statistical distribution is used for the calculation of the index.

Despite this process capability indices are a valuable tool within a design for six sigma methodology and they provide a simple way to estimate process failure rates and hence to make quality cost estimates for a given process and design. It is at once obvious that quality costs must be kept to a minimum and as such Design for Six Sigma (DFSS) dictates a minimum acceptable value for  $C_{pk}$  of 1.5, corresponding to a failure rate of 3ppm (Figure 3-4), while  $1.33 < C_{pk} < 1.5$  is often taken as the range for which Statistical Process Control (SPC) is required.



**Figure 3-4 Relationship Between the  $C_{pk}$  Capability Index and Occurrence (Normally Distributed Performance Variation)**

### 3.5 Manufacturing Risk

CA does not give a single definition of risk as this would be far too inflexible to be applied to a wide range of designs, instead CA introduces the idea that risk is in fact a composite term which may be estimated by constructing a relationship between a number of factors each representing a particular process characteristic and contributing to the whole [B86]. For example when drilling a hole we can easily think of a number of factors that would contribute to the quality of the hole:

- Material thickness
- Type of material
- Type of drill
- Speed of drill

Hence we see that component manufacturing risk ( $q_m$ ) which gives an index to the likelihood success in the manufacturing of a component, can be expressed by the following equation:

$$q_m = t_p * m_p * g_p * s_p * k_p$$

Figure 3-5 Component manufacturing variability risk analysis equation [B87]

Where the terms are:

- Process precision and tolerance capability risk,  $t_p$
- Material to process compatibility risk,  $m_p$
- Component geometry to process limitation risk,  $g_p$
- Surface roughness and detail capability risk,  $s_p$
- Surface engineering and process suitability risk,  $k_p$

Each element of  $q_m$  ( $t_p$ ,  $m_p$ ,  $g_p$  etc.) is assessed using a workbook system [B86] containing a number of capability maps each of which is process specific and describes the relationship between a dimension and the risk associated with the tolerance requirement associated with that dimension. This capability map approach provides an easy to understand and implement method of process risk assessment. The maps (Figure 3-6) show graduated levels of risk towards a perfect score of 1 which would indicate that a particular process is easily capable of performing the required function, scores of value greater than one indicate less satisfactory results. Hence a risk index of 1 would indicate that the engineer need not worry unduly about manufacturing failure, but as the

index increases in value this indicates that manufacturing failure is increasingly likely and hence steps must be taken in order to decrease this risk.

This risk assessment system has a number of advantages, the most prominent of which is possibly its ease of use, the workbook system is easy to follow even for an inexperienced user and has even been converted into a computer based system which allows the workbooks to be quickly searched for the correct chart. Further to this the system is flexible and easily expandable allowing greatly differing designs to be catered for and also the introduction of new capability charts to cover new techniques as and when is necessary. However the system does have limitations, firstly in that it relies upon the presence of suitable capability charts to assess a given design and secondly that complex designs could potentially be laborious to assess and assign risk factors to.

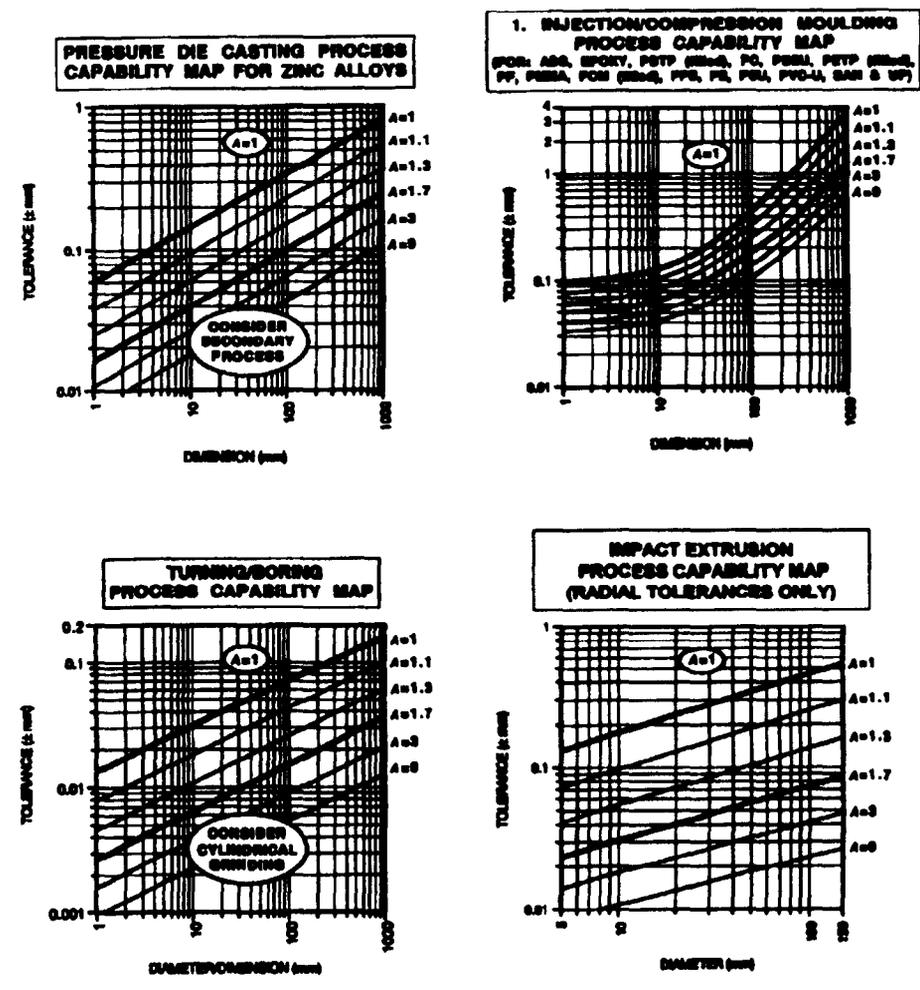


Figure 3-6 Sample Capability Maps [B87]

Returning to the capability maps seen in Figure 3-6 we can see that the contours represent the limits between design characteristics where different levels of risk are present, hence in the upper areas of the maps above the A=1 contour a designer would

have little to worry about but as tolerances and dimensions change moving a design into other regions the A (the risk factor) increases. A=1.7 is highlighted as representing the boundary between an acceptable design and a design which will require SPC or a design change to ensure a quality process is maintained. In [B87] it is noted that there is a relationship between  $q_m$  and  $C_{pk}$  hence the abstract measure  $q_m$  may be easily converted into a form commonly understood by the engineer or engineering team.

$$C_{pk} \approx \frac{4}{q_m^2}$$

**Figure 3-7 Relationship Between Abstract  $q_m$  and  $C_{pk}$  [B87]**

### **3.6 Assembly Risk**

Component assembly risk ( $q_a$ ) gives an index to the likelihood of assembly success for the components under study.

$$q_a = h_p * f_p * a_p$$

- Handling characteristics,  $h_p$
- Fitting characteristics,  $f_p$
- Additional Assembly considerations,  $a_p$

**Figure 3-8 Component Assembly Risk Analysis Equation [B87]**

The component assembly risk is assessed using charts created using expert knowledge to give values to the risk elements [B86], once again an index of 1 would imply a suitably capable design & assembly process combination whilst any greater number means that there is a significant risk of assembly failure occurring. As with the assessment of manufacturing risk assembly risk analysis requires the presence of suitable charts within the workbooks and although a large number of charts are included covering a wide range of situations and techniques, new assembly techniques may pose problems due to a lack of coverage also again as with manufacturing risk analysis complex systems may be difficult to assess and assign a risk factor to.

### **3.7 Workbook System**

As discussed in sections 3.5 & 3.6 designs may be assessed and associated manufacturing and assembly risks calculated using workbook charts such as those seen in Figure 3-9. Although there are disadvantages associated with this approach related to the speed of updating and introduction of new processes the chart system is easy to understand and quick to use allowing engineers to make fast assessments of the risks inherent in the

proposed design. The use of this workbook based system makes the CA process accessible to all engineers with little or no training in the technique, this is a significant advantage for the technique as the easier it is to use the more likely it is to be widely employed.

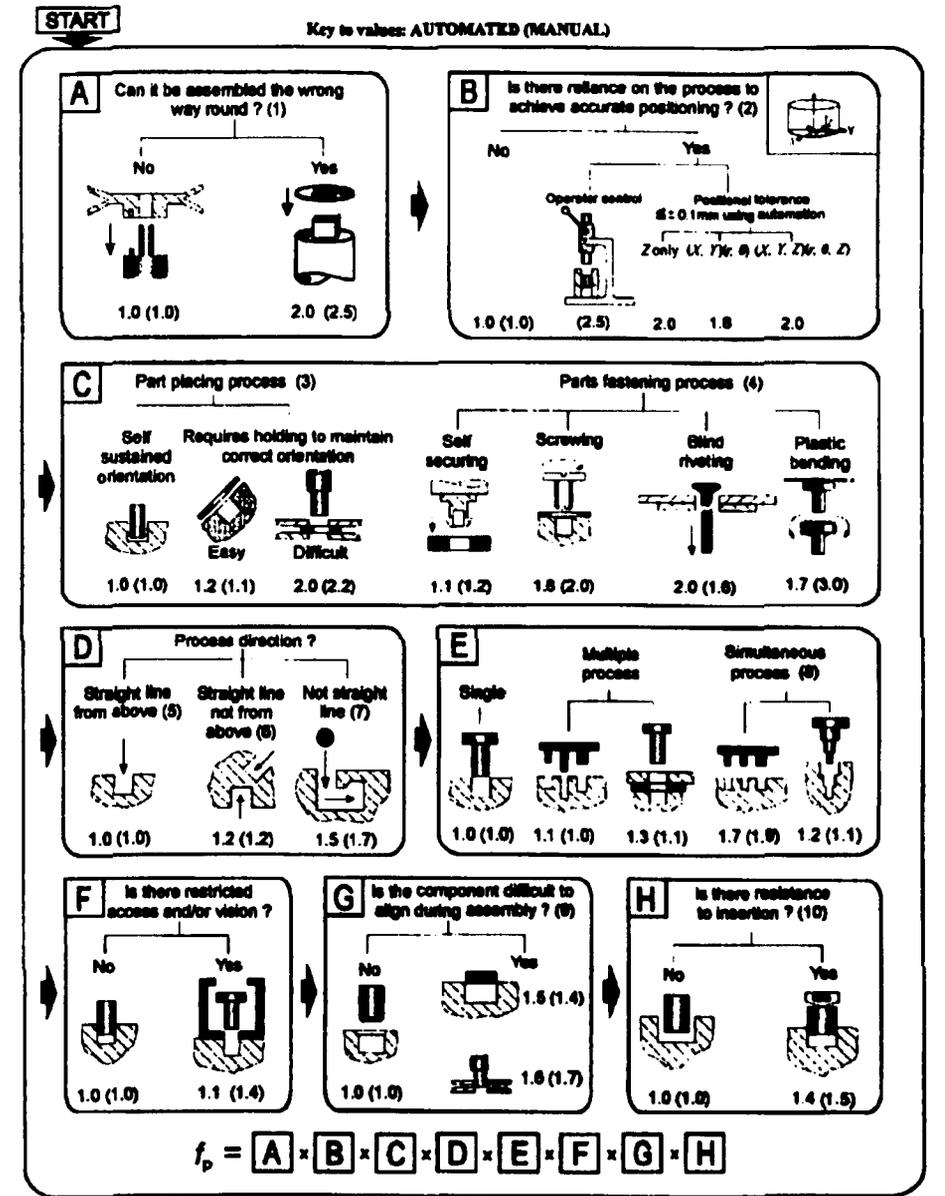


Figure 3-9 Fitting Process Risk Chart [B87]

### 3.8 The Effects of Process Variability

Failure Mode and effects Analysis (FMEA) provides a ready method for the assessment of manufacturing or assembly failure severity. Using the Severity (S) scale shown in Figure 3-10 we may easily equate the effect of a product failure to its effect on a user/customer and hence its impact on Q.

The CA tool estimates the effects of process variability leading to non-conformance by linking failure occurrence with its effect on the user, this is done using the ‘conformability map’, as shown in Figure 3-11, [B86] which plots together process capability (Y-axis) with FMEA severity (X-axis) and links the two by constructing lines of equal quality cost, known as ‘iso-costs’ in CA terminology.

<b>Severity (S)</b>		
<b>Rating</b>		<b>Effect</b>
<b>Non-Safety Critical</b>	1	Non or minimal effect on user / customer
	2	Minor annoyance
	3	Annoyance but no loss of major function
	4	Possible warranty return
	5	Definite warranty return
<b>Safety Critical</b>	6	Failure leading to violation of statutory requirement
	7	Failure leading to injury or a more safety critical related problem with secondary backup
	8	Safety problem – degradation of function with possible severe injury
	9	Complete failure with probable severe injury and/or loss of life
	10	Catastrophic failure with high probability of loss of life

**Figure 3-10 FMEA Severity Scale [B88]**

Costs in the sub safety critical region (Severity < 5) are modelled by a horizontal line which at the boundary of the area of acceptable design is located at  $C_{pk}=1.33$ . The location of this horizontal section of graph implies that the minimum capability for any process used in the manufacture and assembly of a product should be at least 1.33 the widely accepted limit of SPC. The area covered by the horizontal section of the graph represents items such as customer returns and product replacement, above this safety

critical threshold iso-costs are modelled as a diagonal lines representing increasing cost as failure severity increases.

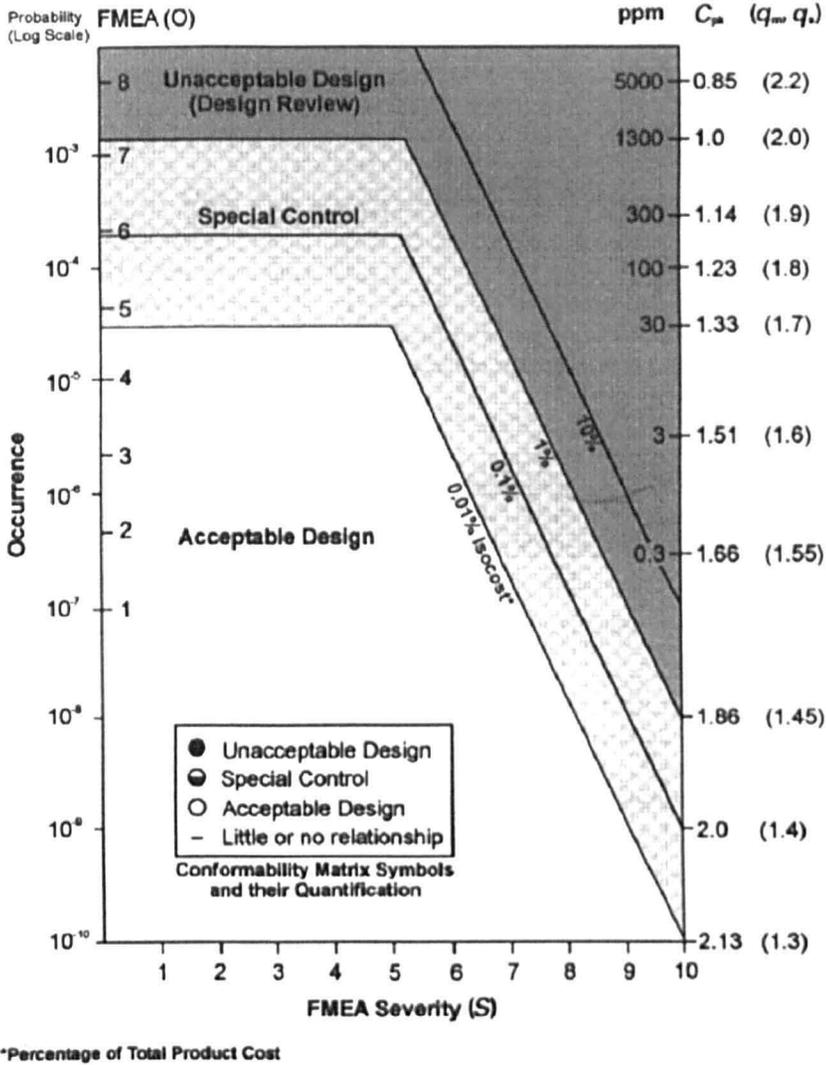


Figure 3-11 Conformability Map [B88]

### 3.9 The Conformability Matrix

The conformability matrix [B88] is the final element of CA bringing together all of the risk data in a form that can be easily read and quickly gives an engineer information on the quality cost implications of a design. The matrix is organised by manufacture and assembly sequence. Each line of the matrix relates to a particular process, for each process the total risk assigned to it using the capability maps is entered and the associated failure modes are described. For each failure mode a level of associated quality costs is then specified using data read from the conformability map. These quality costs may then be summed to determine the total quality cost associated with a design. The use of the matrix has several clear advantages for quality cost assessment:

- all quality costs 0.1% etc. are highlighted and through the matrix completion method are summed. This means that the effects of numerous small quality failures are not ignored.
- The reasons for the occurrence of quality failures and associated quality costs are easily located

### **3.10 CA For Electronics Products**

[B89] first introduces the use of conformability analysis in the design of electronic products, specifically aimed at the mechanical aspects of the design and production of PCB's. The technique developed is essentially a direct adaptation of the methods discussed earlier. The adaptation takes the form of additional CA modules (in the form of PCB specific risk analysis worksheets) tailored to the needs of PCB design and manufacture. The modules cover PCB specifics such as the method of producing holes in the board, artwork layout and soldering techniques. As with assembly risk analysis the design is assessed using a series of worksheets each of which examines a different aspect of the design and assigns risk levels to elements such as component to board edge spacing, component to component spacing, component orientation and hole tolerances. By following through the worksheets the engineer is able to complete a conformability matrix and see which aspects of the design are likely to lead to high quality costs. Advantages and disadvantages of this technique are as for the standard form of conformability analysis, however additional emphasis must be placed upon the need for constant updating of worksheets in the fast moving and fluid field of electronics manufacture additional worksheets must be constantly produced for the numerous new and special techniques developed each year in this fast paced industry.

### **3.11 Software Implementation**

Conformability Analysis is also supported through a software implementation of its workbooks. This software package effectively leads an engineer through the analysis procedure speeding the application as it provides direct access to all of the main components of CA. The software tool guides the user through the use of interactive process capability maps, geometry wizards to produce an estimate of risk which may then be entered into the conformability matrix.

### **3.12 Summary**

CA is a flexible technique which in general is easily applied to a design and provides an engineer with important information regarding the cost consequences of design decisions. The technique is simple relying fundamentally upon a paper based system (although a computerised version is available) hence allowing for future proofing and easy updating of the risk analysis worksheets. The conformability matrix which takes the information gained during the application of the technique at the risk analysis stages and converts it into a complete picture of the design is a novel and powerful tool, and yet is easily operated and understood.

CA is a powerful and accessible technique which may be applied to achieve a number of different aims. These range from determining the level of process capability associated with the manufacture of a particular component / or its assembly through the estimation of quality costs associated with a product through to the comparison of competing or alternative designs on a cost consequence basis. CA is effectively a 'Voice of the Process' expressing the limitations of a design / process combination through an estimate of the quality costs associated with this relationship; as such CA provides a useful tool complementing the 'Voice of the Customer' provided by more traditional tools such as Taguchi analysis.

Conformability analysis has been successful at an industrial level having been adopted by TRW automotive as one of the suite of tools maintained by the organisation for use by its mechanical design teams.

With regard to the applicability of CA to electronic engineering, the usefulness of the established form of the technique is less clear. As previously established [B89] the technique is applicable to the mechanical aspects of electronic products particularly the fabrication and assembly of PCB's and other physical structures. However it is unlikely that CA will be able to successfully capture the highly complex relationships between function, manufacture and test embodied by electronic systems. This limitation is due to the analysis route followed which is not designed to cope with the aspects of performance unrelated to physical form such as those which may be observed in electronic systems.

With regard to electronic products and systems there exists a clear gap in prior research and industrial application with regard to the provision of a technique and supporting tool set able to provide product design guidance with respect to the cost of quality associated with a particular design. Although several techniques including Taguchi have approached the problem from the customer's viewpoint, none have fully addressed the

needs of the manufacturer. The aim of this research is to develop a technique and supporting toolset able to estimate the cost of quality associated with an electronic system in an industrial environment. In order to produce an industrially applicable technique suitable for use in a modern engineering environment this research was case study driven. Each case study was conducted in association with industrial partners whose invested interest was to drive towards the production of a useful and useable technique.

In summary the main objectives of this research where the following:

- **Develop a methodology for the assessment of the Cost of Quality associated with electronic systems**
- **Produce a set of tools capable of supporting the methodology**
- **Where possible provide suitable supporting software**
- **Ensure that the methodology is suitable for its application through the use of several industrially sourced case studies**

## **4 Overview of electronic Conformability Analysis**

### **4.1 Introduction**

The purpose of this chapter is to introduce the Electronic Conformability Analysis (eCA) methodology. The eCA methodology builds upon the Conformability Analysis methodology developed for the analysis of mechanical products. The eCA methodology, which is specifically targeted for application to electronics products, addresses the same DFQ issues as CA; aiming to predict the quality costs a manufacturer will experience as a result of design, manufacture and assembly decisions. Whilst at the same time providing information which may be used to target design improvements as well as forming a basis for design comparison.

### **4.2 Need for the Methodology**

DFQ issues have been addressed by a number of different methodologies and techniques with respect to mechanical designs, and in the electronic field DFQ has also been well covered with respect to VLSI designs. However with regard to more general electronic systems design for quality is less structured and has not been addressed to the same extent. Typically DFQ carried out for general PCB based electronic system is disjointed and incomplete, with different aspects of the system receiving different levels of coverage.

When DFQ solutions are applied to a general PCB based electronic systems they are often based around the use of ad-hoc simulation in combination with the application of legacy design rules; often contained in numerous volumes of difficult to follow literature. Although this situation has improved with the development of Design Rule Checking software which is incorporated into CAD tools [B90;B91] the process is still overly complex to apply. Design rules are also difficult and expensive to maintain in the quickly changing electronics industry. As a result of this such systems are severely underused typically receiving support from only a few members of a design team. Further to this, with the increased emphasis upon product quality due to an increasingly competitive marketplace and a general adoption of quality methodologies, particularly Six Sigma, DFQ issues have become and are becoming increasingly relevant. Particularly necessary for the successful implementation of a Six Sigma based policy is that product quality must be considered by all members of an engineering team at all stages of the product lifecycle and the impact of decisions made during one stage upon

other stages must be carefully considered. Often whilst producing a new design or reviewing a current design with the aim of further development and improvement engineering teams consider only the levels of manufacturing tolerance that the product can accept before it becomes non-functional as opposed to the levels of manufacturing tolerance that it must accept and still function. Further to this when a product is found to have poor yield due to the variation of an established process which will often be pushed to its limits by contemporary designs, a common reaction is to require processes to achieve tighter tolerances. Although this may in some cases be appropriate and possible, in a large number of cases this will not be true. In such a situation the result of this action may well be a further reduction of product yield this is directly opposed to the expected increased yield. In this situation a more appropriate action would be to consider if the design may be changed to accommodate the variation associated with such a process. This concept that a product must be robust to the variation of the processes producing it is poorly understood in the electronics sector. Although existing tools such as Taguchi Analysis address this concept they are often seen as conceptually difficult to understand and are hence rejected. Similarly although the Six Sigma methodology should be able to address such problems there is some considerable resistance to it due to its perceived inflexibility and potentially laborious project structure. This is especially the case in companies developing new products based upon leading edge technology. Further to these points existing techniques do not provide a direct path to the estimation of the quality costs associated with the multifaceted and highly interdependent nature of electronic systems, such a path is available for mechanical products through the application of CA. Existing tools are also somewhat deficient with respects to the differing needs of the three major aspects of electronic systems from which quality costs may emanate. This resistance to the existing techniques and the lack of a direct path to the estimation of quality costs associated with the CTQ aspects of an electronic system together with the need for quality assessment systems able to cope with the three main sources of quality costs associated with electronic systems exposes the need for a new methodology designed specifically for application to the development of electronic systems and catering specifically for the needs of this engineering sector. Such a technique must also be compatible with existing quality techniques and methodologies with a minimum of crossover. In summary there is a clear need for an easily understood quality assessment technique for electronic systems which is capable of producing reliable quality cost estimates in each of the three major domains of electronic systems.

### 4.3 Overview of the Technique

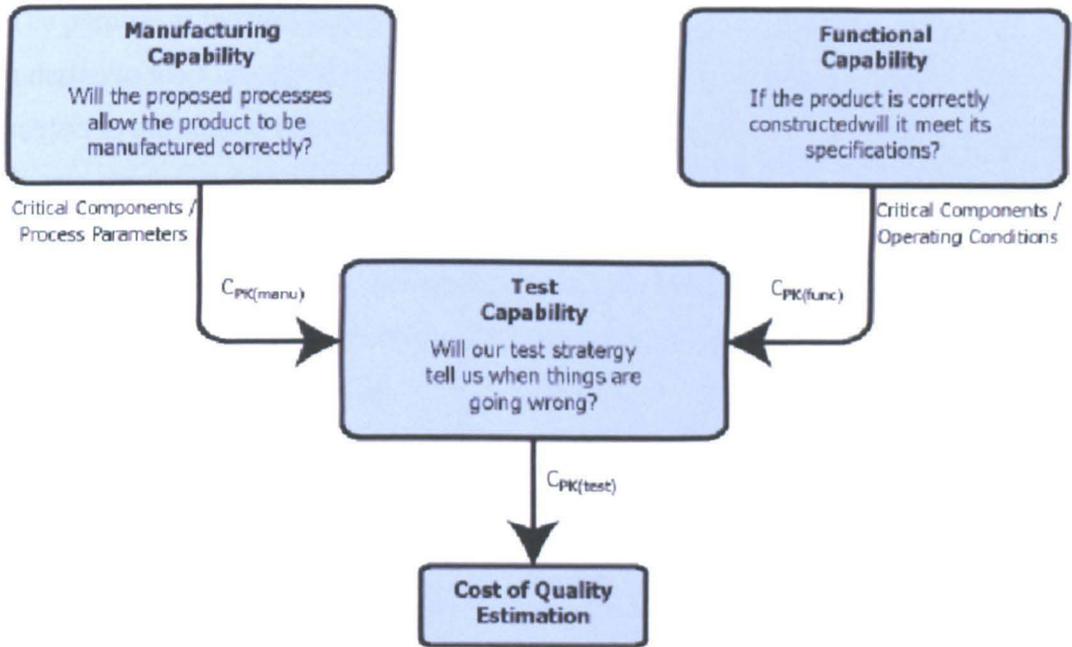


Figure 4-1 The Three Elements of eCA

DFQ issues are manifested as faults, such faults in a product may take several different forms and arise from a number of different sources. For example a product may experience parametric faults due to an oversensitivity or lack of robustness to tolerance variations in components. Alternatively a product may be exposed to faults due to failures in manufacturing processes. Faults from either of these sources will cause quality costs to be incurred by the manufacturer, and it is at once obvious that these costs will depend upon when a fault is discovered. For example a fault detected close to the source and time of its introduction by the testing regime in place during the manufacturing process will have a lower associated quality cost and a smaller impact on a manufacturer than a fault detected once a product has been passed onto a customer or user. The eCA technique accounts for and makes an estimate of these potential quality costs through the use of the unified design analysis framework which is illustrated in Figure 4-1, the frame work consists of three individual modules each with a distinct purpose which may be used separately or more usefully in combination with the other modules to provide an estimation of the potential quality costs a manufacturer is exposed to by a product. This information enables sensible decisions to be taken and improvements to be made in order to bring the various processes involved under a greater level of control.

## 4.4 Functional Capability

The purpose of the functional capability module is to provide a measure of the ability of a design to meet the specified required performance levels if manufactured correctly but subject to the normal statistical variation in component parameters. In effect this module gives a quick measure of the robustness of a design with regard to the intended range of parametric variation in its component parts. The functional analysis also provides additional key information indicating the significance of the contribution made by individual circuit parameters to the overall circuit performance.

The results of this analysis are provided both in the form of capability data using a version of the  $C_{pk}$  PCI ( $C_{pk(func)}$ ) along with an estimate of the number of expected defects expressed in Defects Per Million Opportunities (DPMO). This data is conveniently presented for individual design specifications in the form of a capability breakdown as shown below in Figure 4-2 and discussed in detail in chapter 6.

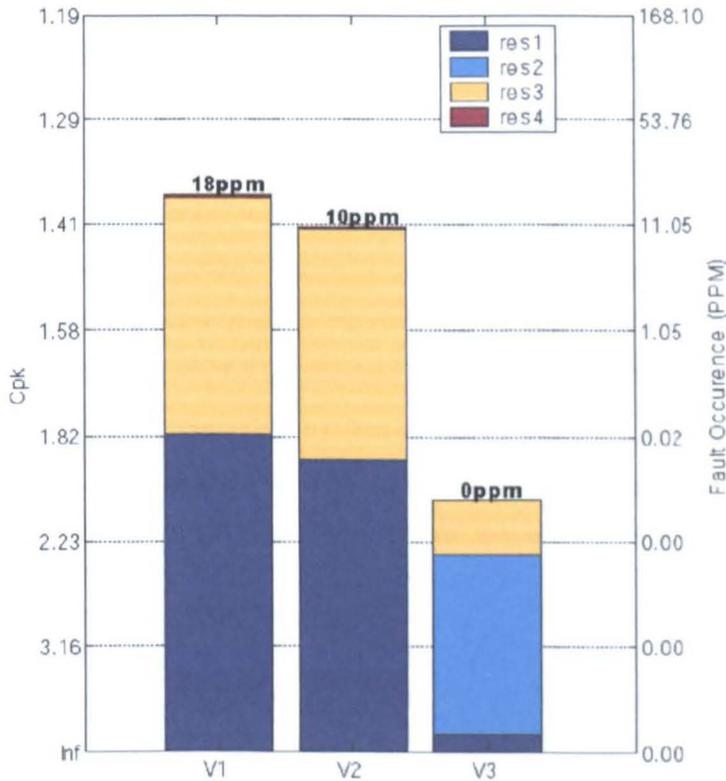


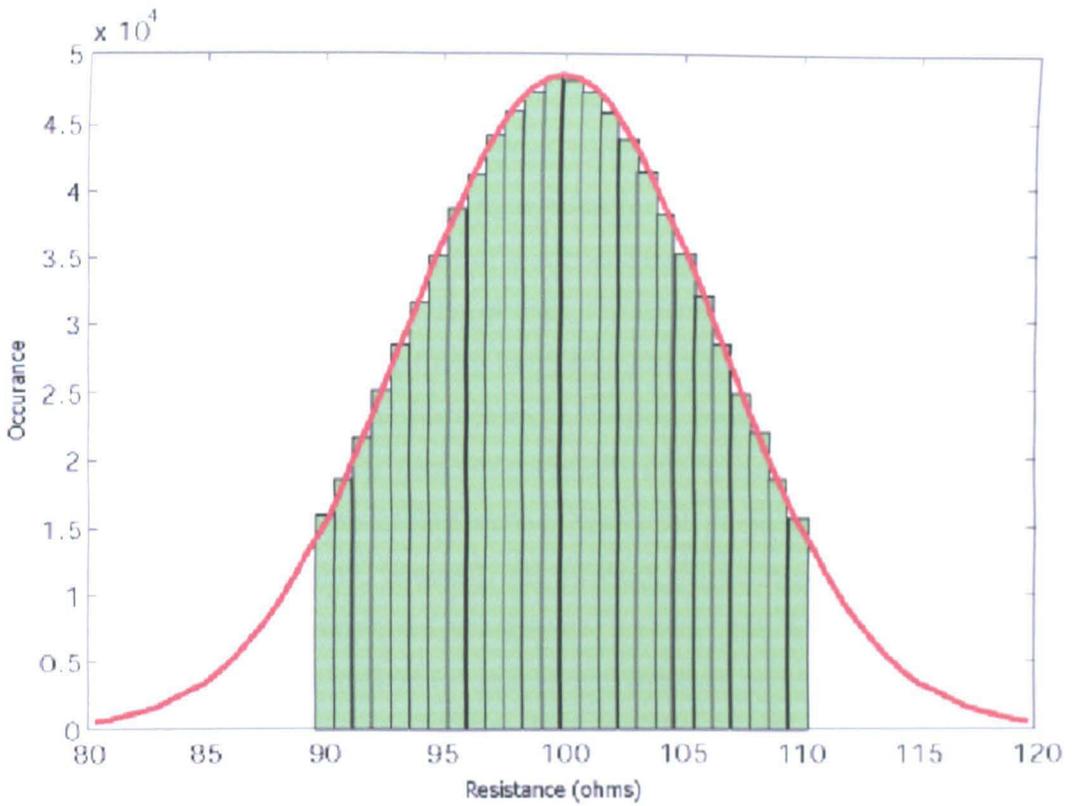
Figure 4-2 An Example Capability Breakdown

The usefulness of this module is easily understood through the use of a simple example. Consider that given a filter the application of this module would quickly allow an engineer to calculate the capability of the proposed circuit in meeting its specification for commonly used measures such as Gain, Bandwidth and Q; whilst also providing an

estimation of the significance of the contribution of each circuit component to each metric.

#### **4.5 The Effects of Variability on Functionality**

The most basic CTQ aspect of a product is its conformance to its functional specification if design tolerances are held. A lack of conformance given that design tolerances are held would indicate that a product is unlikely to attain any level of conformance if design tolerances slip during manufacture. Any loss of conformance would lead to quality loss and hence incur an associated cost of quality for the manufacturer. Any quality costs arising in this way can typically be broken down into several sub categories, cost of rework, scrap or replacement for example. Any lack of conformance when design tolerances are held stems from a poor design, although the problematic aspects of a design may not be immediately apparent. It is commonly accepted that electronics designers must deal with a wide spectrum of problems, many of which will stem from the fact that they do not have complete control of component parts which are used to fabricate a product. Further to this the component parts of the product cannot be made perfectly and will all, to greater or lesser extent, demonstrate some basic parametric variation which may also vary with environmental conditions. The simplest examples of parametric variation are encountered when dealing with common passive components. For example resistors are typically specified to a defined value  $x$  with a tolerance of  $y\%$  hence the true value of the resistor is not known. This situation may be further complicated by any selective grouping procedure carried out upon the component. For example consider that the spread of values taken by a single batch of resistors will typically take the form of a truncated normal distribution as shown in Figure 4-3.



**Figure 4-3 Distribution of Resistor Values with a Nominal Value of 100 Ohms and 10% Tolerance**

More complex components will generally have more complex parametric variations although these are often not specified explicitly. However the characteristics may be expressed by some component models which have been constructed based upon characterisation experiments. The cumulative effect of these parametric variations will possibly be to negatively influence the performance of the product as a whole. Further to the influence of parametric effects other variations from unidentified sources known as noise factors (such noise factors do not include environmental factors such as temperature and humidity) may also affect the product. Typically noise sources may include outer noise from external factors such as temperature and other environmental conditions and inner noise from internal factors for example changes in the product due to age (this is a particularly common problem when using electrolytic capacitors).

In a well designed robust system the effects of these variations should be rendered negligible however in many cases this is not found to be the case. Problems are often discovered when prototype products are produced and the measured performance may be found to differ from the expected performance hence requiring expensive redesign.

## **4.6 Controlling Variability**

A design which is not significantly effected by parametric variation is known as a robust design. The most common method applied to a design with the aim of achieving a robust design, is to apply extremely tight tolerance limits across all components in a product. For example in the pursuit of a robust design an engineer might replace all resistors with 10% tolerance with 5% or even 1% tolerance components. There are two defects with this design strategy firstly the practice increases the total cost of a product due to the increased cost of the sum of its component parts (given the assumption that higher precision / performance parts are more expensive) and yet does not increase the value of the product in terms of its function. Hence the profit margin is reduced due to an increased cost of quality. Secondly the strategy does not actually produce a true robust design; instead it simply reduces the total variability in the circuit with respect to the main signals. A better method for variability control i.e. one with a lower associated cost of quality would be to use information about the weak aspects of a design to implement targeted design improvements or alternatively to use the same information to implement targeted tolerance allocation based upon the impact of a component s value on functional performance.

## **4.7 Assessing Variability**

Circuit designers are not new to the concept of variability assessment, as discussed in the background given in chapter 1 a number of techniques already exist and are used to assess the performance of circuit design under parametric variation. However despite the widely available statistically advanced tools for the assessment of circuit functional variability, and despite the wide use of such tools by design engineers, the potential benefits are often not fully exploited. The reason for this lack of exploitation is a general lack of interest expressed by design engineers in using complex statistical analysis tools. The functional assessment module designed in this work provides a means to harness the power of statistical analysis tools through the use of capability analysis in a form which is more readily accepted by engineers. As capability may be described as the relationship between variability and specification, functional capability may be expressed as:

$$C_{pk(func)} = \frac{\text{Function\_Performace\_Variation}}{\text{Function\_Specification}}$$

upon examination of this equation we see that in order to assess the functional capability of a product we must first quantify the performance variations.

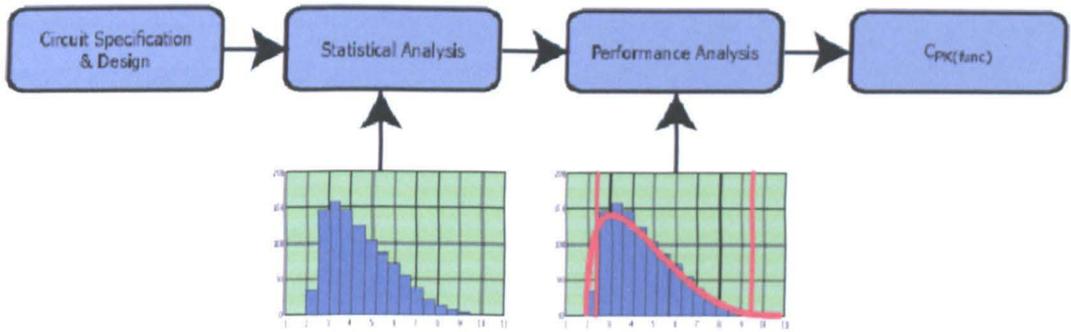


Figure 4-4 Functional Capability Assessment

The first step in assessing functional capability is to define the critical performance measures for the circuit or part of circuit in question. When applying eCA within a Six Sigma framework the definition of these critical measures will usually be simple as they should be related to the CTQ factors identified during the project define stage. Once suitable measures have been defined, specification limits should be identified for these performance measures. These limits will generally be based upon the performance limits defined in the projects statement of requirements created during the systems engineering stage of the project. For example considering a band pass filter the critical measures of performance based upon the customers CTQ's may be the centre frequency of the pass band and the width of the band.

Once the critical performance parameters have been defined, functional capability is assessed by carrying out a statistical analysis of the circuit under parametric variation using a technique such as Monte Carlo analysis. Typically tools for the application of such a statistical analysis are included with even the most basic circuit analysis software. This analysis may be carried out at any appropriate level of abstraction from behavioural up and in any mix so long as performance data for the aspects of interest is produced. The results from the statistical analysis form the basis for the capability breakdown as discussed in chapter 1. This automated method of data analysis and simplified presentation of the data provides a simple route for engineers to follow in order to assess the functional performance of a product.

## 4.8 Manufacturing Capability

The manufacturing capability module provides a methodology which may be followed to enable the assessment of the manufacturability of a product, circuit or sub circuit with

regard to the process capability of the manufacturing route. This analysis is key to the concept of conformability analysis relating a design to manufacturing capability in a unique manner. The need to know this relationship is crucial to achieving a high level of production quality, and it directly opposes the traditional ‘over the wall’ engineering practice observed as a product is passed from design to manufacture. Due to this ‘over the wall’ practice the traditional approach to achieving high quality levels in production is directed only at improving production processes. This as illustrated in Figure 4-5, is inefficient, as it implies that quality costs may be easily reduced by improving manufacturing processes. The new approach favoured by the eCA methodology is directed at ensuring manufacturing considerations are taken into account whilst designing a product.

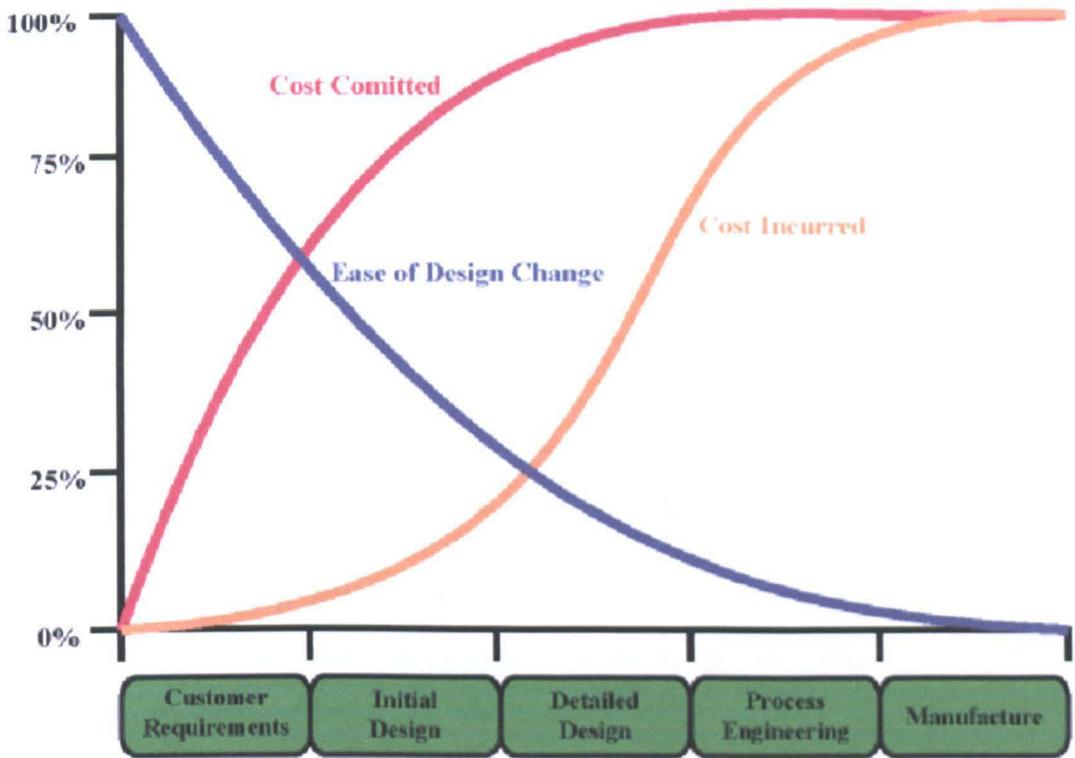


Figure 4-5 Illustration of Cost Committed as a Project Progresses

The benefits of the application of this module are multifaceted and include, amongst others, reduced production costs and associated failure costs, reduced design revisions and lower overall quality costs.

#### 4.9 The Effects of Variability on Manufacture

The most visible effect of manufacturing variability is a reduction in product yield and hence an associated increase in the cost of quality manifested as higher costs incurred by rework and/or scrap. Further to these ‘first level’ effects are second level effects

experienced by customers which are manifested in terms of reduced reliability and field failures. The potential spectrum and impact of manufacturing process variability upon a product is large, ranging from relatively minor defects such as cosmetic blemishes through catastrophic defects and on to major defects causing decreased product life and reliability with the associated risks and consequences of possible product failure whilst in operation. Typically attempts are made to control the potential effects of manufacturing variability through the use of process control and monitoring techniques. The most successful process control techniques used preventively to limit variability are SPC and Poka Yoke. Production test systems are also frequently employed to monitor manufactured products although these are only able to detect defects once they have occurred they can be used diagnostically to implement process changes. Manufacturing defects caused by process variability may be placed into one of two categories:

- **Special Cause** – those defects due to a random or unusually difficult to predict or control event. Defects caused by faulty incoming parts could be placed into this category.
- **Product Design Failure** – those defects which may have been avoided if the correct analysis of a product had been carried out. Hence these failures could have been predicted and preventative actions taken. Such actions could include design or process changes.
- **Process Design Failure** – those defects which occur due to the use of a process which is unsuitable for application to the product.

#### **4.10 Assessing Variability**

Within the eCA framework manufacturing variability may be assessed through the use of one of four tools or through any combination of them; this flexibility allows the most suitable assessment method to be chosen for a particular design.

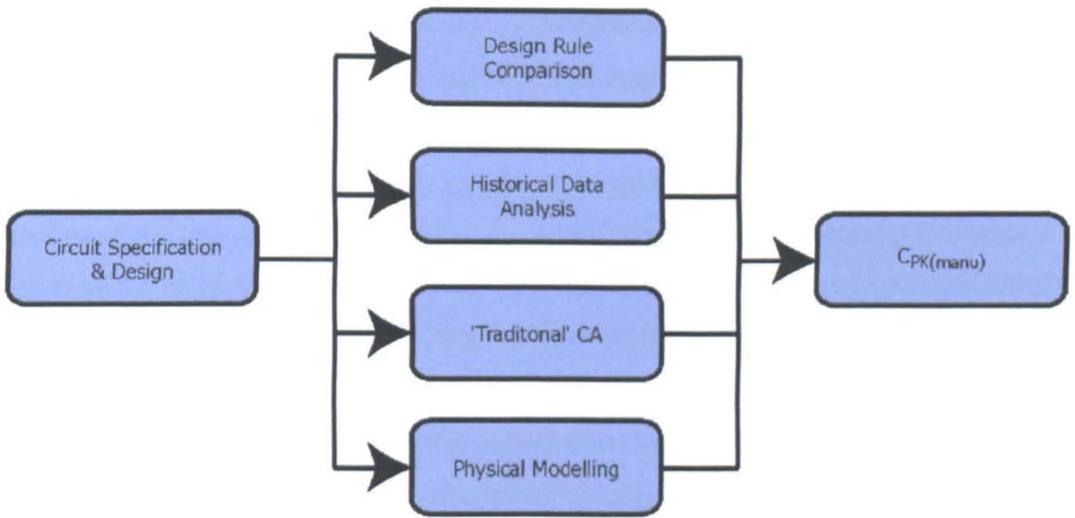


Figure 4-6 Manufacturing Analysis Route

The design rule comparison method both encapsulates an element of historical data analysis and provides the simplest technique for the analysis of manufacturing capability. Analysis carried out using design rule comparison could be implemented through the use of specially modified design rules. The rules are modified by adding a small amount of additional data to established design rules such that an assessment can be made of the likely occurrence of manufacturing failure. This data should typically be derived from internal experience (historical data) or where no internal experience exists from information provided by the process supplier.

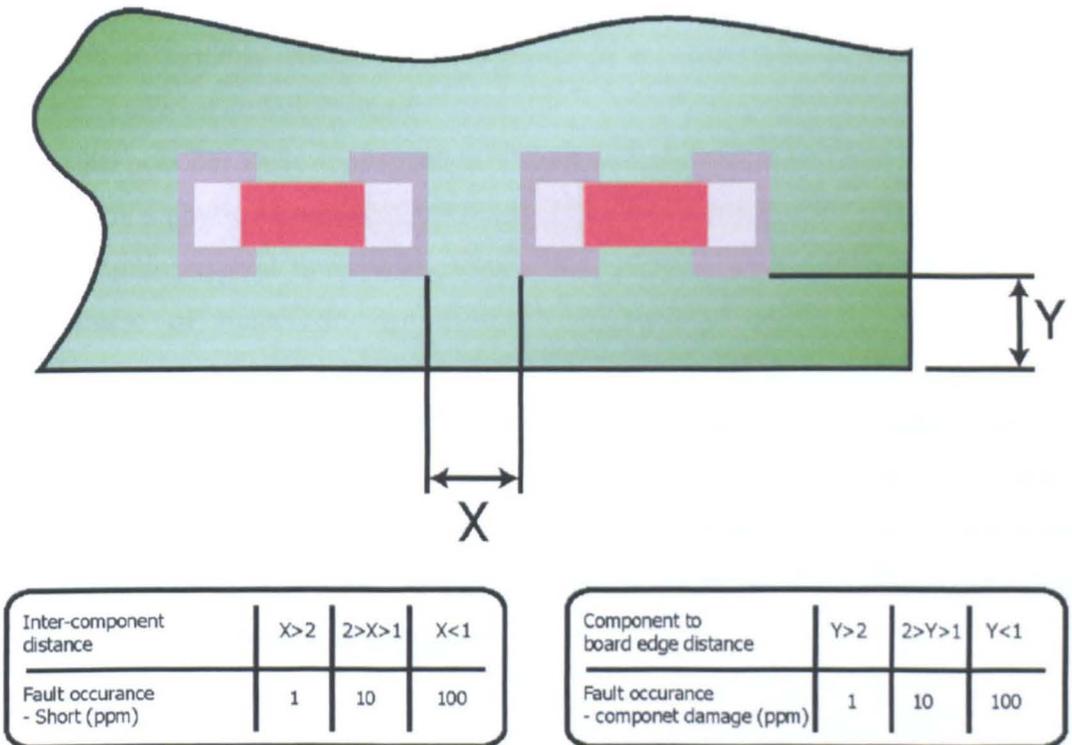


Figure 4-7 A modified design rule

A typically modified design rule is shown in Figure 4-7. The modification consists of the addition of data detailing expected fault occurrence rates. In this example the fault occurrence rates are given as a function of inter-component spacing and component to board edge distances. Alternatively the defect occurrence rate could be expressed as a function of a components distance from the edge of the PCB, or component separation. The analysis of historical data also provides relatively direct access to manufacturing defect occurrence rates. Historical data analysis works by estimating defect occurrence rates by comparing common elements of current and future designs to previously and currently manufactured products. The major draw back of the historical data analysis technique is the need to verify the validity of the collected data; this should however not be a serious problem as numerous standard techniques exist detailing methods for the collection and verification of manufacturing data. When collecting and using historical data a certain amount of flexibility in interpretation may be applied for example given that electronic packaging is in general standardised we may easily infer failure rates experienced when placing a particular kind of package from one product to another. Design Rule comparison and Historical data analysis are particularly suited to the analysis of mass manufactured PCB based products where inspection systems capable of achieving high levels of defect coverage are typically employed.

The third potential source of capability data regarding the manufacturability of a product is to apply the 'traditional' or standard form of conformability analysis; this route is particularly suited to the analysis of the assembly capability mechanical elements of mechatronic systems.

The final possible route which may provide an estimation of manufacturing capability is to employ a physical modelling technique. Providing that suitable skills exist within an organisation physical modelling provides a convenient and flexible method for the assessment of manufacturing variability particularly suited to the analysis of mechatronic systems or unusual electronic assemblies. An analysis carried out following this route would closely resemble the functional analysis stage in terms of application. The physical model should allow the ability of a process to construct a product to be assessed, possibly in terms of the functional performance of the device. An example of the application of this technique is discussed in the Torque and Angle Sensor case study presented in chapter 9.

## 4.11 Test Capability

The purpose of the test capability module is to provide a structured framework for the assessment of the effectiveness of the proposed testing procedure which may be expressed in terms of test defects. The module classifies test defects according to the definitions given in Figure 4-8 for Type I and II errors, each of which will have different associated quality costs. Through the analysis of test procedures quality costs may be reduced through the application of targeted test improvements including both the removal of inappropriate or un required testing procedures and the addition of new testing procedures.

## 4.12 The Effect of Variability on Test

There are four major sources of variability in the testing process:

- Variability in the circuit function cause by the normal parametric variation of components
- Variability in circuit function caused by abnormal parametric variation in components
- Variation in circuit function caused by manufacturing defects
- Variation in the testing process itself caused by imprecise control of the system or external influences such as temperature and noise

The effects of these sources of test variability upon a given testing procedure is potentially to cause one of two different test errors as illustrated in Figure 4-8, the cost consequences of each error category differ. A Type II error has potentially the largest quality cost consequence depending both upon the production stage at which the test error occurs, and the severity of the resulting error.

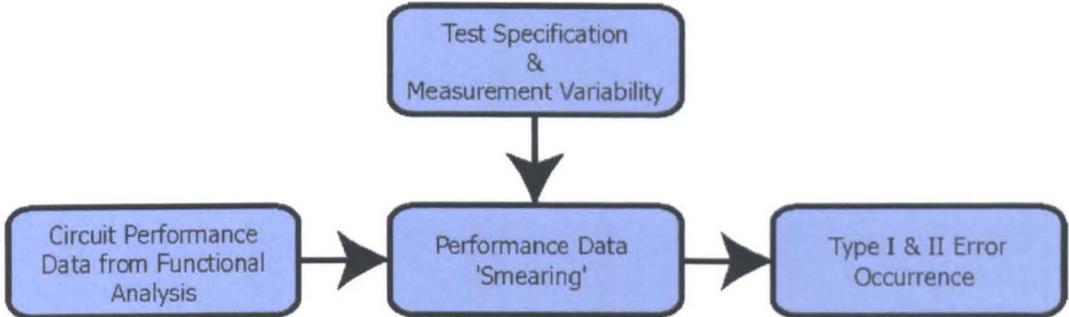
	Pass	Fail
Defect Free Circuit	OK	Type I
Defective Circuit	Type II	OK

Figure 4-8 Test Error Categories

For example the failure to detect a defect with the potential to cause a safety critical failure has a higher associated quality cost than a failure to detect a defect which does not cause any detriment to product function but only causes cosmetic defects.

### 4.13 Assessing Variability

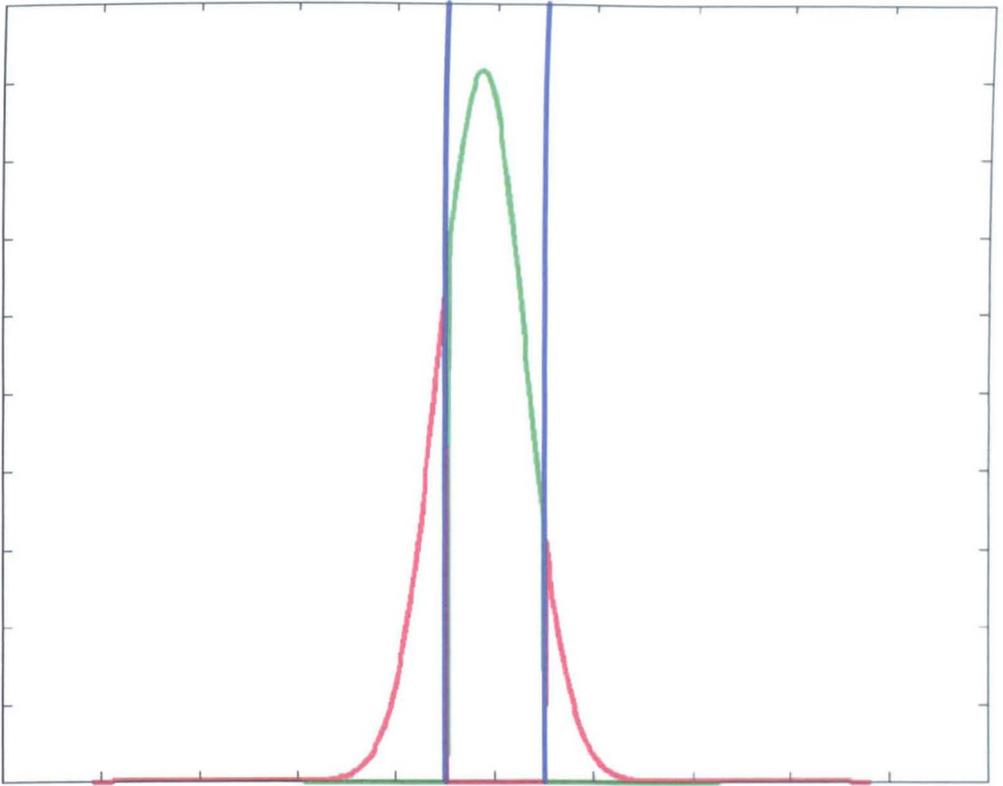
The assessment of test variability is a two stage process with one stage targeted at detecting the rate of occurrence of both error types for circuits with the potential for only 'soft defects' (those defects caused by parametric variation). The second stage is used to determine the occurrence of Type II errors for circuits containing 'hard defects'.



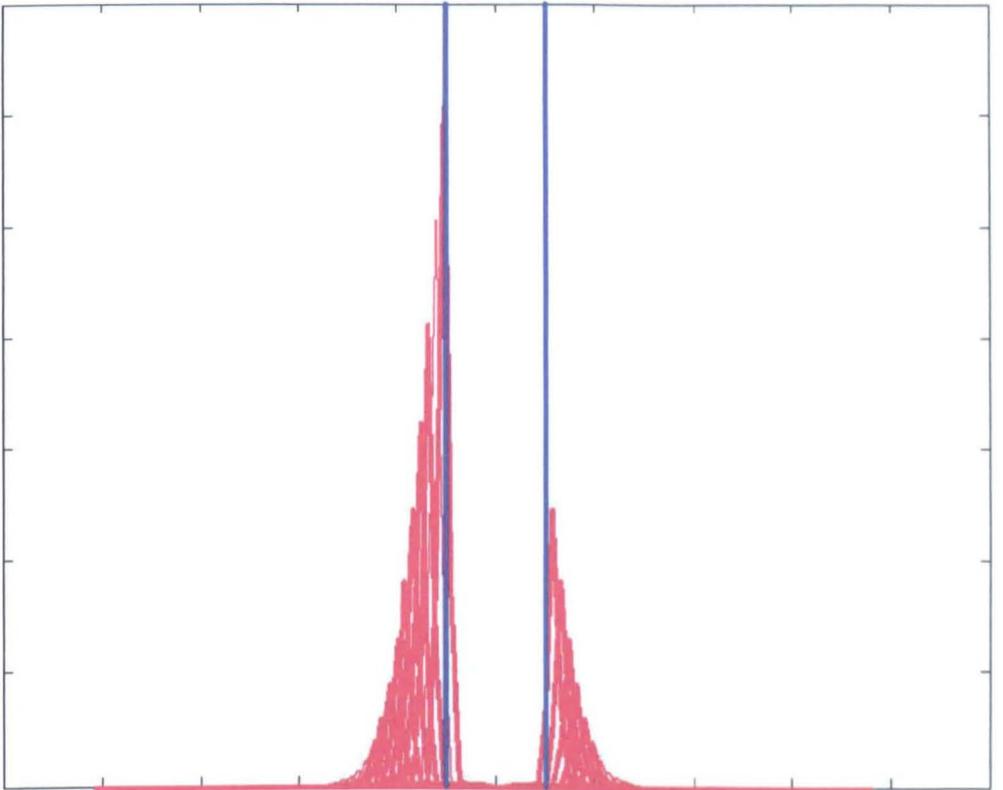
**Figure 4-9 Assessment of Type I & II Error Occurrence Caused by 'Soft Defects'**

The estimation of test errors caused by soft defects is the simpler of the two stages. It makes use of the circuit performance data generated during the functional analysis step of the analysis procedure or requires the generation of suitable alternative data using a statistical analysis technique such as Monte Carlo analysis. This data is then 'smeared' itself a three stage process as detailed below:

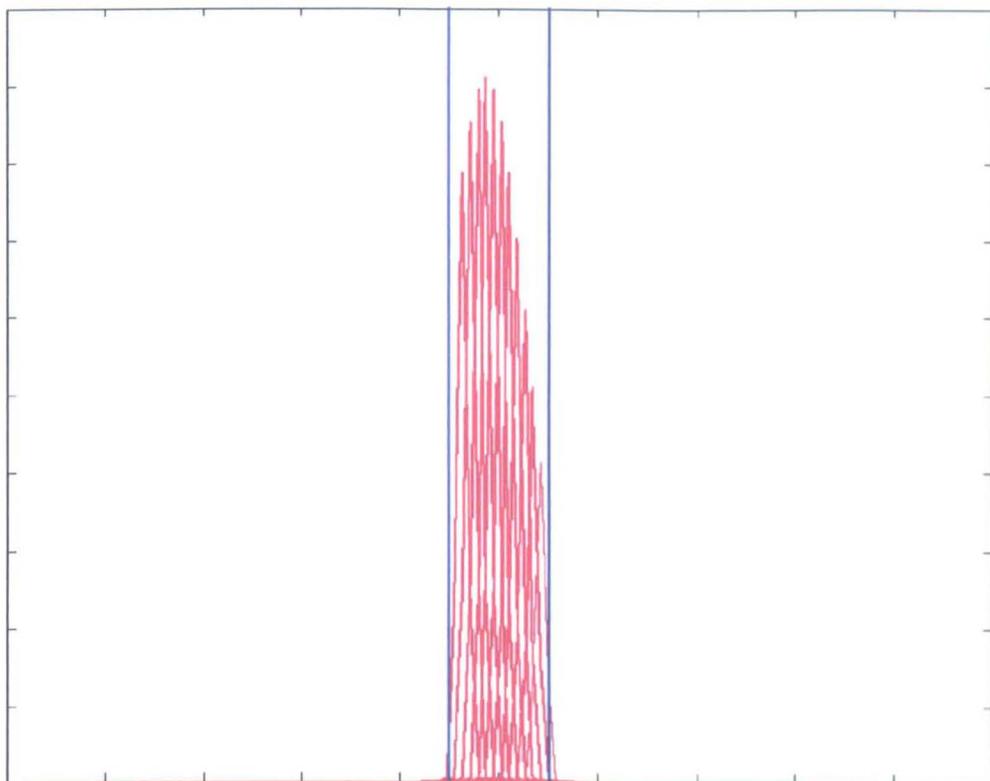
1. The probability density function representing the performance measure of interest is first split into two separate distributions (Figure 4-10)
  - a. A 'Good' or pass distribution of those points falling inside the test limits as shown in green on Figure 4-10
  - b. A 'Bad' or failing distribution of those points falling outside the test limits as shown in red on Figure 4-10
2. By defining the expected maximum measurement variability as the three sigma point on a measurement noise PDF a noise PDF is now calculated for each point in the 'Good' and 'Bad' distributions, this is illustrated below in Figure 4-11 & Figure 4-12
3. These individual 'PDF's for each point within the separated distributions may now be summed to give two new PDF's showing the 'Good' and 'Bad' PDF's as they will appear to the test equipment as shown in Figure 4-13 & Figure 4-14



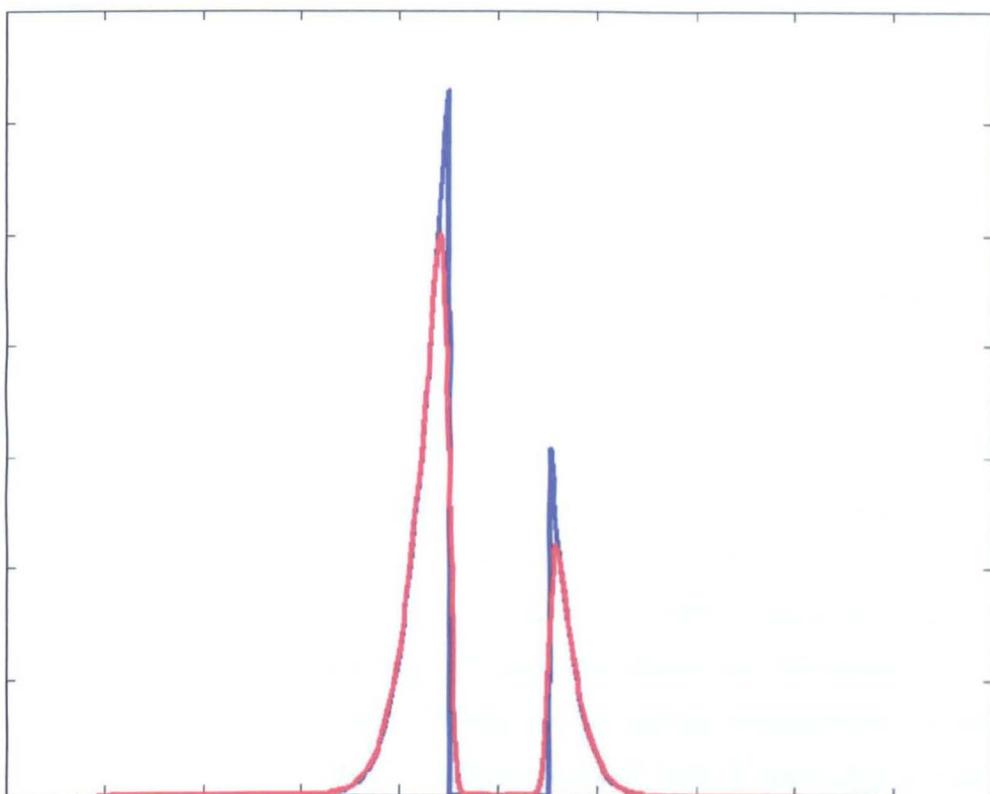
**Figure 4-10 A PDF Split Into Passing and Failing Portions**



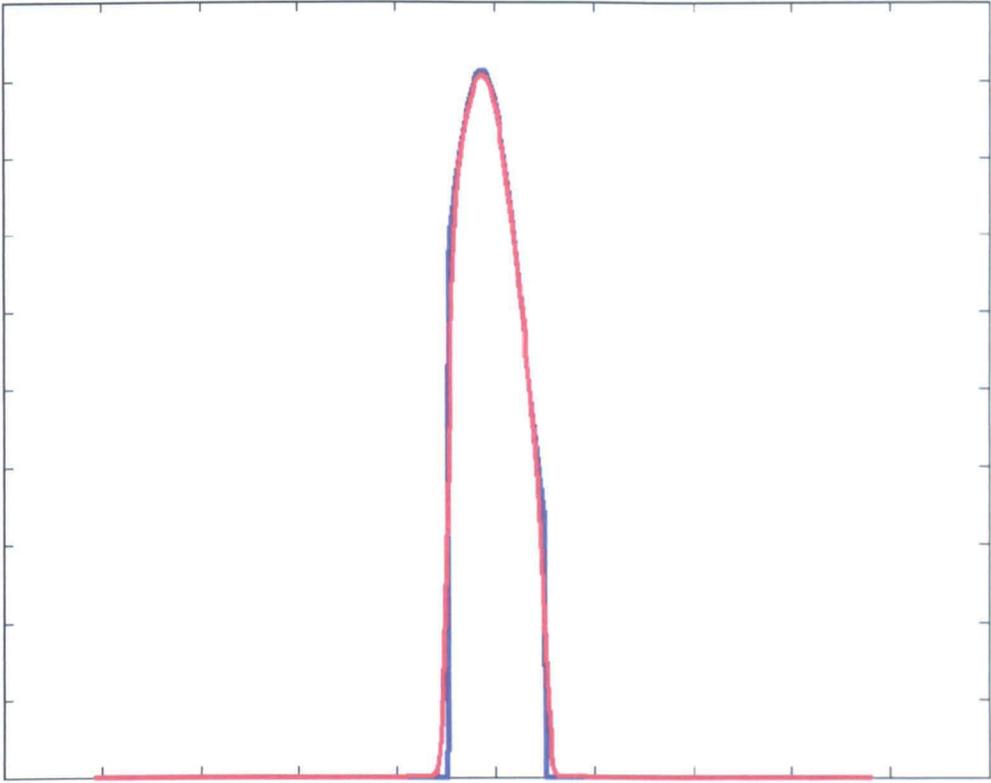
**Figure 4-11 The Individual 'Bad' Distributions**



**Figure 4-12 The Individual 'Good' Distributions**



**Figure 4-13 The New 'Bad' Distribution (in Red) Shown with the Original PDF (in Blue)**

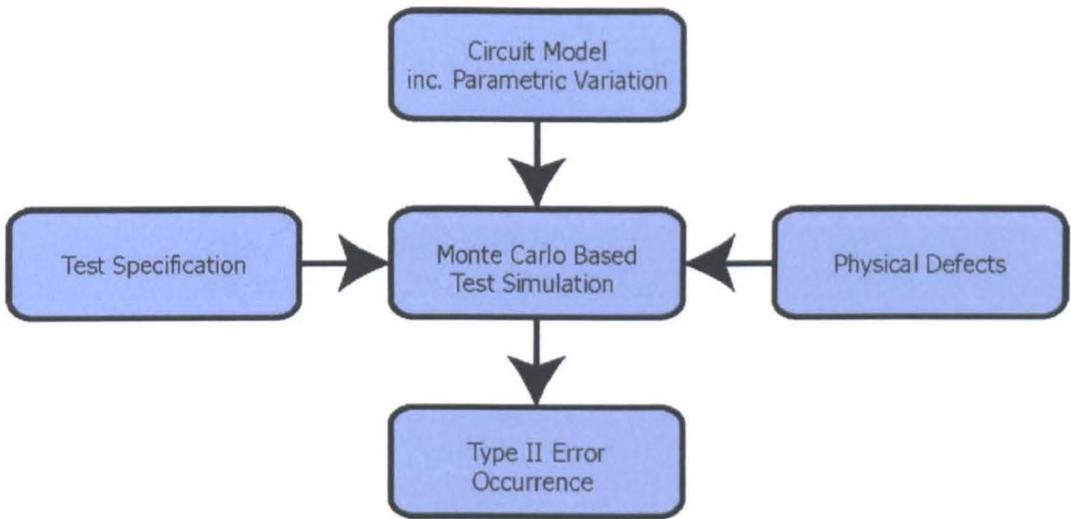


**Figure 4-14 The New 'Good' Distribution (in Red) Shown With the Original PDF (in Blue)**

This smeared data may now be used to calculate the occurrence of Type I and II test errors. This is achieved by using the new PDF's firstly to calculate the probability of 'Good' circuit appearing to exceed the test limits and secondly to calculate the probability of a 'Bad' circuit appearing to fall inside the test limits.

The potential accuracy of this procedure is very high with the main limitation being the number of points at which the distributions are calculated. The effect of using too few points can be seen in Figure 4-11 & Figure 4-12 where individual distributions are easily distinguished. However with modern fast computers it is simple and fast to achieve a sufficiently high resolution for acceptable results.

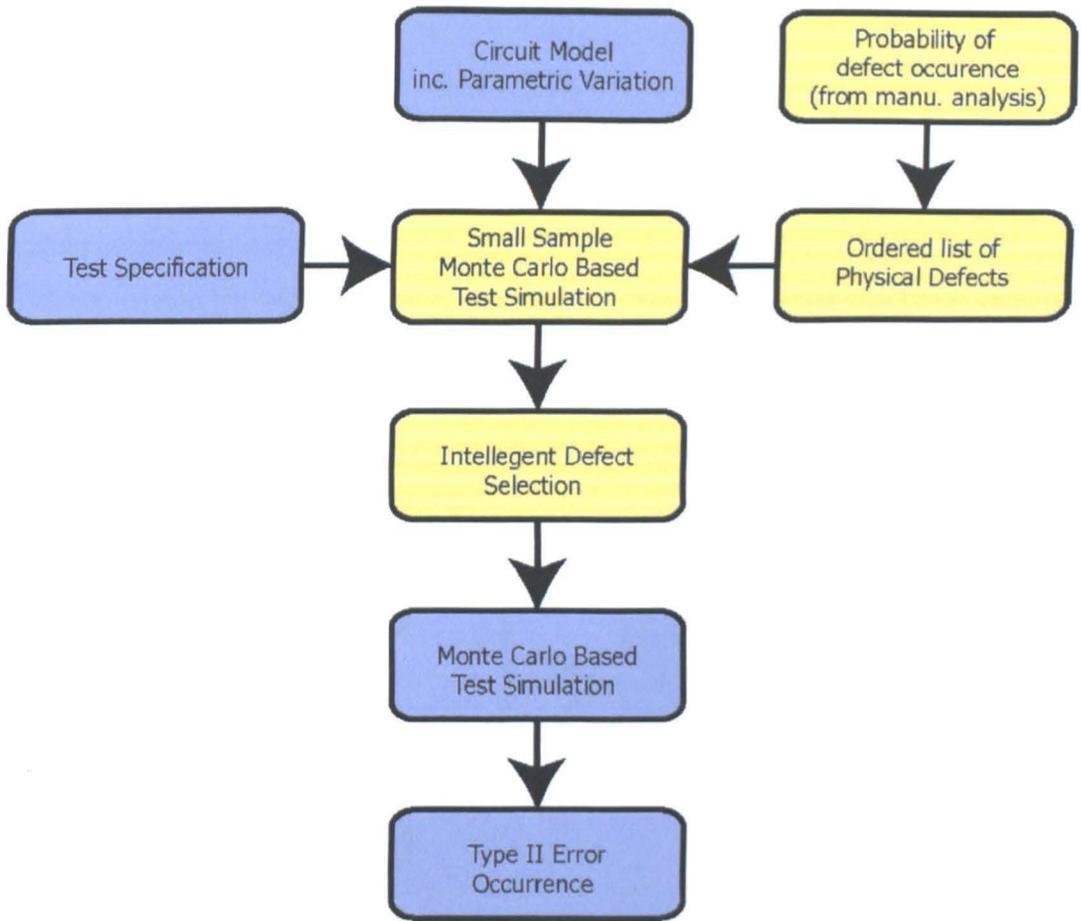
In summary this is a relatively simple procedure and importantly is not a particularly computationally expensive procedure requiring only a single Monte Carlo analysis during which all of the performance measures of interest may be observed or alternatively and more efficiently the data generated during any previously carried out functional analysis may be reanalysed taking into account test measurement equipment. Conversely the estimation of the rate of occurrence of Type II errors due to 'Hard' or physical defects is more complex and could be extremely computationally expensive, the procedure is illustrated below in Figure 4-15.



**Figure 4-15 Assessment of Type II Error Occurrence Due to 'Hard' Defects**

The procedure requires that for each identified potential defect a 'defective' circuit model is created and then statistically modelled effectively modelling the application of a test or inspection procedure to the circuit [B92;B76]. The circuit's performance measures are then examined and using the same procedure as explained above the rate of occurrence of Type II test errors is determined (note that a Type I test error is impossible as no good circuits exist). Due to the potentially high computational cost of this analysis method an improved version is illustrated below in Figure 4-16. Here we see that the efficiency of the analysis may be significantly increased through two improvements:

- The defects for which the analysis is carried out may be selected using an ordered defect list generated from the data gained during the manufacturing analysis stage. Only the most significant defects should be investigated at first, with subsequent investigations gradually investigating all defects as significant problems are removed.
- Secondly the process may be further improved through the use of an 'intelligent' simulation program as described below.



**Figure 4-16 Assessment of Type II Test Error Occurrence Due to 'Hard' Defects**

The estimation of Type II error occurrence commences with small sample Monte Carlo simulations, this involves  $n$  separate Monte Carlo simulations where  $n$  is the total number of potential defects, each simulation run should consist of the minimum permissible number of samples of the population, in general this is around 30 samples [B46]. Once the initial analysis has been completed for each fault engineering judgement must be used to classify the expected success of the test in terms of the predicted occurrence of Type II errors, this is best done through a three tier classification system. In this system the possibility of type II errors are classified into three groups Likely, Unlikely and Unsure. These classifications are now used as the basis for a series of more significant Monte Carlo simulations; both the Likely and the Unsure groups must be extensively simulated in order to calculate the occurrence of Type II errors.

Following the completion of the estimation of Type I and II errors the capability of the testing process may, if desired, be calculated through the use of the capability/occurrence relationship detailed in chapter 1. This will result in three values of  $C_{pk}$  for test:

- An overall value  $C_{PK(\text{Test})}$
- A value for Type I errors  $C_{PK(\text{Test Type I})}$
- A value for Type II errors  $C_{PK(\text{Test Type II})}$

The overall value encompasses all of the potential test errors whilst the subsidiary values account for only the relevant errors.

The conversion between occurrence and capability indices is not a strict requirement of the test analysis module, test failures are commonly expressed as rates of occurrence (DPMO & PPM are commonly used) hence it may well be more convenient not to carry out this conversion when communicating with production / test engineers.

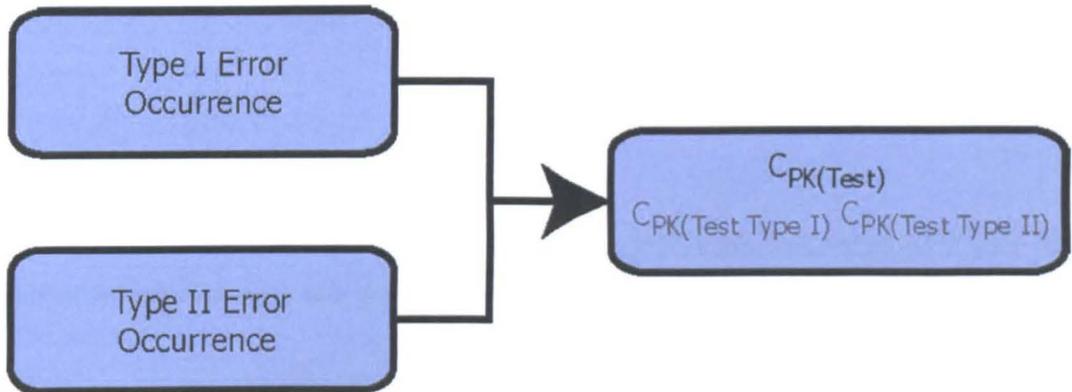


Figure 4-17 Calculation of Test Capability

#### 4.14 The effect and cost of a defect

This section introduces the concept that defects do not only have a probability of occurring which may be determined as discussed in the previous sections but also an associated cost which is dependent upon the potential effects of a defect and its rate of occurrence.

#### 4.15 The effect of a defect

Thus far methods for the determination of both process capability and associated failure rates within the context of electronic products have been discussed, the varying consequences of different defects has not been considered. The FMEA scale provides a measure of the severity of the consequences of a particular defect. The FMEA severity scale is defined entirely in respect to the effect that a failure has on the customer. In the analysis of manufacturing capability, we are concerned with the capability of a design to be manufactured correctly and the effect that this has on the supply chain. We therefore use a modified scale developed by Field and Swift [B88] called Impact (Severity): The definition of Impact (Severity) utilises the widely accepted “rule of ten” of failure costs.

This rule states that costs of failure generally increase tenfold at each process step in the supply chain where the failure is detected. Thus a reject from the customer costs the unit price (the cost of a replacement unit plus the profit element to pay for the handling and disruption), a fault found at final assembly costs 10% of product price, a subassembly fault 1%, etc. Working up the supply chain, warranty returns probably cost ten times the price of the original unit, with re-fitting costs, investigations, etc. It is difficult to put a cost on more severe failures: breach of the statutory requirements or product liability cases. Investigations of insurance cover requirements for various potential liabilities have lead to indicative ratings included in Figure 4-18.

Alternatively, the cost model represented in Figure 4-18 may be written as:

$$C_d = 10^{I-4}$$

where  $C_d$  is the average quality cost resulting from a single occurrence of a fault with impact severity rating  $I_i$  as a proportion of the cost of a single product

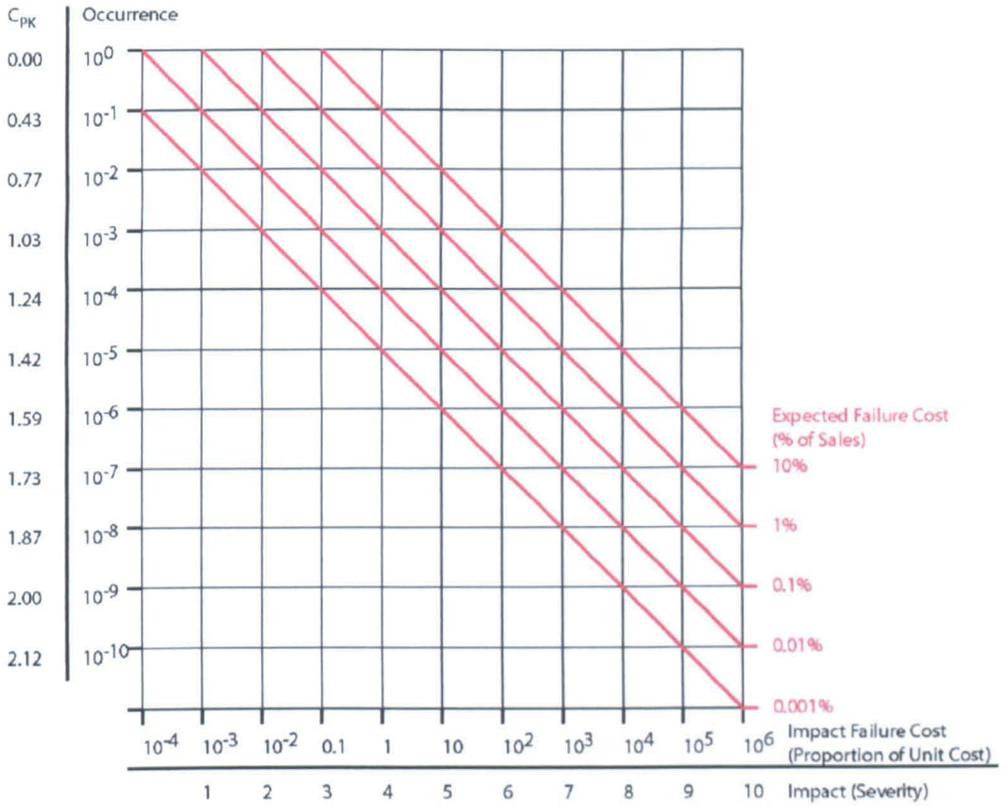
Impact (Severity)	Characteristics	Cost (% of product)
1	Component Failure (found before/at 1 <sup>st</sup> assembly stage)	0.001
2	Failure in Subassembly	0.01
3	Failure at Final Assembly	0.1
4	Scrap Unit or Customer Reject (OE Return)	1
5	Warranty Return	10
6	Warranty Return, Consequential Damage	100
7	Breach of Statutory or Regulatory Requirements	1000
8	Potentially Hazardous Failure	10 000
9	Hazardous Failure – Some Control Possible	100 000
10	Serious Hazardous Failure – No Control	1 000 000

Figure 4-18 Impact (Severity) Ratings Used by eCA

#### 4.16 The cost of a defect

The scale introduced above give an indication of the likely cost of a single defect should it occur, however the likely total cost of a defect to a company is also dependent upon its rate of occurrence. The average cost to the manufacturer arising from a particular type of fault is simply the probability of its occurrence multiplied by the cost when it does occur. This relationship may readily be represented in the form of a quality cost

map as shown in Figure 4-19. The logarithmic axes of Occurrence (or  $C_{pk}$  on the left hand scale) versus Impact (Severity) (or failure cost) mean that points of equal expected cost (“Isocosts”) are simply diagonals on the graph. It is thus straightforward to read the cost of failure of a characteristic from the graph. Thus, for example, a fault which occurs at a rate of 10ppm which has consequences with a severity rating of 6 will have an average quality cost of 0.1% of the product cost.



**Figure 4-19 Cost Mapping for Occurrence and Impact (Severity)**

Alternatively, this may be written as:

$$C_o = O \times 10^{I-4}$$

where  $C_o$  is the average quality cost arising for a fault,

$O$  is the probability of occurrence of the fault, which may be derived from  $C_{pk}$  as discussed in section 1

and  $I$  is the impact (severity) rating of a failure to meet the specification

## 4.17 Quality Cost Summary

We may estimate the quality costs incurred due to imperfect designs and processes through the use of a modelling technique which models the production scheme as a series of discrete processes. Each individual manufacturing process has the potential to introduce a defect whilst each test process may detect or miss the previously introduced defects, such a scheme is illustrated in Figure 4-20.

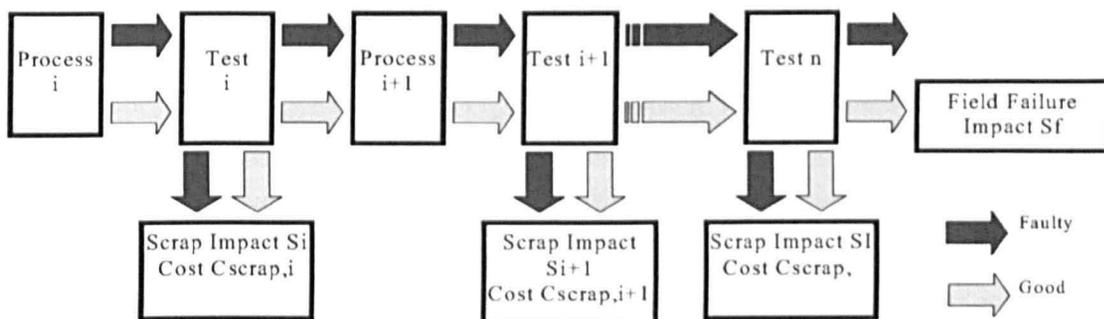


Figure 4-20 Manufacturing and Test Cost Model

At each stage we can estimate the potential costs based on the probabilities of defect occurrence and test error this may be calculated for a production scheme such as that illustrated in Figure 4-20 as shown below:

$$TS1(1-PH(TS1))(F0)*10S1*C$$

Gives the cost of scrap at this stage

$$PI(TS1)*10S1*C$$

Gives the cost of scrapping good circuits at this stage

$$(1-PH(TS2))(E(II)TS1)*10S2*C+(1-PH(TS2)) (1-PH(TS3))(E(II)TS2)*10S3*C+(1-PH(TS2)) (1-PH(TS3))(1-PH(TS4))(E(II)TS3)*10S4*C+(1-PH(TS2)) (1-PH(TS3)) (1-PH(TS4)) (1-PH(TS5))(E(II)TS3)*10S5*C+PH(TS5)(E(II)TS3)*10SF*C$$

Gives the total cost of test failure at this stage (i.e. for existing faults which may be missed by subsequent stages)

This modelling technique may be modified to included the information gained during the functional analysis stage and hence we may estimate the incurred costs based upon the probabilities of defect occurrence due to all of the main influences upon an electronic system. This is done in the final stage of the eCA process by the completion of a conformance matrix. The conformance matrix is used to display and summarise the information generated by each of the eCA analysis modules. An example matrix is

shown in Figure 4-21 and a key to what should be entered in each cell is given in Figure 4-23. The greyed out areas indicate cells which should be left empty, whilst those shown in red highlight areas of concern. The conformance matrix is simple to complete and as would be expected is split into three distinct segments each of which may be completed as the appropriate analysis module has been applied to a circuit or system. The first section of the conformance matrix contains details of the functional performance of the circuit and requires entry of either  $C_{PK}$  or DPMO together with the associated Impact (Severity) for each performance metric. The second section of the conformance matrix holds the data generated during the manufacturing capability analysis of the circuit or system. The completion of this section is dependent upon the form of performance analysis carried out and the matrix must currently be customised by hand to suit the task at hand. Once customised the section should be organised as a hierarchy detailing the effects of each analysed potential defect upon each performance measure. The third and final section of the conformability matrix holds the data generated by the *eCA* test capability analysis module, the data should be entered in the form of defect occurrence rates (DPMO) and a representative  $C_{PK}$  value will be displayed. The test section of the matrix is split into two sections one covering Type I defects and II errors resulting purely parametric variation and the other covering Type II errors resulting from manufacturing defects. Additionally a summary matrix (Figure 4-22) is produced automatically using the data stored in the main matrix; this gives a more general picture of the conformance of the product to specification and the overall levels of manufacturing and test capability. The table details the total defect rates for all three aspects of the design analysed and the associated relative capability levels calculated using this total defect occurrence rate figure; also displayed is the total estimated cost of quality associated with ensuring conformance to specification for the system or product. Along side these defect occurrence rates and quality costs produced using the *eCA* analysis framework an estimate of the quality costs and total defect rates that would be experienced should a Six Sigma process be achieved is also displayed.

Performance Metric	Defect	Conformance Area															
		Functional				Manufacture				Test (Type I)				Test (Type II)			
		Cpk	DPMO	Impact	Cost (%)	Cpk	DPMO	Impact	Cost (%)	Cpk	PPM	Impact	Cost (%)	Cpk	PPM	Impact	Cost (%)
Metric 1	NA																
Metric 2	NA																
Metric 3	NA																
Metric 4	NA																
Metric 1	Defect a																
Metric 2	Defect a																
Metric 3	Defect a																
Metric 4	Defect a																
Metric 1	Defect b																
Metric 2	Defect b																
Metric 3	Defect b																
Metric 4	Defect b																
Metric 1	Defect x																
Metric 2	Defect x																
Metric 3	Defect x																
Metric 4	Defect x																

Figure 4-21 Example Conformance Matrix

Summary Table by Single Area					
	Conformance Area				
	Functional	Manufacturing	Test (Type I)	Test (Type II)	Test (ALL)
Total DPMO / PPM					
Representative Capability					
Total Associated Cost (%)					

Cumulative Summary Table						
	Conformance Area					6 Worst Case
	Functional	Manufacturing	Test (Type I)	Test (Type II)	Test (ALL)	
Total DPMO / PPM						
Representative Capability						
Total Associated Cost (%)						

Cost Summary Table		
	Current	6 Worst Case
Unit Cost (£ to produce)		
Quality Cost per unit (£)		
Quality Cost per 1,000,000 units (£)		
Excess Quality Cost (£)		

Figure 4-22 Conformance Matrix Summary

Performance Metric	Defect
The measure used to determine the performance of the circuit or system	The manufacture induced fault in the circuit or system e.g. a short or open

Conformance Area			
Functional			
Cpk	DPMO	Impact	Cost (%)
The capability of the circuit or system to conform to its requirements in the indicated performance area	The number of defects per million opportunities associated with the current capability level	The Impact (Severity) associated with a failure to conform to the specification for the indicated performance measure	The incurred cost due to incapability and the associated Impact

Manufacture			
Cpk	DPMO	Impact	Cost (%)
The capability of the manufacturing process with respect to a particular potential defect	The number of defects per million opportunities associated with the current capability level	The Impact (Severity) associated with the production of the current defect	The incurred cost due to incapability and the associated Impact

Test (Type I)			
Cpk	PPM	Impact	Cost (%)
The capability of the test process with respect to the current performance metric and the occurrence of Type I test errors	The number of defects expressed in parts per million associated with the current capability level	The Impact (Severity) associated with the occurrence of a test error	The incurred cost due to incapability and the associated Impact

Test (Type II)			
Cpk	PPM	Impact	Cost (%)
The capability of the test process with respect to the current performance metric, associated manufacturing defect and the occurrence of Type II test errors	The number of defects expressed in parts per million associated with the current capability level	The Impact (Severity) associated with the occurrence of a test error	The incurred cost due to incapability and the associated Impact

Figure 4-23 Key to the Conformance Matrix

### 4.18 Summary

This chapter has introduced the concepts and methodologies employed by electronics conformability analysis for the estimation of quality costs associated with the CTQ aspects of an electronic system. The chapter has described the three elements of the methodology each of which addresses one of the major potential sources of quality costs associated with an electronic system. The methodology addresses the same issues as CA allowing the ‘Voice of the Process’ to be expressed for electronic products.

## **5 Process Characterisation**

This chapter introduces and describes a key element of the *eCA* tool set, Process Characterisation. The purpose of process characterisation is to provide key information regarding the performance of a process. Often this information will not only be process specific but also product specific.

### **5.1 What Is a Process?**

By necessity the first stage in any process characterisation must be to identify the processes of interest, before we may do this we must first define what a process is; the Cambridge English dictionary provides the following definitions of a process:

- A series of actions or events that are part of a system or a continuing development
- A series of actions that are done to achieve a particular result

With reference to electronics systems we may interpret these definitions in two ways; firstly, we may define a process as a single production stage making up the manufacturing route of a given product. Secondly, we may define a process as an operational function of an electronic product, for example consider that one of the processes carried out by a filter is to reject the undesired frequency components of the signal passed to it.

### **5.2 Process Capability Analysis**

Process Capability Analysis (PCA) is a popular form of process characterisation; it is a simple statistical technique which defines the ability of a process to meet its specification as a single number. This metric is derived from the relationship between the inherent variability of the process referenced to the specification limits associated with the process. This concept is illustrated by the following illustrations.

### 5.2.1 Example 1 : A Capable Process

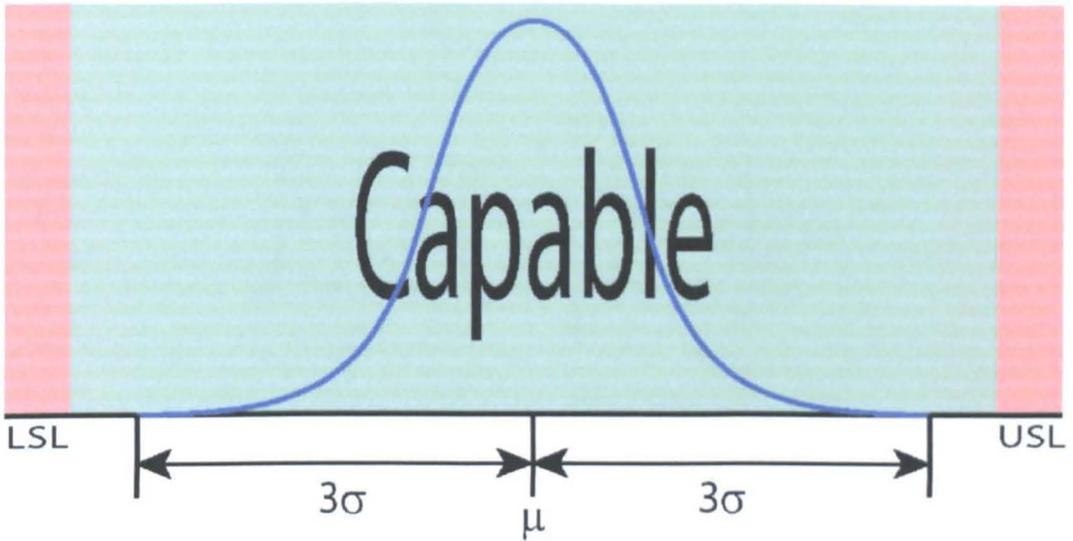


Figure 5-1 A Capable Process

If a process is capable then we can observe a situation similar to that shown in Figure 5-1, the diagram shows a process spread (generally this is measured from  $+3\sigma$  to  $-3\sigma$ ) which is well within the Upper (USL) and Lower (LSL) specification limits. This is a desirable situation for a number of reasons including the following:

- As the specification limits are well outside the normal range of the process spread there will be few if any process failures.
- The specification limits could be reduced resulting in a product with a tighter and hence more desirable specification. As a result of this a company may be able to charge more for a product. For example consider the tolerance and price bands associated with common passive electronic components such as resistors and capacitors.
- It may be possible to reduce costs by using cheaper materials and yet still be within the range defined by the specification limits.

### 5.2.2 Example 2: A 'Just' Capable Process

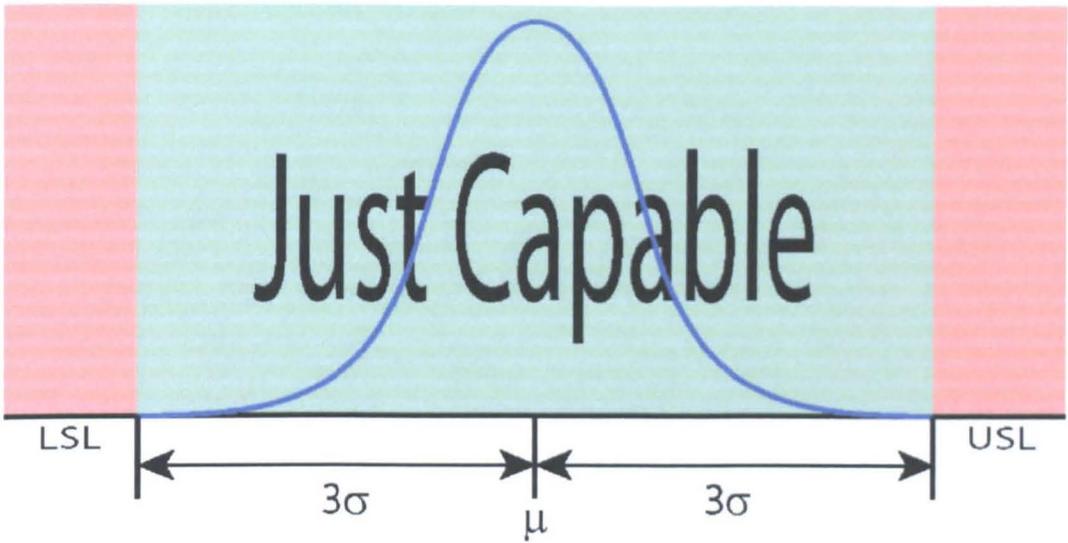


Figure 5-2 A 'Just' Capable Process

A process which is only just capable will have similar characteristics to those illustrated in Figure 5-2. From this frequency curve it may be observed that the process specification limits are in line with or only slightly greater than the extent of the ( $6\sigma$ ) process spread. Although the process represented by this frequency curve is currently process capable any additional variation will cause the process to exceed its specification limits. Such variation may be caused by any source including external influences such as environmental factors or internal influences such a change in the materials or devices being processed. In this situation careful consideration must be given to the process and its suitability for use without additional monitoring and control or modification.

### 5.2.3 Example 3: An Incapable Process

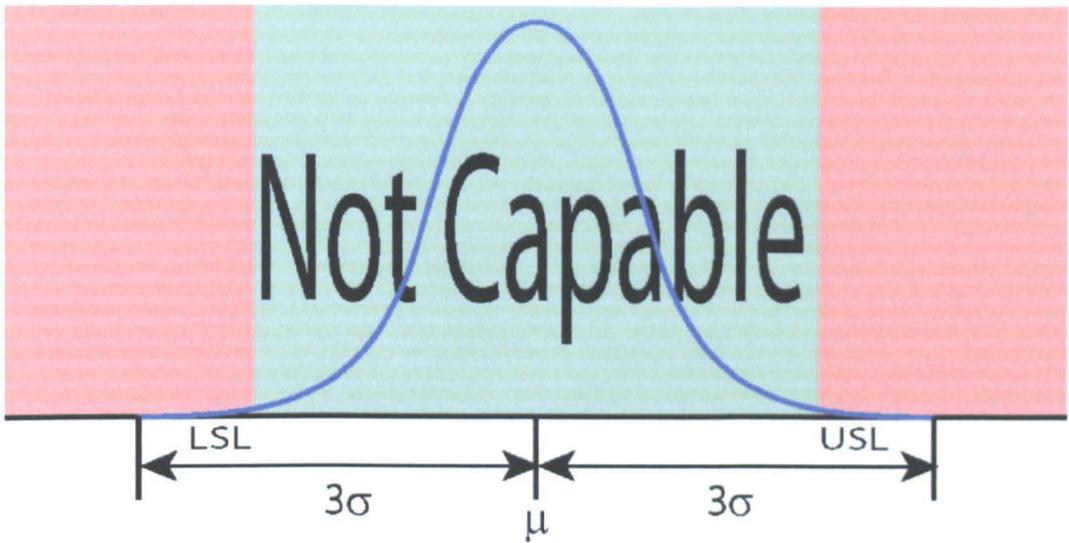


Figure 5-3 An Incapable Process

An incapable process such as that shown in Figure 5-3 occurs whenever the process spread defined as the distance from the process mean to  $\pm 3\sigma$  is greater than the distance between the specification limits ( $LSL$  &  $USL$ ), hence the process will produce out of specification results wherever the process mean ( $\mu$ ) is located. Alternatively an incapable process may result from a process which is poorly centred such as that shown below in Figure 5-1.

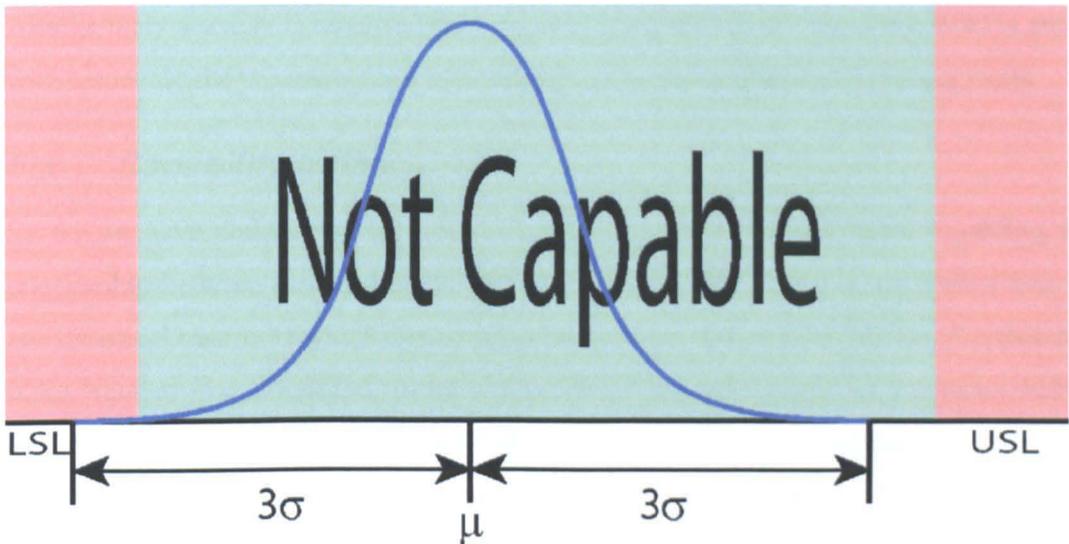


Figure 5-4 An Incapable Process Due to Poor Process Centring

## 5.2.4 Reasons for Poor Capability

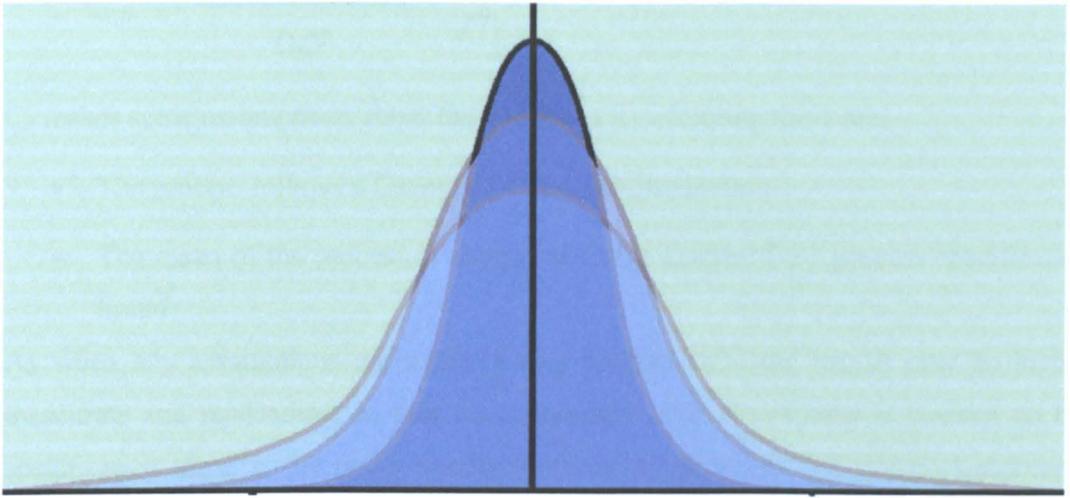


Figure 5-5 Illustration of the Effect of Standard Deviation on Process Spread

A Process may be incapable for either one or a combination of two reasons:

- The process spread is too large (i.e. the standard deviation is too great)
- The process limits are too close together for the process
- The process is poorly centred within the specification limits

Hence we may deduce that a process is incapable if the process spread is large with respect to the process specification limits referenced against the process mean. Alternatively we may determine that a process is capable if the process spread is small with respect to the process specification limits, referenced against the process mean.

## 5.3 Capability Indices

So far we have defined the capability of a process only in loose terms regarding the relationship between process spread and process specification limits, capability indices are statistical measures which define this relationship in numerical terms. A capability index number is a simplified measure describing the performance of a process with a single number and hence they cannot completely describe a process however when used correctly they do provide a good indication of process performance.

### 5.3.1 $C_p$

The most basic capability index,  $C_p$ , shown in equation 7 is the ratio of process specification to process spread [B93] which is defined as six standard deviations ( $6\sigma$ ), the equation for this index is shown in equation 7.

$$C_P = \frac{USL - LSL}{6\sigma} \quad (7)$$

$C_P$  makes some assumptions about the process it is describing these are:

- The process follows a Gaussian or Normal distribution
- The mean of the process is aligned with the centre of the process specification limits

As when any assumptions are made if they are not valid the results may be highly inaccurate and misleading, in fact the assumption that the process is centred on the specification mean is the major weakness of the  $C_P$  index as few practical processes have this attribute.

### 5.3.2 $C_{PK}$

In order to combat the major weakness of the  $C_P$  index  $C_{PK}$  (equation 8) was developed.

$$C_{PK} = \min \left| \frac{USL - \mu}{3\sigma}, \frac{\mu - LSL}{3\sigma} \right| \quad (8)$$

$C_{PK}$  considers where the process mean is located relative to the specification limits, comparing the process mean,  $\mu$ , to the specification limits (USL & LSL) relative to the process spread (in this case process spread is  $3\sigma$  as we have effectively split the distribution around the mean,  $\mu$ ) and taking the worst case scenario as the result.  $C_{PK}$  effectively computes  $C_P$  with compensation for non-centred processes, in fact if the process mean is centred then  $C_{PK}=C_P$ , this does however mean that, like  $C_P$ ,  $C_{PK}$  assumes that a process may be modelled by a Gaussian or Normal distribution.

$C_{PK}$  does have one potential disadvantage when compared to process sigma in that it effectively only consider half of the potential failures associated with a process, however as it is currently the metric of choice for many organisation it is considered that the benefits of this popularity outweigh this potential pitfall.

## 5.4 *Process Distribution*

As we have discussed both  $C_P$  and  $C_{PK}$  make the assumption that the process distribution is normal or Gaussian in form, although in many cases this may be a valid assumption when it is not the capability calculations may be misleading [B94;B95].

### **5.4.1 Process Data**

Before we can provide a description or even a diagram of a process distribution data must be collected about the performance of the process in question, the data collected should be in the form of a set of  $n$  samples of process output this is known as frequency data. For example given a process which produces pencils we may be interested in the capability of the process to produce pencils of length  $l$  in that case we would measure the actual length of  $n$  pencils produced and record this data as a list of lengths.

### **5.4.2 Transformation**

One possible option when we need to estimate the capability of a process which does not follow the normal distribution is to use a transformation which will effectively convert the data into a normal distribution. This can be an effective technique if somewhat computationally intensive however, some distributions cannot be transformed into a normal form and as such we may not calculate process capability.

### **5.4.3 Curve Fitting**

A second option when estimating the capability of a non-normal process is to approximate the data by using a suitable frequency curve. This can then be used to make estimations of points which are equivalent to the standard deviation of a normal distribution. Again this process is computationally intensive however it is also more flexible than the transformation method as most distributions may be modelled using a frequency curve. This technique also leads to better visualisation as an engineer is able to directly examine the relationship between the original data and the frequency curve, and does not have to analyse the mathematical relationship as would be the case when using the transformation method.

### **5.4.4 Frequency Curves**

Several families of frequency curves provide us with suitable equations for modelling non-normal data, of particular interest are Johnson Curves and Pearson Curves both of [B96;B97;B98;B97;B99] which provide flexible systems which may be used to model frequency data. For this work the Pearson family is used for its slightly greater flexibility and easier application than Johnson curves.

### 5.4.5 The Method of Moments

The first requirement when fitting a curve to a set of data is that we must provide a basic description of the data in mathematical terms, the method of moments provides us with a technique which we may use to do this.

The definition of the  $r^{\text{th}}$  moment about the origin of the discrete random variable  $X$  is:

$$\mu'_r = \sum_x x^r f(x) \quad (9)$$

So for a sample of size  $n$  consisting of elements  $x_1, x_2, x_3 \dots x_n$  we may use the following formula to calculate the  $r^{\text{th}}$  non-central moment:

$$\mu'_r = \frac{1}{n} \sum_{i=1}^n x_i^r \quad (10)$$

From equation 10 we see that the first moment  $\mu_1$  is actually the sample mean.

Moments about the sample mean, known as central moments, may also be defined and these are connected to the non-central moments by the following formulae:

$$\mu_1 = \mu_1' \quad (11)$$

$$\mu_2 = \mu_2' - (\mu_1')^2 \quad (12)$$

$$\mu_3 = \mu_3' - 3\mu_2' \mu_1' + 2(\mu_1')^3 \quad (13)$$

$$\mu_4 = \mu_4' - 4\mu_3' \mu_1' + 6\mu_2' (\mu_1')^2 - 3(\mu_1')^4 \quad (14)$$

From these formulae describing the relationship between the first four central and non-central moments we can see that as the first moment  $\mu_1$  is the sample mean the second moment  $\mu_2$  is equivalent to the sample variance  $\sigma^2$ . The third and fourth moments are used in the following equations for the calculation sample skew and kurtosis.

$$\sqrt{B_1} = \frac{\mu_3}{(\mu_2)^{\frac{3}{2}}} \quad (15)$$

Equation 15 shows the calculation used for the measurement of sample skew, whilst equation 16 shows the calculation for sample kurtosis.

$$B_2 = \frac{\mu_4}{\mu_2^2} \quad (16)$$

Using these equations we are now able to provide a mathematical description of the shape of a sample in terms of:

- Sample mean
- Sample variance
- Sample skew
- Sample kurtosis

Taken together these measures provide us with a general view of the shape and form the process distribution takes.

## 5.5 Pearson Curves

The Pearson system of frequency curves (also known as probability density functions), defined by Karl Pearson, consists of a family of 12 curves [B100] derived from a single differential equation (equation 17), the terms of which are dependent upon the first four central moments of the sample data. The Pearson probability density function  $f(x)$  is described by the following differential equation:

$$\frac{1}{f(x)} \frac{df}{dx} = \frac{s + x}{t_0 + t_1x + t_2x^2} \quad (17)$$

The constants  $t_0$ ,  $t_1$ ,  $t_2$  and  $s$  may be calculated from the first four central moments of the process distribution using the following formulae:

$$d = 2(5B_2 - 6B_1 - 9) \quad (18)$$

$$s = \frac{\sqrt{m_2}(B_2 + 3)\sqrt{B_1}}{d} \quad (19)$$

$$t_0 = \frac{m_2(4B_2 - 3B_1)}{d} \quad (20)$$

$$t_1 = s \quad (21)$$

$$t_2 = \frac{(2B_2 - 3B_1 - 6)}{d} \quad (22)$$

The 12 curves derived from the single differential equation may be distinguished by the roots of the quadratic equation in the denominator of the differential equation. Pearson split the curves into two groups, the main group consisting of three curves and a sub group known as the transitional types consisting of the other nine curves.

Pearson also defined the Pearson Criterion  $k$  which may be used to distinguish between the curves:

$$K = \frac{t_1^2}{(4t_0t_2)} \quad (23)$$

For the purposes of this work we will only consider the three main curves, Types I, IV and VI, which may be distinguished by the conditions listed in the following table:

$K < 0$	Type I
$0 < K < 1$	Type IV
$K > 1$	Type VI

Figure 5-6 Distinguishing Conditions (Using  $K$ ) for the Three Main Curves

### 5.5.1 Type I

The Type I curve is defined for values of  $K$  less than zero indicating that the roots of the quadratic in the denominator of 17 are real and have opposite signs. The specific form of the curve may be derived as follows

First we find the roots of the quadratic and then split the equation into a partial fraction to give:

$$\frac{1}{f(x)} \frac{df}{dx} = \frac{U}{r1+x} - \frac{V}{r2-x} \quad (24)$$

Now integrating 24 we find the following:

$$\ln f(x) = \int \frac{U}{r1+x} - \frac{V}{r2-x} dx \quad (25)$$

$$\ln f(x) = U \ln(r1+x) - V \ln(r2-x) + C \quad (26)$$

Where  $C$  is the arbitrary constant of integration hence we can write:

$$\ln f(x) = U \ln k(r1+x) - V \ln(r2-x) \quad (27)$$

Now we can write 27 in the following form:

$$f(x) = f_0(r1+x)^U (r2-x)^V \quad (28)$$

Adjusting 28 so that the origin is the true origin and not the mean of the curve we find:

$$f(x) = fo(r1 - \mu_1' + x)^U (r2 - \mu_1' - x)^V \quad (29)$$

Where  $fo$  is a compensating factor which allows us to adjust the area under the curve, in the case of a probability distribution  $fo$  I adjusted to give an area of one.

### 5.5.2 Type II

The Type II curve is defined for values of  $K$  in the range of zero to one and hence the denominator of 17 has complex roots. To find the form of the equation for the Type II curve we will use substitution to allow the integration as shown below.

For the denominator the procedure is as follows:

$$t_2x^2 + t_1x + t_0 \quad (30)$$

$$t_2 \left( x^2 + \frac{t_1}{t_2}x + \frac{t_0}{t_2} \right) \quad (31)$$

$$t_2 \left( \left[ x - \frac{\left( \frac{t_1}{t_2} \right)}{2} \right]^2 + \frac{t_0}{t_2} - \left[ \frac{\left( \frac{t_1}{t_2} \right)}{2} \right]^2 \right) \quad (32)$$

$$t_2 \left( \left[ x - \frac{t_1}{2t_2} \right]^2 + \left( \frac{t_0}{t_2} \right) - \frac{t_1^2}{4t_2^2} \right) \quad (33)$$

Now let  $X = x + \frac{t_1}{2t_2}$  &  $A^2 = \frac{t_0}{t_2} - \frac{t_1^2}{4t_2^2}$

Hence Denominator is reduced to

$$t_2(X^2 + A^2) \quad (34)$$

Also let  $C = s - \frac{t_1}{2t_2}$

Hence the numerator may be written

$$X + C \quad (35)$$

Now we may substitute 34 & 35 into 17 which gives the following:

$$\ln f(x) = \int \frac{X+C}{t_2(X^2+A^2)} dX \quad (36)$$

$$\ln f(x) = \int \frac{X}{t_2(X^2+A^2)} dX + \int \frac{C}{t_2(X^2+A^2)} dX \quad (37)$$

Now given

$$\frac{d}{dx} \ln f(x) = \frac{f'(x)}{f(x)} \quad (38)$$

$$\frac{d}{dx} \tan^{-1}(x) = \frac{1}{1+x^2} \quad (39)$$

We see may see that

$$\frac{d}{dx} \tan^{-1}\left(\frac{x}{I}\right) = \frac{I}{x^2+I^2} \quad (40)$$

so using 40 we may rewrite 37 as

$$\ln f(x) = \int \frac{2X}{2t_2(X^2+A^2)} dX + \int \frac{CA}{At_2(X^2+A^2)} dX \quad (41)$$

$$\ln f(x) = \frac{1}{2t_2} \int \frac{2X}{(X^2+A^2)} dX + \frac{C}{At_2} \int \frac{A}{(X^2+A^2)} dX \quad (42)$$

which we may integrate to give (Where k is the arbitrary constant of integration)

$$\ln f(x) = \frac{1}{2t_2} \ln(X^2+A^2) + \frac{C}{At_2} \tan^{-1}\left(\frac{X}{A}\right) + k \quad (43)$$

This may be rewritten as in 44 where  $f_0$  is the constant supplying a scaling factor to allow us to adjust the area under the curve to the correct proportions.

$$f(x) = f_0(X^2+A^2)^{\frac{1}{2t_2}} e^{\left(\frac{C}{At_2}\right) \tan^{-1}\left(\frac{X}{A}\right)} \quad (44)$$

44 shows the equation formatted so that the origin of the curve is the sample mean, this may be compensated for by subtracting the first moment,  $\mu$ , from the values of x passed to the equation.

### 5.5.3 Type VI

The type VI curve is valid for values of  $K$  greater than one and hence the roots of the denominator of 17 are both real and have the same sign, hence we may derive the curve in the following way, first we split 17 to give partial fractions:

$$\frac{d}{dx} \ln f(x) = \frac{U}{r1+x} + \frac{V}{r2+x} \quad (45)$$

We may now integrate 45 to give:

$$\ln f(x) = \int \frac{U}{r1+x} + \frac{V}{r2+x} dx \quad (46)$$

$$\ln f(x) = U \ln(r1+x) + V \ln(r2+x) + k \quad (47)$$

Which may be rewritten as shown in 48 where the sample mean is the origin of the curve.

$$f(x) = fo(r1+x)^U (r2+x)^V \quad (48)$$

As with the Type I and II curves the equation may be adjusted so the that the origin is shifted to the true origin from the sample mean, in that case 48 may be rewritten as seen in 49.

$$f(x) = fo(r1 - \mu'_1 + x)^U (r2 - \mu'_1 + x)^V \quad (49)$$

## 5.6 Application of an Arbitrary Distribution In Capability Analysis

As discussed in section 5.4.3 an arbitrary probability distribution may be used in the calculation of process capability, we may achieve this by selecting points on the arbitrary distribution which are equivalent to the  $3\sigma$  points of a normal distribution and using the selected points in the capability calculation.

### 5.6.1 Selection of points equivalent to $3\sigma$

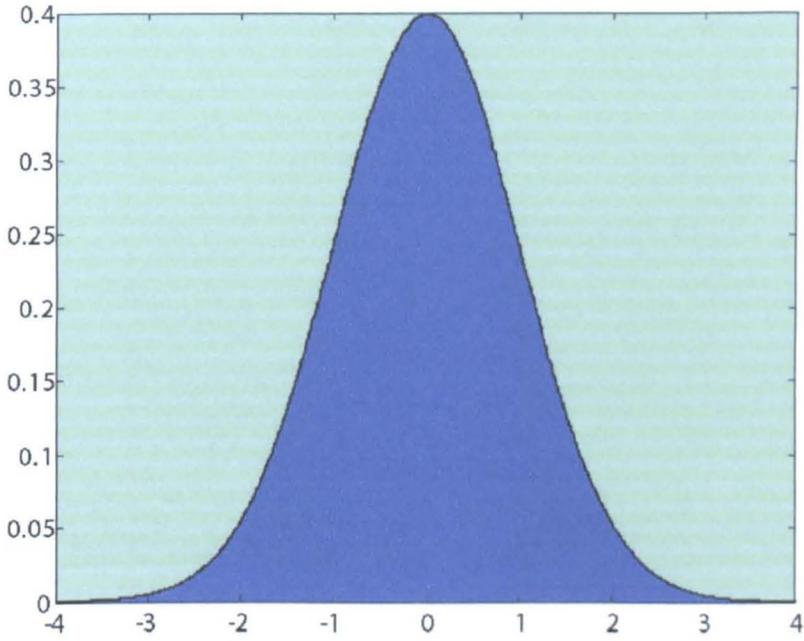


Figure 5-7 Standard Normal Distribution  $N(0,1)$

Given a standard normal distribution we know that the standard deviation,  $\sigma$ , is one hence the upper and lower three sigma,  $3\sigma$ , points lie at +3 and -3 respectively on the x-axis. Using this information regarding the location of the  $3\sigma$  points we may find the probability of a point lying in either of the tails of the distribution outside of the  $3\sigma$  points which to 9 decimal places is 0.001349898. Hence given a cumulative normal distribution we may locate the positions of the upper and lower  $3\sigma$  points by finding the values on the x-axis where the probability is equal to 0.001349898 for the lower  $3\sigma$  point and 0.998650102 for the upper point.

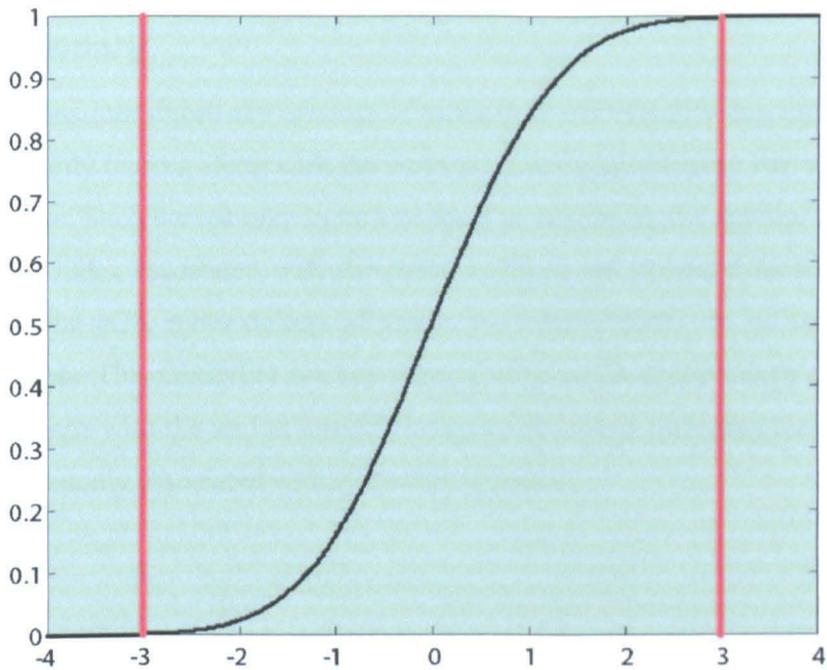


Figure 5-8 Cumulative Normal Distribution

This technique leads us to write a new definition of  $C_{PK}$

$$C_{PK} = \min \left| \frac{USL - \mu'_1}{x_{0.998650102} - \mu'_1}, \frac{\mu'_1 - LSL}{\mu'_1 - x_{0.001349898}} \right| \quad (50)$$

where  $\mu'_1$  is the first moment of the distribution and  $x_{0.998650102}$  and  $x_{0.001349898}$  are the percentiles of the distribution which equate to the  $3\sigma$  points. Examining this new definition of  $C_{PK}$  we see that it is in fact distribution independent and that the only requirements for its application to a process distribution are, firstly, that the first moment of the distribution may be identified and secondly, that the  $x_{0.998650102}$  and  $x_{0.001349898}$  percentiles are located. Given that we may meet these conditions through the use of an arbitrary frequency curve fitted to a process distribution we may now calculate the capability of any process regardless of the shape and form of its distribution.

## **5.7 Summary**

This chapter has introduced the concept of process characterisation through the use of process capability indices along with the concept of using an arbitrary curve to describe a given process. Such curves may in turn be used to determine the appropriate value of the capability index associated with the process. These are powerful tools which play key roles in the *eCA* methodology allowing a common metric to be applied to an arbitrary process. This flexibility is a key strength of the *eCA* methodology allowing the technique to cope with the widest possible range of processes including the non-normal processes commonly associated with electronic systems.

## **6 Assessment of Contributing Factors**

Using the techniques described in chapter 1 we are able to analyse processes relating to an electronic product and calculate the value of the process capability index  $C_{PK}$  which provides us with an estimate of the ability of the process to conform to its associated specification. Clearly besides knowing the capability of a process to conform to its specification it would also be useful to know the extent of the contribution made by individual process influencing factors. This breakdown of information would allow targeted design improvements to be made based upon data which would complement the engineering 'knowledge' employed by the design team.

### **6.1 Regression Analysis**

Regression analysis uses a range of statistical techniques to examine and model the relationship between two or more variables in a system or process. For example consider a solder paste printing process, the yield of the process is dependent upon a number of factors including:

- The speed of the squeegee
- The squeegee pressure
- The shape of the holes in the mask
- The ambient temperature
- The age of the solder paste

Regression analysis may be used to build a statistical model of the process taking into account these factors, this model could then be used for a number of different purposes ranging from process optimization through to process control.

### **6.2 Simple Linear Regression**

Simple linear regression is possible when the situation exists that only two variables within a system are considered, these are the regressor  $x$  (the system input) and its associated response variable  $y$  (the system output). Simple linear regression assumes that the relationship between  $x$  and  $y$  is linear and hence that it may be represented by a straight line. The implication of this assumption is that the mean value of  $y$  is a linear function of  $x$ , however the observed values of  $y$  do not necessarily lie on the straight line representing this linear relationship. The relationship between  $x$  and  $y$  may be represented by equation (51), where  $\varepsilon$  is an error term explaining any deviation of the

observed value of  $y$  from the linear model,  $\alpha_0$  is the intercept of the line and  $\alpha_1$  the slope.

$$y = \alpha_0 + \alpha_1 x + \varepsilon \quad (51)$$

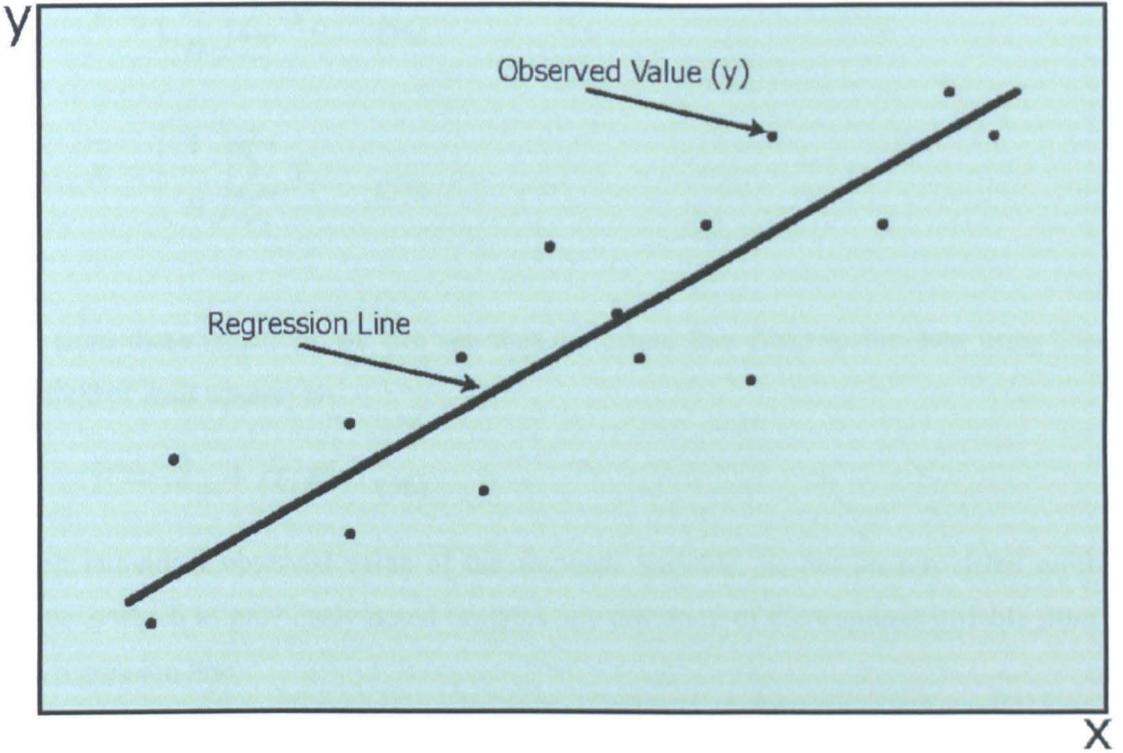


Figure 6-1 An Example of Simple Linear Regression

Simple linear regression may be applied using the least squares fit method developed by Karl Gauss, the method works by minimising the sum of the squares of the vertical deviations of the data points from the regression line to produce a line of best fit. Provided with  $n$  pairs of observations or coordinates  $(x_i, y_i)$  the intercept and slope of the line of best fit may be calculated using the least squares equations shown below.

$$\hat{\alpha}_1 = \frac{\sum_{i=1}^n x_i y_i \frac{\left(\sum_{i=1}^n x_i\right)\left(\sum_{i=1}^n y_i\right)}{n}}{\sum_{i=1}^n x_i^2 - \frac{\left(\sum_{i=1}^n x_i\right)^2}{n}} \quad (52)$$

$$\hat{\alpha}_0 = \bar{y} - \hat{\alpha}_1 \bar{x} \quad (53)$$

Where

$$\bar{y} = \left( \frac{1}{n} \right) \sum_{i=1}^n y_i \quad (54)$$

$$\bar{x} = \left( \frac{1}{n} \right) \sum_{i=1}^n x_i \quad (55)$$

So from these equations we can see that the actual line fitted to the data using the method of least squares is:

$$\hat{y} = \hat{\alpha}_0 + \hat{\alpha}_1 x \quad (56)$$

Each individual observed value of the response variable,  $y_i$ , has an associated error value  $\varepsilon_i$  which as previously noted explains any deviation of the response variable from the regression line.

The significance or goodness of fit of the regression model may be assessed through the application of Analysis of Variance (ANOVA). The ANOVA identity given in equation (57), calculates the total corrected sum of squares ( $S_{yy}$ ) from the regression sum of squares ( $SS_R$ ). This is a measure of the total variability of the regression model around the mean of the observed response and the error sum of squares ( $SS_E$ ) which measures the total deviation of the observed response from the response predicted by the regression model, so the  $S_{yy}$  is a measure of the total variability of the observed response to the predicted response.  $SS_R$  and  $SS_E$  may be calculated as shown in equations (58) and (59) respectively.

$$S_{yy} = SS_R + SS_E \quad (57)$$

$$SS_R = \sum_{i=1}^n (\hat{y}_i - \bar{y})^2 \quad (58)$$

$$SS_E = \sum_{i=1}^n (y_i - \hat{y}_i)^2 \quad (59)$$

Further to this we may calculate the mean square of regression ( $MS_R$ ) and the mean square of error ( $MS_E$ ) using equations (60) and (61) respectively. From these equations we can see that the mean square of error is simply the variance error of the regression, it should be noted that we have only  $n-2$  degrees of freedom as the equations are concerned with the error involved in the prediction of  $y$  from  $x$ .

$$MS_R = \frac{SS_R}{1} \quad (60)$$

$$MS_E = \frac{SS_E}{n-2} \quad (61)$$

$$F_0 = \frac{MS_R}{MS_E} \quad (62)$$

We may now complete the ANOVA for the regression by calculating the F statistic (62) for the regression and comparing this to the appropriate value from the 'f' distribution ( $f_{\alpha,1,n-2}$ ) to ensure that  $F_0$  is larger i.e.  $F_0 > f_{\alpha,1,n-2}$ . This test cannot prove that the regression is valid (if it is a good fit to the data or not) however if we find that  $F_0$  is greater than  $f_{\alpha,1,n-2}$  we may assume that the relationship between  $x$  and  $y$  described in equation (51) is linear however it may be possible to achieve a better regression with a higher order polynomial.

### 6.3 Multiple Linear Regression

In many cases simple linear regression may not be applicable to a system. For example consider again the solder paste printing process where the height of the paste (the response) is dependent upon a number of variables (regressors). In this situation the system may be represented by a relationship such as that shown in equation (63).

$$y = \alpha_0 + \alpha_1 x_1 + \alpha_2 x_2 + \epsilon \quad (63)$$

This is a multiple linear regression model with two regressors ( $x_1$  &  $x_2$ ) and may be represented by a plane in three dimensional space as shown in Figure 6-3. In general multiple linear regression models will have more than two regressors and the model will be similar to than shown in equation (64)

$$y = \alpha_0 + \alpha_1 x_1 + \alpha_2 x_2 + \dots + \alpha_k x_k + \epsilon \quad (64)$$

$y$	$x_1$	$x_2$	...	$x_k$
$y_1$	$x_{11}$	$x_{21}$	...	$x_{k1}$
$y_2$	$x_{12}$	$x_{22}$	...	$x_{k2}$
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
$y_l$	$x_{1l}$	$x_{2l}$	...	$x_{kl}$

Figure 6-2 Example of Multiple Linear Regression Data

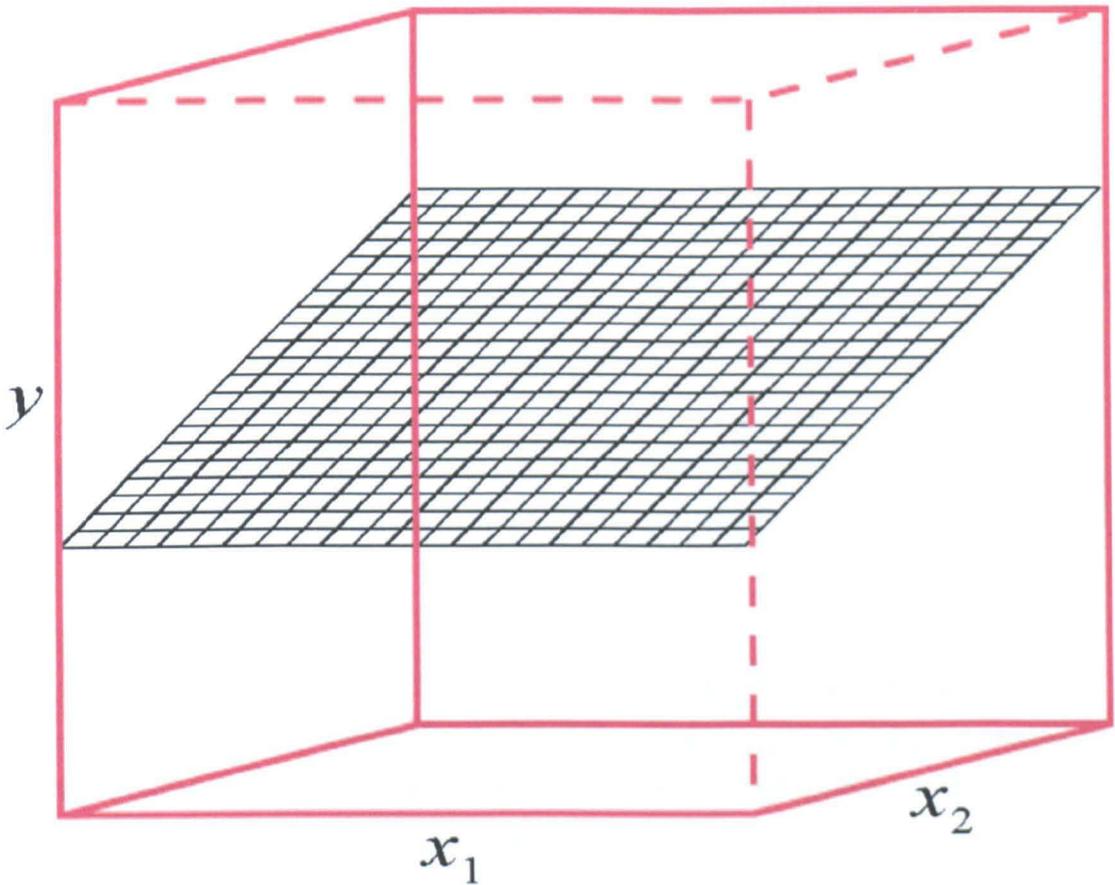


Figure 6-3 An Example of a 2 Variable Multiple Linear Regression Plane

As with simple linear regression we may use Gauss least squares technique to estimate the regression parameters for the regression model shown in (64). Considering the example data shown in Figure 6-2 we see that the regression model may be rewritten as shown in equation (65) such that each term is derived from the collected data.

$$y_i = \alpha_0 + \sum_{j=1}^k \alpha_j x_{ij} + \varepsilon_i \quad \text{for } i=1 \text{ to } l \quad (65)$$

By far the simplest method to fit the regression model is to use a matrix based approach, firstly we may express (65) in matrix form as shown in equation (66) and may be written as in equation (67).

$$\begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_l \end{bmatrix} = \begin{bmatrix} 1 & x_{11} & \cdots & x_{1k} \\ 1 & x_{21} & \cdots & x_{2k} \\ \vdots & \vdots & & \vdots \\ 1 & x_{l1} & \cdots & x_{lk} \end{bmatrix} \begin{bmatrix} \alpha_0 \\ \alpha_1 \\ \vdots \\ \alpha_k \end{bmatrix} + \begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \vdots \\ \varepsilon_k \end{bmatrix} \quad (66)$$

$$Y = X\alpha + \varepsilon \quad (67)$$

now we may solve for  $\hat{\alpha}$  the least squares estimate of  $\alpha$  using the formula shown in equation (68).

$$\hat{\alpha} = (X'X)^{-1} X'Y \quad (68)$$

So the model fitted to the data is

$$\hat{y} = X\hat{\alpha} \quad (69)$$

From this we may calculate the residual ( $r$ ), that is the difference between the fitted model and the observed value, this is illustrated in equation (70)

$$r = y - \hat{y} \quad (70)$$

As with simple linear regression we may calculate  $SS_E$  through the application of equation (59), however in order to calculate  $MS_E$  we must apply the following equation where  $n$  and  $p$  are derived from the size of  $X$  which is  $(n * p)$  this accounts for the multidimensional nature of this regression.

$$MS_E = \frac{SS_E}{n - p} \quad (71)$$

As with  $SS_E$ ,  $SS_R$  may be calculated as for simple linear regression through the application of equation (58), and we may also apply equation (57) to calculate the total sum of squares. Again as with simple linear regression we may apply these results using equation (62) to a test of significance where if  $F_0 > f_{\alpha, k, n-p}$  is satisfied we may assume that a linear relationship exists between the response variable and the regressors or a

subset of the regressors. Further to this we may calculate the coefficient of multiple determination  $R^2$  which gives an indication of the proportion of variation in the response variable that is explained by the model.

$$R^2 = \frac{SS_R}{S_{yy}} = 1 - \frac{SS_E}{S_{yy}} \quad (72)$$

So  $R^2$  is measuring the variability of the residual values around the regression line relative to the total overall variability, hence the larger the value of  $R^2$  the better the regression model. As  $R^2$  is a ratio it may take any value from 0 to 1 and a value of 1 or close to 1 would indicate that the regression model accounts for all or the majority of variability in the observed data.

#### **6.4 Limitations of Linear Regression**

The most obvious limitation of linear regression is the assumption that the relationships between the variables are linear, however the technique is reasonably robust and is not effected by small deviations from linearity. The number of variables chosen to be used in the model may also be significant, generally to produce a good regression about 20 times as many samples as variables are required otherwise the regression will be poor, and an alternative set of observations of the original function (a different sample of the population) may produce a different regression model.

#### **6.5 Capability Breakdown**

Using the regression techniques described in the previous section we may calculate the influence individual circuit parameters have over the various performance measures. We may then use this information to produce a 'capability breakdown'. This section describes the process of producing a capability breakdown and its mathematical basis. To begin we must first define the behaviour of a process with respect to its controlling factors, this may be written as shown in equation (73) where a process,  $P_i$  is dependent on the contributing factor,  $C_j$ .

$$P_i = f_i(C_1, C_2, \dots, C_m) \quad (73)$$

If we assume that the variation in controlling factors is small compared to their nominal value and that the relationship between controlling factors and process performance is continuous, then the relationship shown in equation (73) may be approximated by a linear response surface model, which may be calculated by applying multiple linear

regression through the application of a least squares fit of process performance to controlling factor values, as described in the previous section.

Thus, within a local area of the operating point, the variation in process performance  $\Delta P_i$  resulting from variation in controlling factors,  $\Delta C_j$  may be written as shown in equation (74).

$$\Delta P_i = \sum_{j=1}^m \frac{\partial f_i}{\partial C_j} \Delta C_j \quad (74)$$

Alternatively equation (74) may be represented in matrix form as shown below.

$$\begin{bmatrix} \Delta P_1 \\ \Delta P_2 \\ \vdots \\ \Delta P_n \end{bmatrix} = \begin{bmatrix} \frac{\partial f_1}{\partial C_1} & \frac{\partial f_1}{\partial C_2} & \dots & \frac{\partial f_1}{\partial C_m} \\ \frac{\partial f_2}{\partial C_1} & \frac{\partial f_2}{\partial C_2} & \dots & \frac{\partial f_2}{\partial C_m} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial f_n}{\partial C_1} & \frac{\partial f_n}{\partial C_2} & \dots & \frac{\partial f_n}{\partial C_m} \end{bmatrix} \begin{bmatrix} \Delta C_1 \\ \Delta C_2 \\ \vdots \\ \Delta C_m \end{bmatrix} \quad (75)$$

Given that the partial derivative of the function,  $\frac{\partial f_i}{\partial C_j}$ , is equivalent to the sensitivity of

the process  $P_i$  to component parameter  $C_j$  we may rewrite equation (74) in the following form

$$\Delta P_i = \sum_{j=1}^m S_{ij} \Delta C_j \quad (76)$$

and now using a multiple linear regression model (also known as a response surface model) which may be calculated based upon a sample of simulation, experimental, or production data for  $C_j$  and  $P_i$  the values of  $S_{ij}$  may be found. In which case equation (75) may be modified using these sensitivities to the following form:

$$\begin{bmatrix} \Delta P_1 \\ \Delta P_2 \\ \vdots \\ \Delta P_n \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots & S_{1m} \\ S_{21} & S_{22} & \cdots & S_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ S_{n1} & S_{n2} & \cdots & S_{nm} \end{bmatrix} \begin{bmatrix} \Delta C_1 \\ \Delta C_2 \\ \vdots \\ \Delta C_m \end{bmatrix} \quad (77)$$

If we now make the assumption that the variation in component parameters is normally distributed with standard deviation  $\sigma C_j$  and that the resulting deviation in performance due to the variation in component parameters is also normal then we modify equation (76) to the following form.

$$\sigma P_i = \sqrt{\sum_{j=1}^m (S_{ij} \sigma C_j)^2} \quad (78)$$

$$C_{pki} = \frac{|\mu_i - NSL_i|}{3\sigma_i} \quad (79)$$

Now given 8 we may write this using equation (78) as

$$C_{pki} = \frac{|\mu_i - NSL_i|}{3\sqrt{\sum_{j=1}^m (S_{ij} \sigma C_j)^2}} \quad (80)$$

Hence the inverse capability ( $1/C_{pk}$ ) for  $P_i, I_b$  may be written as

$$I_i = \frac{3\sqrt{\sum_{j=1}^m (S_{ij} \sigma C_j)^2}}{|\mu_i - NSL_i|} \quad (81)$$

or alternatively this may be summarised as

$$I_i = \sum_{j=1}^N I_{ij} \quad (82)$$

where  $I_{ij}$  is as shown below

$$I_{ij} = \frac{3\sqrt{(S_{ij}\sigma C_j)^2}}{|\mu_i - NSL_i|} \quad (83)$$

However this assumes that the response model explains 100% of the variation of the observed model. This is unlikely to be the case due to non-linear process behaviour, simulation noise and other effects all of which will lead to a less accurate model in. This situation may be compensated for using  $R^2$ , which is effectively a measure of the amount of observed variation explained by the regression model, modifying equation (83) as shown below.

$$I_{ij} = R_i^2 * \frac{3\sqrt{(S_{ij}\sigma C_j)^2}}{|\mu_i - NSL_i|} \quad (84)$$

We may also write an equation for the portion of the capability of  $P_i$  that is not explained by the model,  $I_{iu}$ .

$$I_{iu} = (1 - R_i^2) * \frac{3\sqrt{\sum_{j=1}^m (S_{ij}\sigma C_j)^2}}{|\mu_i - NSL_i|} \quad (85)$$

The larger the value of  $I_i$  (equation (81)) the larger the probability of an out of specification fault relating to performance  $i$  occurring while a large value of  $I_{ij}$  (equation (84)) indicates that component parameter  $j$  makes a large contribution to those faults and should be targeted for further action. A large value of  $I_{iu}$  (equation (85)) indicates that the variation in  $P_i$  is not explained by a linear combination of controlling factor variations, or that key controlling factors influencing the process performance have not been included in the response surface model. It would be possible to extend the response surface model to include polynomial or other functions of controlling factors or products of controlling factors in order to achieve a closer fit to the data and reduce the unexplained element.

We may also note that the inverse capability  $I_i$  is the sum of the explained and unexplained portions of capability as shown in equation (86).

$$I_i = \sum_{j=1}^m I_{ij} + I_{iu} \quad (86)$$

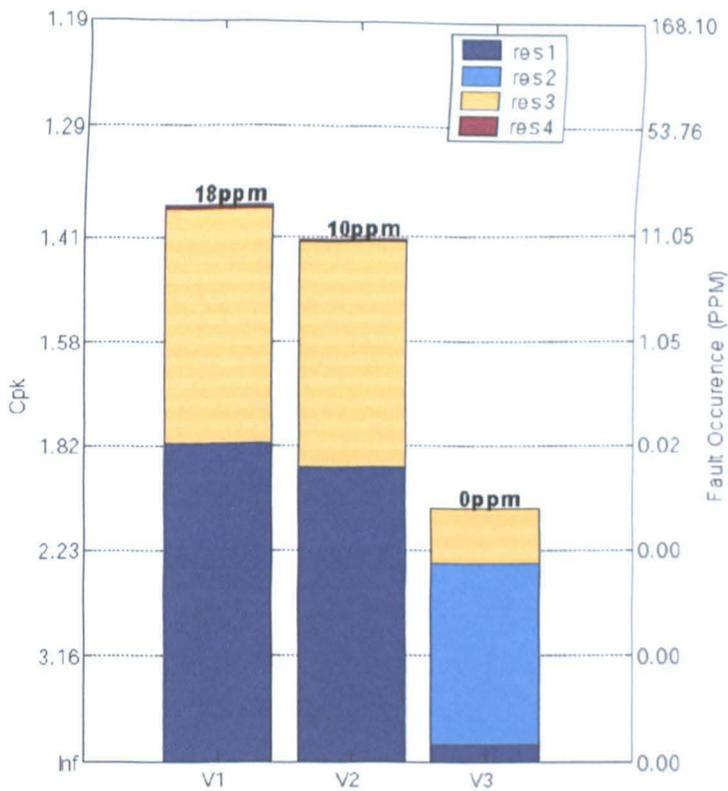
This method of describing the contributions made by individual process parameters to the process as a whole may be further enhanced, in its current form it suffers from the limitation that the relationship between the contribution of an individual element ( $I_{ij}$ ) and the total inverse capability ( $I_i$ ) is not linear. Hence a 50% reduction in the contribution of a single element may not produce a proportional response in the total. This problem may be solved by squaring the inverse capability,  $I_i$ , as seen in equation (87)

$$I_i^2 = \frac{1}{C_{pki}^2} = \sum_{j=1}^m I_{ij}^2 + I_{iu}^2 \quad (87)$$

$$I_i^2 = R_i^2 \frac{9 \sum_{j=1}^m (S_{ij} \sigma C_i)^2}{|\mu - NSL|^2} + (1 - R_i^2) \frac{9 \sum_{j=1}^m (S_{ij} \sigma C_i)^2}{|\mu - NSL|^2} \quad (88)$$

## 6.6 Capability Histograms

Equation (88) embodies critical information for the circuit designer that may conveniently be presented graphically in the form of a histogram. If the histogram is created such that the y axis is proportional to  $1/C_{pk}^2$  the overall height of bar  $i$  represents  $I_i^2$  and the individual elements represent  $I_{ij}^2$  and  $I_{iu}^2$ . In order to better use the resulting histogram the vertical axis maybe with the appropriate values of  $C_{pk}$  and an additional vertical axis labelled with fault occurrence (ppm) may be added as shown below in Figure 6-4.



**Figure 6-4 Explanation of the Capability Histogram**

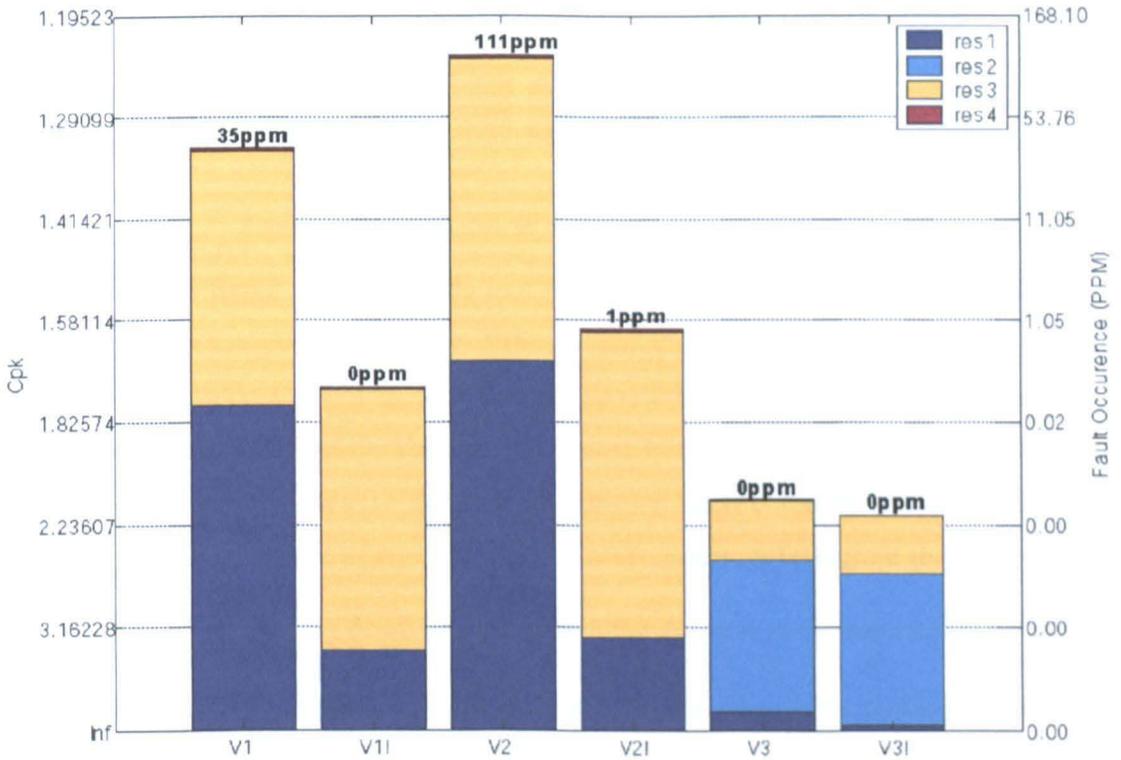
This graphical method of capability analysis has several advantages over more traditional index based methods, firstly as the method plots  $\frac{1}{C_{pk}^2}$  the height of the bar is inversely proportional to the capability of a particular aspect of process performance, hence large bars indicate lower capabilities as can be seen from the scale on the left hand side Y-axis.

Further to this on the right hand side of the histogram an equivalent scale giving an indication of the expected rate of fault occurrence in parts-per-million is presented.

A significant characteristic of this representation is that it is proportional to the tolerance of individual process parameters, hence the effect of changing one or all of the process tolerances by a given amount  $k_j$  may be easily predicted, according to the relationship shown in equation (89).

$$\frac{1}{C_{pk}^2} = \frac{9 \sum_{j=1}^m (s_{ij} \sigma C_i k_j)^2}{|\mu_i - NSL|^2} \quad (89)$$

So due to the squaring term in the equation if a circuit tolerance is multiplied by  $k_j$  the contribution of that component to any performance aspect will be scaled by  $k_j^2$ . For example reducing the tolerance band on a given component by half will have the effect of reducing the contribution that that component makes to each aspect of performance by 4. This effect is best illustrated graphically, consider the histogram shown in Figure 6-5, the bars marked simply  $V_x$  where  $x$  is a number are generated by a Monte Carlo simulation whilst those marked  $V_x!$  show the effect of tolerance scaling, and represent the effect of reducing the tolerance of the component R1 from 10% to 5%. From this representation we can see that this tightening of the tolerance limits on R1 has reduced the contribution of its variability to each performance measure by three quarters whilst leaving the contributions made by the other components unchanged.



**Figure 6-5 The Effect of Tolerance Scaling**

This property of the  $\frac{1}{C_{pk}^2}$  representation may be confirmed through the use of an additional simulation using the new component tolerances, the results of such a simulation may be seen below in Figure 6-6 where  $V_x$  and  $V_x!$  represent the same quantities as in Figure 6-5 whilst  $V_x^*$  shows the results of an additional Monte Carlo simulation replacing the original tolerance of 10% by 5%. The small differences in bar height are due to the nature of Monte Carlo simulation, using different parameter values for each sample.

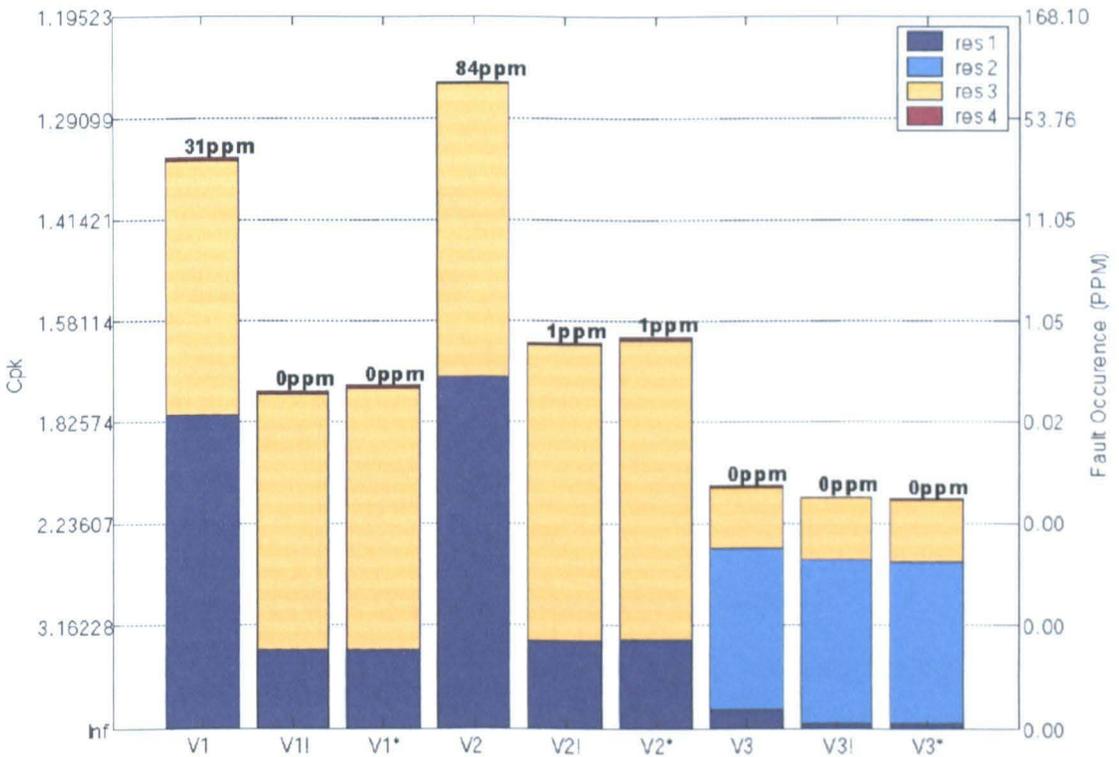


Figure 6-6 Confirmation of the Scaling Factors Accuracy

In general, it is found that variability in a particular controlling factor affects different aspects of process performance by different amounts and so it can be difficult to determine which controlling factor tolerance should be altered to achieve the greatest overall increase in capability. The data presented in the Capability Histogram (Figure 6-4) may be recast to indicate the contribution that each controlling factor makes to capability for each aspect of performance. In other words, a histogram may be plotted showing  $I_j = \sum_{i=1}^M I_{ij}$  broken down into the individual  $I_{ij}$  terms in the summation (M is the number of aspects of performance considered). An example of this representation may be seen Figure 6-7, which illustrates sample data.

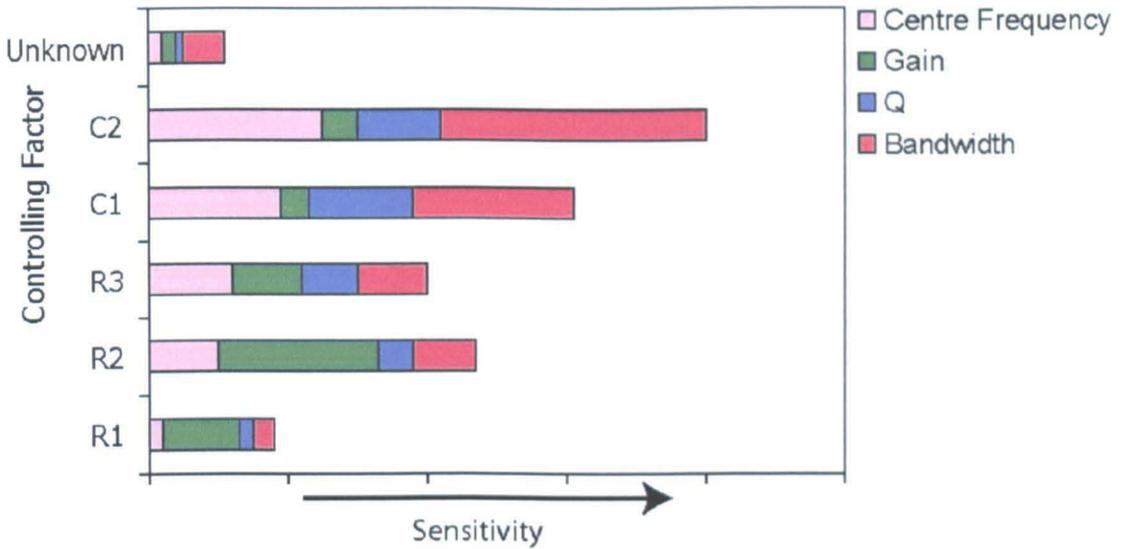


Figure 6-7 Capability Contributions by Component

Figure 6-7 demonstrates this ‘recasting’, note the lack of scale on the x-axis for this graph as the scale would have no real numerical significance and would hence be likely to mislead engineers it has instead been replaced with an indication of increasing sensitivity. Rather than using this graph to gain numerical design information it should be treated as an indication of the influence a particular component has over a product, this enables engineers to target efforts to improve a design by concentrating on those components which have the greatest influence.

## 6.7 Cost Breakdown

Further to the standard capability breakdown we may rescale the individual bars according to the costs likely to be incurred by a lack of conformance in any individual performance aspect.

As the cost incurred for any performance aspect is a function of its rate of occurrence and the impact of a particular fault, we may simply rescale the elements of each bar to give a cost breakdown as shown in Figure 6-8.

$$C_o = O \times 10^{I-4} \quad (90)$$

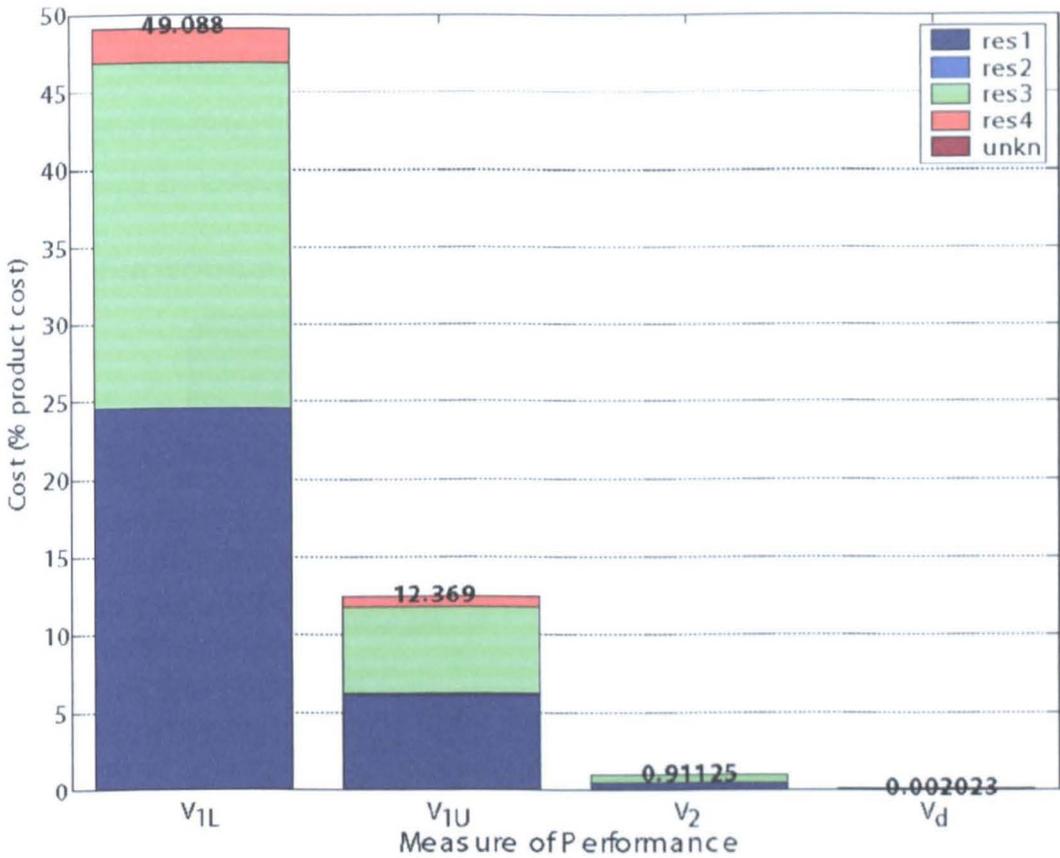


Figure 6-8 An Example Cost Breakdown

## 6.8 Summary

This chapter has introduced a technique for decomposing the capability associated with the CTQ aspects of an electronic system into the contributions attributable to individual factors. The developed capability breakdown is a powerful tool for the analysis of the causes of quality costs associated with a particular system feature or function. It enables sensible decisions to be made regarding design changes and helps to deflect the tendency of excessive variation to be corrected simply through the use of tighter tolerance ranges. Although it also has considerable power in that it can be used to assess the impact of tolerance band changes without the need to result to further simulation.

# 7 Summary of the Application Procedure

This chapter provides a summary of the application of *eCA* to a generalised electronic system using the techniques and tools described in the preceding chapters.

## 7.1 Functional Capability Analysis

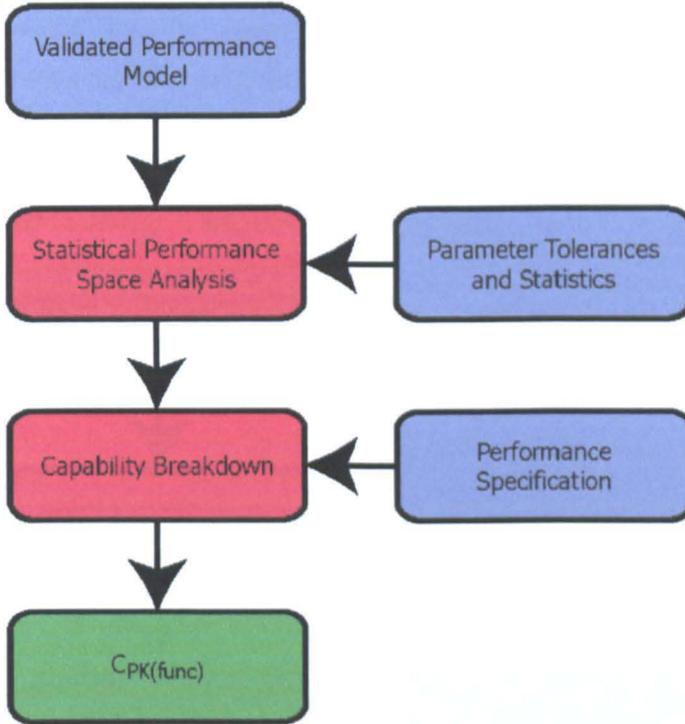


Figure 7-1 Block Diagram Showing the Main Steps to the Estimation of Functional Capability

The first requirement of the functional analysis module is the development of a functional performance model, this model may be at any level of abstraction capable of delivering performance information in sufficient detail for comparison with the system specification. It is also acceptable to use mixed level models provided that the quality of the performance data provided by the model is not compromised. Once a model has been created or obtained it is necessary to create a set of statistics describing the frequency distribution of values that the factors controlling the system and hence the model may take. If any factor distributions are unknown a good first assumption would be to assume a normal distribution centred on the nominal value and the standard deviation set to one third of the closest tolerance band. Once statistics defining the frequency distributions of each of the controlling factors have been established statistical exploration of the performance space may be carried out. The preferred technique for this analysis is the application of Monte Carlo analysis, however any analysis technique providing a similar quality of performance information may be used.

Following statistical analysis of the system performance space the data is subjected to a sensitivity analysis and the resulting information is used in combination with the performance specification and the curve fitting technique described in chapter 1 to produce a capability breakdown. The simplest method of carrying out this procedure is to apply the Matlab based tools provided as part of the eCA toolbox described in Appendix A. Following the creation of the capability breakdown the capability information provided by the capability breakdown should be entered into the conformability matrix together with the Impact (Severity) associated with each potential failure.

## 7.2 Manufacturing Capability Analysis

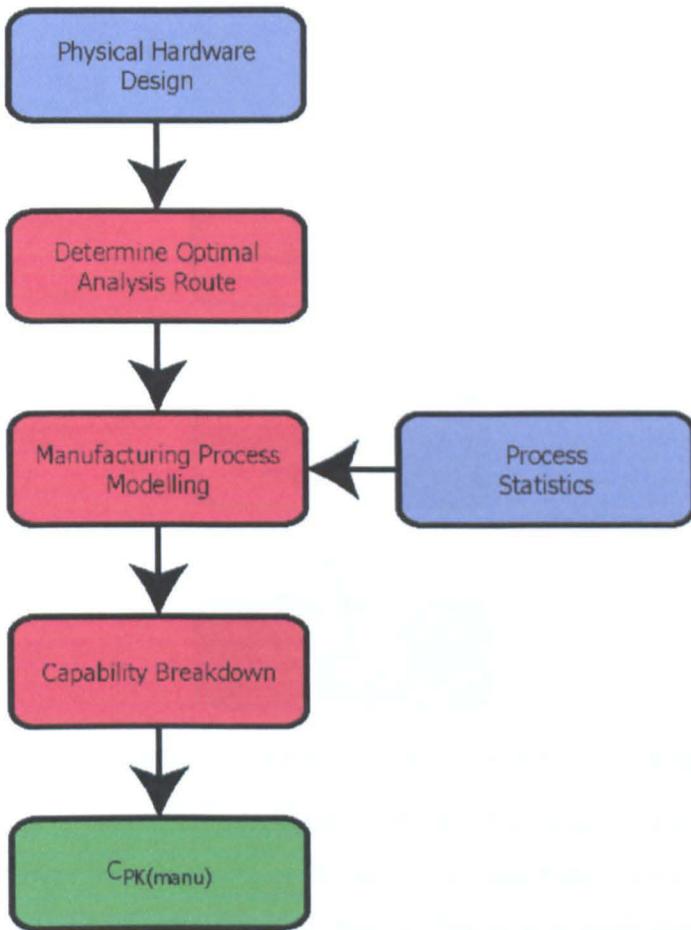


Figure 7-2 Block Diagram Representing the Application of Manufacturing Capability Assessment

The first step that must be undertaken to determine the manufacturing capability associated with the design is to determine the optimal analysis route; for example an engineer may decide to use physical modelling or historical data analysis as described in Chapter 4. Once the optimal analysis route has been decided upon we may calculate the defect occurrence rate associated with the manufacture of a system, further to this

dependent upon the analysis route undertaken we may also produce a capability breakdown for the system manufacture. Upon completing the estimation of the defect occurrence rates associated with the manufacture of the electronic system the data should be entered into the conformability matrix along with the associated Impact (severity) figures.

### 7.3 Test Process Analysis



Figure 7-3 Block Diagram Showing the Main Elements of Test Capability Analysis

Test capability analysis is a two stage procedure, the first stage is aimed at discovering the rate of occurrence of Type I and II test errors associated with hard defect free systems and hence the associated cost of quality. The second stage estimates the rate of occurrence of Type II test errors associated with defective systems and the consequential quality costs associated with these errors. The first part of the analysis simulates the test process applied to a standard system performance model and hence allows the estimation of the rate of occurrence Type I and II errors due to the parametric variability associated with both the circuit and test process. The second stage of the analysis process simulates the test process applied to a system model which includes an

‘injected defect’ (for example a resistor may be replaced by a low resistance connection to simulate the presence of a short) this process allows the occurrence of Type II test errors associated with the combinational effects of system defects and test parametric variation to be estimated. This analysis procedure may incur a high computational cost in complex systems, to combat this a two level procedure is suggested for the second half of the analysis. The first stage of this procedure is a screening phase during this phase of the analysis small sample ( $\approx 30$ ) statistical simulations should be carried out, the results of each of these small samples should then be analysed and only those system configurations with border line results should be exposed to the more detailed second phase of the analysis. Once the defect occurrence rate (DPMO) associated with each potential system failure mode has been established an equivalent value of  $C_{PK}$  may be calculated, and the defect rates entered into the conformability matrix.

#### 7.4 Quality Cost Estimation

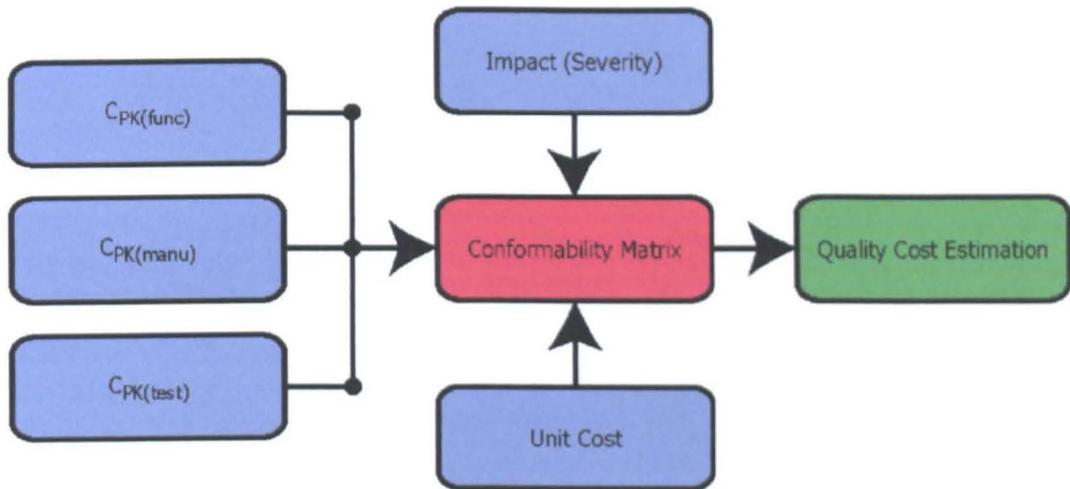


Figure 7-4 Block Diagram of the Quality Cost Estimation Procedure

The final stage of the *eCA* process converts the capability or defect occurrence figures calculated by each of the analysis modules into a quality cost estimation, this process is illustrated in Figure 7-4. The quality cost estimation is made by entering the appropriate capability or defect occurrence figures into the conformability matrix along with the associated failure Impact (severity) figures. This information is then automatically converted into a quality cost estimation. Two forms of the quality cost estimation are presented, firstly the cost associated with each of the CTQ functions is displayed as part of the main matrix and secondly the summary matrix presents a composite quality cost estimate for the entire system. At the same time an estimate of the quality costs that

would be expected should the system achieve six sigma quality levels is also made for comparison with the current expected level of quality.

## 8 Example Analysis – Potential Divider

The purpose of this chapter is to provide an overview of the practical application of electronic conformability analysis through demonstration using a simple product. The example given is not a case study but a simple circuit design to showcase the features of the technique, the circuit provided is a twist on the common potential divider circuit.

### 8.1 Introduction

A circuit is to be designed to meet the performance specification given in Figure 8-1. The Impact (Severity) of a failure to meet this specification is also given in Figure 8-1. Note that for  $V_2$  and  $V_d$  the Impact of failing to meet either the upper or lower specification limit is the same. However, in the case of  $V_1$  the Impact of exceeding the upper or lower limit differs; with more severe consequences attached to a failure to meet the lower specification limit.

<b>INDEX</b>	<b>PARAMETER</b>	<b>LSL</b>	<b>USL</b>	<b>IMPACT (SEVERITY)</b>
1	$V_1$ min	7.55	-	8
2	$V_1$ max	-	8.45	6
3	$V_2$	7.52	8.42	6
4	$V_d$	0.33	0.46	7

Figure 8-1 Potential Divider Circuit Performance Specification

### 8.2 Circuit Design

A proposed design based upon a potential divider circuit is given in Figure 8-2 where resistors R1, R3 and R4 will have a tolerance of 10% whilst R2 will have a tolerance of 5% and the proposed PCB layout is shown in Figure 8-3. For the purpose of this example we will assume that historical statistics are available for the proposed manufacturing route and that they indicate that the probability of failing to correctly place a component resulting in an open circuit defect is 10dpmo, whilst the probability of a short circuit defect is dependant upon the distance between the two nodes. The probabilities of occurrence of such a defect for the distances on the proposed PCB are given below in Figure 8-4.

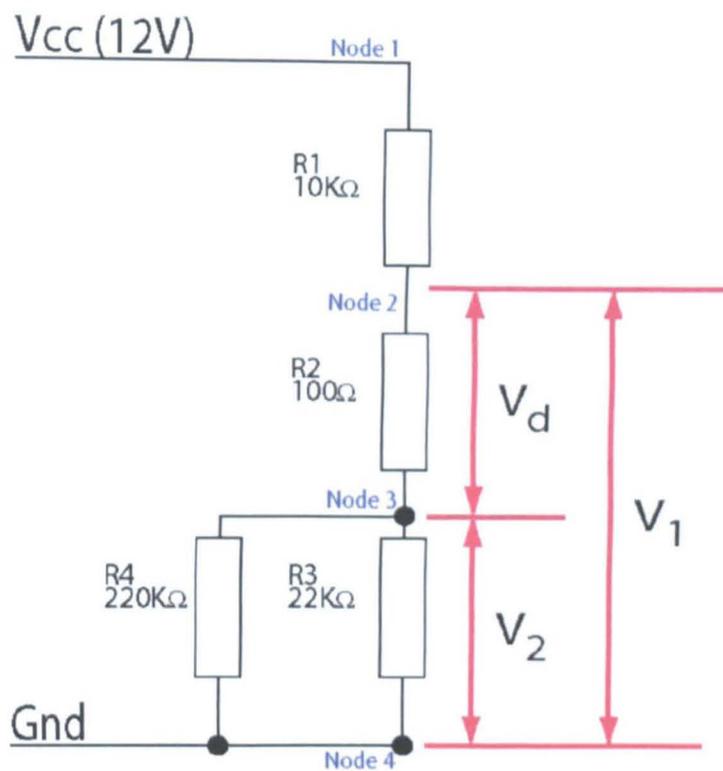


Figure 8-2 Proposed Potential Divider Circuit Design

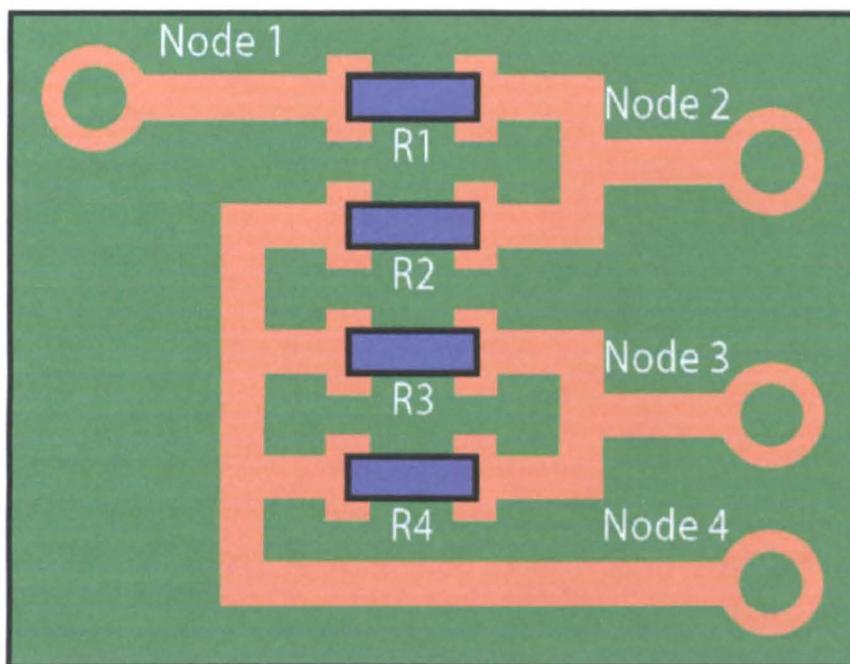


Figure 8-3 Proposed PCB Layout for the Potential Divider

Nodes	N1	N2	N3	N4
N1	1	10dpmo	1dpmo	100dpmo
N2		1	10dpmo	10dpmo
N3			1	100dpmo
N4				1

Figure 8-4 The Frequency of Occurrence of Short Circuit Faults Between Circuit Nodes

### 8.3 Statistical Modelling

This simple circuit may be modelled in a number of different ways including the use of a straight forward SPICE model. Alternatively the circuit as shown in Figure 8-2 may be described analytically by the following equations which may be easily represented in a mathematical package such as Matlab.

$$i = \frac{VS}{R1 + R2 + \left( \frac{R3R4}{R3 + R4} \right)} \quad (91)$$

$$V1 = i * \left( R2 + \frac{R3R4}{R3 + R4} \right) \quad (92)$$

$$V2 = i * \frac{R3R4}{R3 + R4} \quad (93)$$

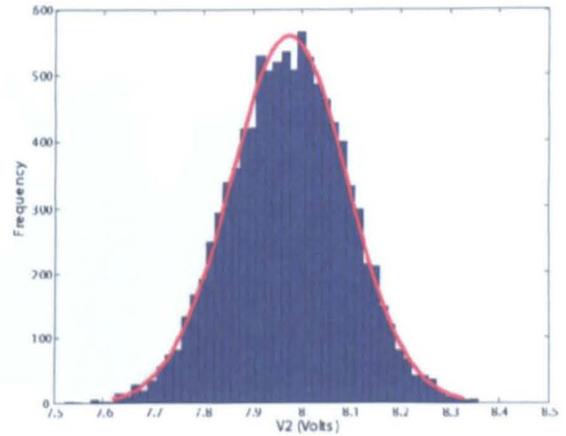
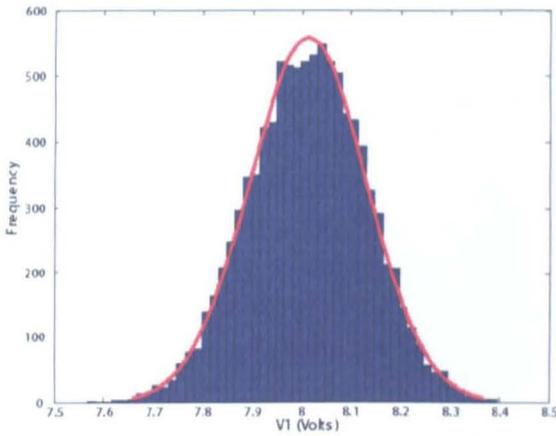
$$Vd = V1 - V2 \quad (94)$$

Hence for the purposes of this example we may carry out a statistical exploration of the performance space of this circuit using a simple Matlab script to apply a Monte Carlo analysis. The Matlab script works by taking N sets of pseudo random samples from the parameter space of the circuit and for each sample calculating the resulting circuit performance. Truncated normal distributions are used to represent the typical spread of values a resistor may take, given that resistors are selected according to tolerance bands which lie approximately at +/- 3σ, for example a 100Ω 10% resistor would have a σ of approximately 3.33Ω.

## 8.4 Functional Analysis

The purpose of the functional analysis is as previously stated to assess the conformance of the circuit to its performance specification when subject to no defects or variations introduced by the manufacturing process route. For the purpose of this example the statistical exploration of the circuits functional performance space consisted of 10,000 samples taken from the population using Monte Carlo Analysis. Histograms of the distributions of each of the voltages ( $V_1$ ,  $V_2$  &  $V_d$ ) are given below in Figure 8-5. From these histograms which each include a fitted normal curve it can be seen that the data follows a normal distribution and hence for this analysis the curve fitting technique will not be required.

These distributions may be analysed with respect to the performance specification using the Matlab based electronic Conformability Analysis toolbox described in Appendix A. The results of this analysis are presented below in Figure 8-6 and Figure 8-7 in the form of both a functional capability and functional cost breakdown. The results of the functional analysis are also summarised in Figure 8-8 which presents both the capability and associated quality costs for a particular performance defect together.



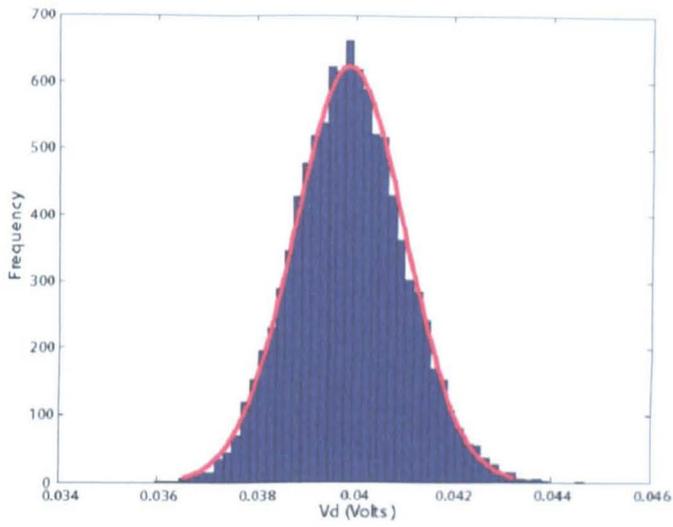


Figure 8-5 Histograms of the Distribution of  $V_1$ ,  $V_2$  &  $V_d$  as Predicted by the Circuit Model

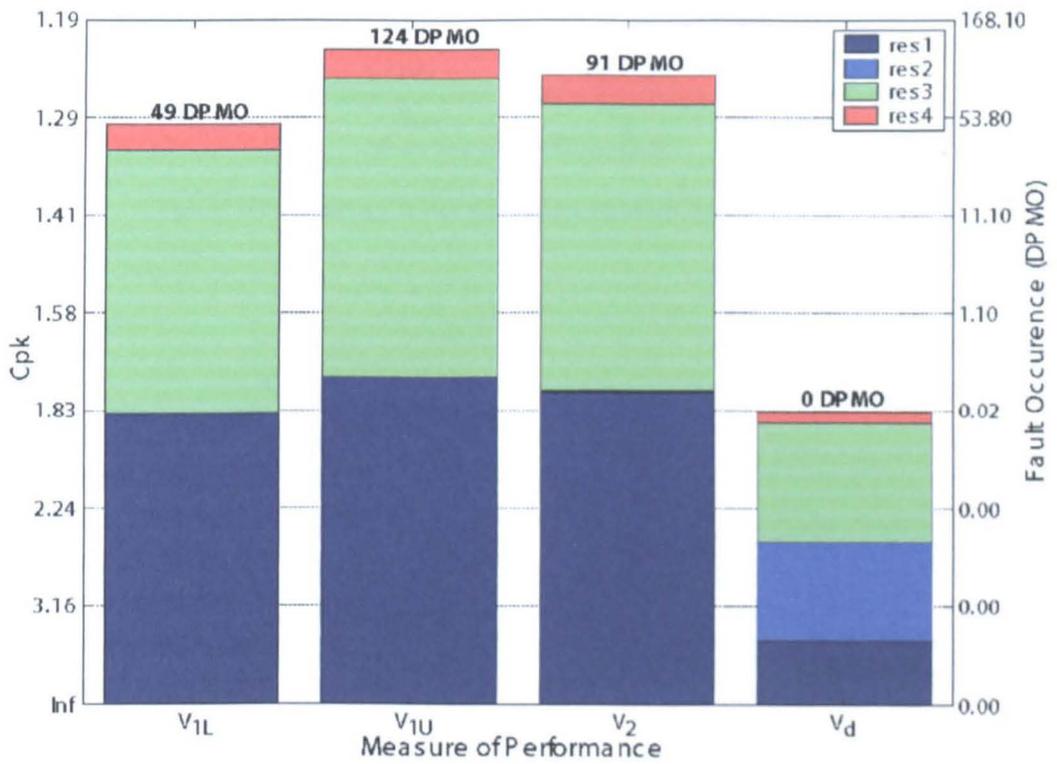
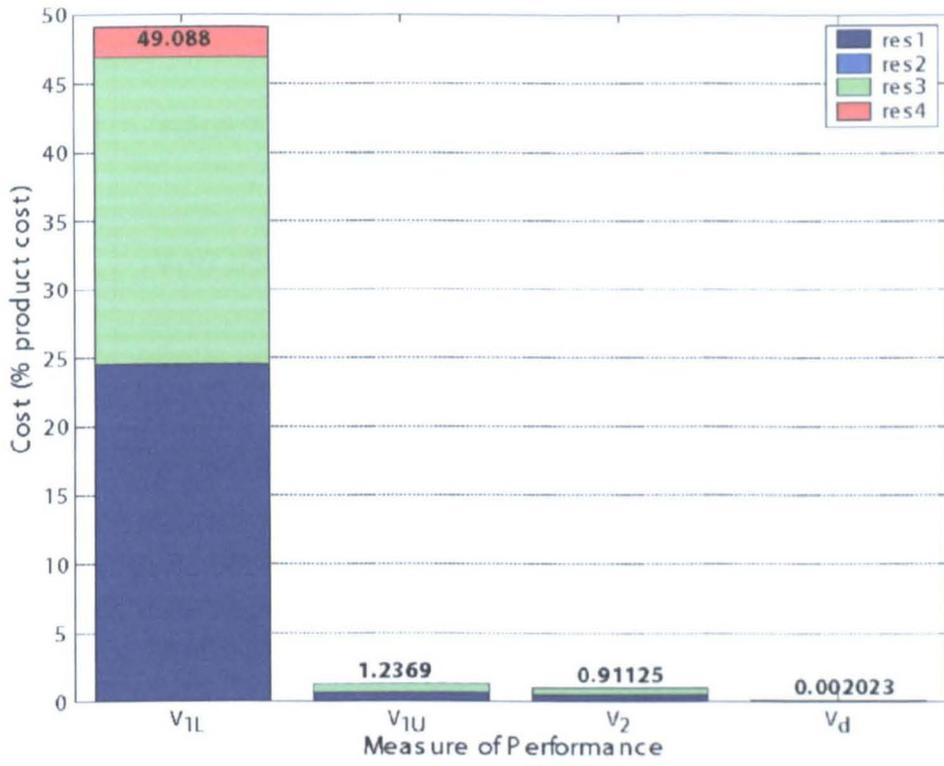


Figure 8-6 Potential Divider Circuit Functional Capability Breakdown



**Figure 8-7 Potential Divider Circuit Functional Quality Cost Breakdown**

<b>INDEX</b>	<b>FAULT</b>	<b>IMPACT (SEVERITY)</b>	<b>Cpk</b>	<b>OCCURRENCE (DPMO)</b>	<b>COST (% PRODUCT COST)</b>
1	$V_1 < 7.55$	8	1.30	49	49.090
2	$V_1 > 8.45$	6	1.22	124	1.240
3	$V_2 < 7.52$ or $V_2 > 8.42$	6	1.25	91	0.910
4	$V_d < 0.33$ or $V_d > 0.46$	7	1.83	0	0.002

**Figure 8-8 Summary of Functional Conformability Analysis Results for the Proposed Potential Divider Circuit Design**

### **8.5 Manufacturing Analysis**

The purpose of the manufacturing analysis is to determine the impact of the proposed manufacturing route in terms of both the number of defective boards produced and the potential associated quality costs.

Given the probabilities of short circuit faults in Figure 8-4, it is straightforward to determine the resulting quality cost. It should be noted that a single fault can affect several aspects of the specification so, for instance, a short between nodes 1 and 2, with an occurrence of 10dpmo, will result in a failure to meet specification 1,3 and 4 with associated quality costs of 10%, 0.1% and 1% respectively due to the differing impact (severity) ratings. It should also be noted that in some instances there is only a certain probability that a particular fault will affect a certain aspect of the specification. For instance a short circuit fault between nodes 2 and 3 (occurrence 10dpmo) will cause the circuit to fail to meet specification 4 but will only have a 13ppm probability of affecting specification 1. Although specification 1 has a higher impact (severity) the very low probability (10dpmo x 13dpmo) means the predicted cost is negligible. The quality cost attributable to a given defect may be calculated as shown below in equation 95:

$$C_o = O * 10^{I-4} \quad (95)$$

consider a short between N1 and N2 the costs incurred by such a defect would be 11.1% this is the summation of the cost due to the defect occurrence and impact for each

performance metric. The total expected cost for all short circuit faults is 139% of the product cost and the individual elements of this are given in Figure 8-9, open circuit faults may be treated similarly and the breakdown of the elements of the total cost for open circuit faults are also given. It may be noted that although most open circuit faults are almost certain to cause out of specification behaviour, an open circuit on  $R_4$  will only affect specification 1 in 57% of cases because its effect is masked by being in parallel with  $R_3$ . The effects on other aspects of the specification have similar probabilities. The predicted total quality cost associated with open circuit faults is 41% of the product cost. The manufacturing analysis is summarised in Figure 8-9 shown on the following page.

As the manufacturing process is not capable with potentially high failure costs additional testing processes must be considered in an attempt to ensure that quality costs are minimized. These additional processes will be introduced, discussed and analysed in the following section.

<b>PERFORMANCE METRIC</b>	<b>DEFECT</b>	<b>MANUFACTURE</b>		
		<b>DPMO</b>	<b>IMPACT</b>	<b>COST (%)</b>
V1 Lower	Short N1 - N2	10.00	8.00	10.00
V2	Short N1 - N2	10.00	6.00	0.10
Vd	Short N1 - N2	10.00	7.00	1.00
V1 Lower	Short N1 - N3	1.00	8.00	1.00
V1 Upper	Short N1 - N3	1.00	6.00	0.01
V2	Short N1 - N3	1.00	6.00	0.01
Vd	Short N1 - N3	1.00	7.00	0.10
V1 Lower	Short N1 - N4	100.00	8.00	100.00
V1 Upper	Short N1 - N4	100.00	6.00	1.00
V2	Short N1 - N4	100.00	6.00	1.00
Vd	Short N1 - N4	100.00	7.00	10.00
V1 Lower	Short N2 - N3	0.00	8.00	0.00
V1 Upper	Short N2 - N3	10.00	6.00	0.10
V2	Short N2 - N3	10.00	6.00	0.10
Vd	Short N2 - N3	10.00	7.00	1.00
V1 Lower	Short N2 - N4	10.00	8.00	10.00
V1 Upper	Short N2 - N4	10.00	6.00	0.10
V2	Short N2 - N4	10.00	6.00	0.10
Vd	Short N2 - N4	10.00	7.00	1.00
V1 Lower	Short N3 - N4	0.00	8.00	0.00
V1 Upper	Short N3 - N4	100.00	6.00	1.00
V2	Short N3 - N4	100.00	6.00	1.00
V1 Lower	Open R1	10.00	8.00	10.00

**Figure 8-9 Summary of Manufacturing Capability Analysis Results**

<b>PERFORMANCE METRIC</b>	<b>DEFECT</b>	<b>MANUFACTURE</b>		
		<b>DPMO</b>	<b>IMPACT</b>	<b>COST (%)</b>
V1 Upper	Open R1	10.00	6.00	0.10
V2	Open R1	10.00	6.00	0.10
Vd	Open R1	10.00	7.00	1.00
V1 Lower	Open R2	10.00	8.00	10.00
V1 Upper	Open R2	10.00	6.00	0.10
V2	Open R2	10.00	6.00	0.10
Vd	Open R2	10.00	7.00	1.00
V1 Lower	Open R3	10.00	8.00	10.00
V1 Upper	Open R3	10.00	6.00	0.10
V2	Open R3	10.00	6.00	0.10
Vd	Open R3	10.00	7.00	1.00
V1 Lower	Open R4	5.70	8.00	5.70
V1 Upper	Open R4	5.70	6.00	0.06
V2	Open R4	6.20	6.00	0.06
Vd	Open R4	10.00	7.00	1.00

**Figure 8-10 Summary of Manufacturing Capability Analysis Results (Continued)**

## **8.6 Test Analysis**

The purpose of the test analysis is to determine the effectiveness of the proposed test regime and to make an estimate of the quality costs associated with any test errors which are expected to occur.

In order to assess the effectiveness of the proposed test regime and its associated quality costs we must first understand the probabilities of occurrence of Type I and Type II errors in the presence of measurement inaccuracies. The proposed test limits and the measurement noise associated with each are given in Figure 8-11. It should be noted that the figure shows the possibility for differing test and specification limits to be considered. This is in fact a common practice particularly when a product will be subject to additional manufacturing stages with the potential to influence product performance following a test. It is assumed that the noise follows a normal distribution with a mean of zero and the standard deviation given.

<b>INDEX</b>	<b>PARAMETER</b>	<b>LSL</b>	<b>USL</b>	<b>LOWER TEST LIMIT</b>	<b>UPPER TEST LIMIT</b>	<b>MEASUREMENT NOISE DEVIATION</b>
1	$V_1$	7.55	-	7.55	-	10mV
2	$V_1$	-	8.45	-	8.45	10mV
3	$V_2$	7.52	8.42	7.52	8.42	10mV
4	$V_d$	0.33	0.46	0.33	0.46	50 $\mu$ V

**Figure 8-11 Proposed Test Limits and the Associated Standard Deviation of the Error in the Measurement**

The effects of these measurement inaccuracies are summarised below in Figure 8-12 where the expected occurrence rates for Type I and Type II errors are given with respect to measurements taken from circuits with only soft (tolerance induced) defects. The performance data generated during the functional analysis stage provided the input to this analysis and the analysis was performed using the `test_error` function included with the electronic conformability analysis toolbox.

<b>INDEX</b>	<b>TEST</b>	<b>TYPE I (DPMO)</b>	<b>TYPE II (DPMO)</b>
1	$V_1 < 7.55$	2.90	6.09
2	$V_1 > 8.45$	4.91	10.58
3	$V_2 < 7.52$ or $V_2 > 8.42$	7.52	16.07
4	$V_d < 0.33$ or $V_d > 0.46$	0.00	0.00

**Figure 8-12 Probabilities of Type I and Type II Errors for Measurements Against Functional Specification**

In the case of most catastrophic faults, these tests are fully capable since the output voltages move to extreme values. In the case where  $R_4$  is absent and when nodes 2 and 3 are shorted there is a finite probability of type II errors as listed below in Figure 8-13

INDEX	FUNCTIONAL FAILURE		R4 OPEN CIRCUIT (10 DPMO)		SHORT NODES 2-3 (10 DPMO)		TOTAL (DPMO)	
	TYPE I	TYPE II	TYPE I	TYPE II	TYPE I	TYPE II	TYPE I	TYPE II
1	2.90	6.09	NA	1000,000	NA	999900	2.90	1,999,906
2	4.91	10.58	NA	932426	NA	999924	4.91	1,932,361
3	7.52	16.07	NA	941310	NA	999728	7.52	1,941,054
4	0.00	0.00	NA	1000,000	NA	0.00	0.00	1,000,000

Figure 8-13 Unadjusted Test Error Occurrence Expressed in DPMO for Both *Soft* and *Hard* Defects

In calculating the quality costs arising from type II errors due to manufacturing faults we must take account of the probability of the fault occurrence. Thus the probability of a short circuit fault (10dpmo) and it passing test 1 (999900dpmo) is  $10\text{dpmo} \times 999900\text{dpmo} = 10\text{dpmo}$ , the adjusted failure rates are given in Figure 8-14.

INDEX	FUNCTIONAL FAILURE		R4 OPEN CIRCUIT (DPMO)		SHORT NODES 2-3 (DPMO)		TOTAL (DPMO)	
	TYPE I	TYPE II	TYPE I	TYPE II	TYPE I	TYPE II	TYPE I	TYPE II
1	2.90	6.09	NA	10.0	NA	10.0	2.90	26.09
2	4.91	10.58	NA	9.3	NA	10.0	4.91	29.90
3	7.52	16.07	NA	9.4	NA	10.0	7.52	35.48
4	0.00	0.00	NA	10.0	NA	0.0	0.00	10.00

Figure 8-14 Adjusted Test Error Occurrence Expressed in DPMO

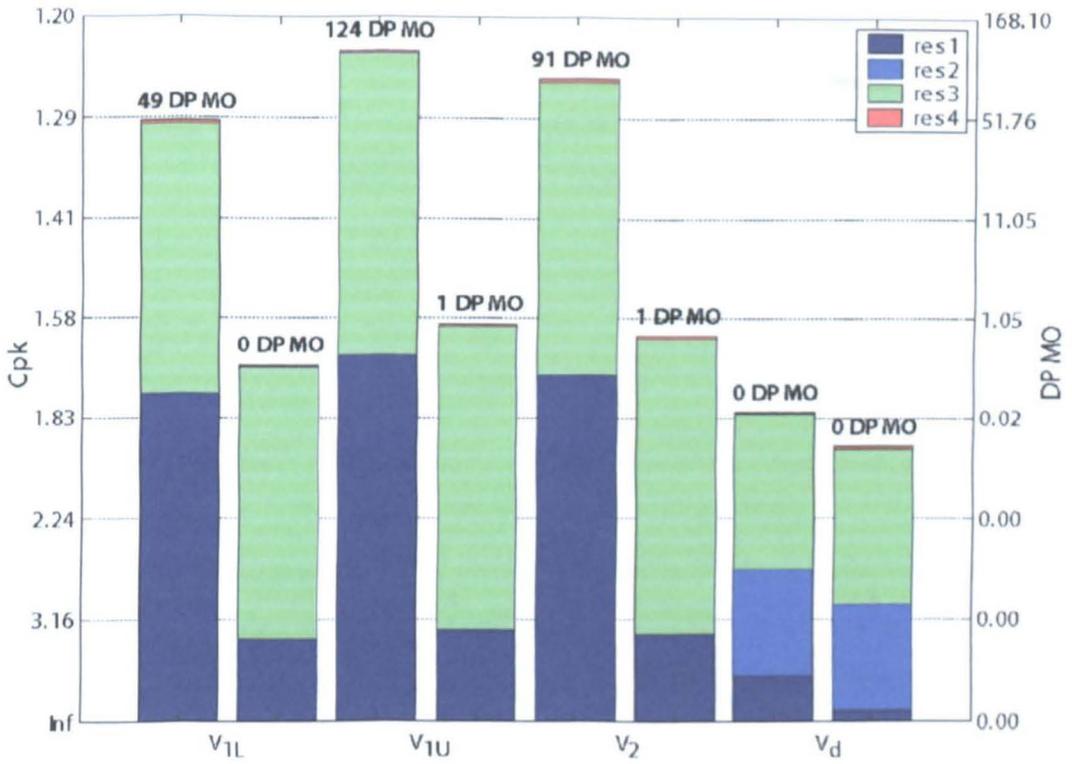
Thus given 1000,000 opportunities 26.09ppm type II errors arising with test 1 (this figure arises from  $6.09 + 10.0 + 10.0$ ) would be shipped and the resulting quality cost would have an impact (severity) of 8, giving a quality cost of 26% of product cost (calculated using equation 95). Similar calculations may be made for each test, and a summary of the expected quality costs due to both soft and hard defect occurrence, combined with test error failure, is given in Figure 8-15.

<b>INDEX</b>	<b>TYPE I (PPM)</b>	<b>TYPE II (PPM)</b>	<b>COST TYPE I</b>	<b>COST TYPE II</b>	<b>TOTAL COST</b>
1	2.90	26.09	2.900%	26.090%	28.99%
2	4.91	29.90	0.049%	0.2990%	0.35%
3	7.52	35.48	0.075%	0.3548%	0.43%
4	0.00	10.00	0.000%	1.0000%	1.00%
					30.77%

**Figure 8-15 Summary of Quality Costs After the Application of EOL Test for the Potential Divider Circuit Expressed as a Percentage of Total Product Cost**

### **8.7 Product Improvements**

Clearly from the results presented in Figure 8-6 the circuit design is not acceptable. The high levels of 'soft' defect occurrence with regard to specification areas 1,2 and 3 are a cause of concern. The defects occurring in specification area 1 are however the most serious with the high associated quality cost of 49% indicated in Figure 8-7. Figure 8-6 and Figure 8-7 also indicate the solution to the problem. If the variability in either  $R_1$  or  $R_3$  could be reduced then the capability would increase and the fault occurrence and cost reduce. Since both components make a similar contribution to the number of faults we can achieve a similar result whichever one we modify. We will select  $R_1$  for modification. Considering Figure 8-6 if we halve the tolerance band associated with  $R_1$  we would expect that element of the histogram to be reduced in size by a factor of 4, increasing capability and reducing the occurrence of faults in all areas but particularly  $V_{1U}$ ,  $V_{1L}$  and  $V_2$  this is depicted in Figure 8-16. For example reducing the height of the  $R_1$  component of  $V_{1U}$  by  $\frac{3}{4}$  should increase the capability of the circuit with respect to that aspect of performance to around 1.7 from 1.3. We may apply the same reasoning to the cost breakdown shown in Figure 8-7 where we would expect the quality costs associated with the failure to meet the  $V_{1L}$  specification to reduce from 49% to around 0.22% of the product cost when the tolerance of  $R_1$  is halved.



**Figure 8-16 Comparison Between the Original and Modified Potential Divider Circuit**

The improvements in circuit performance gained through the reduction in size of the tolerance band of R1 are shown in Figure 8-16. The left hand bar in each pair represents the original circuit performance whilst the right hand bar is the performance of the modified circuit.

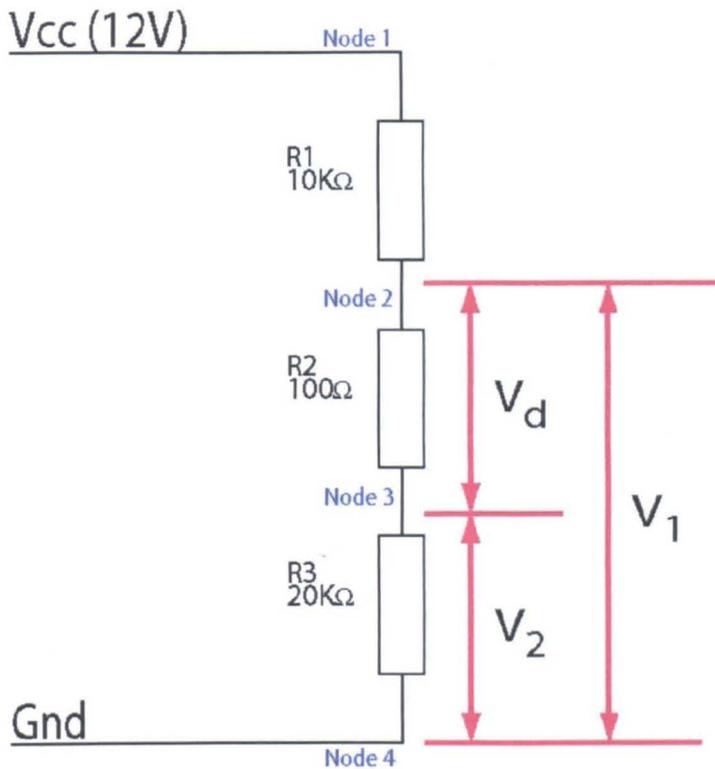
It would, of course, be possible to replace all of the components with more tightly toleranced devices and this would possibly result in a further reduction in quality cost. However, it is clear from Figure 8-16 that the reduction in performance variability achieved would result in only small gains and would probably be outweighed by the extra cost of the higher specification components.

A summary of the benefits gained through a reduction of the tolerance band of R1 from 10% to 5% is given in Figure 8-17.

INDEX	$C_{PK}$		OCCURRENCE (DPMO)		COST (% PRODUCT COST)	
	ORIG	MOD	ORIG	MOD	ORIG	MOD
1	1.30	1.67	49	0	49.090	0.28
2	1.22	1.59	124	1	1.240	0.01
3	1.25	1.61	91	1	0.910	0.01
3	1.83	1.92	0	0	0.002	0.00

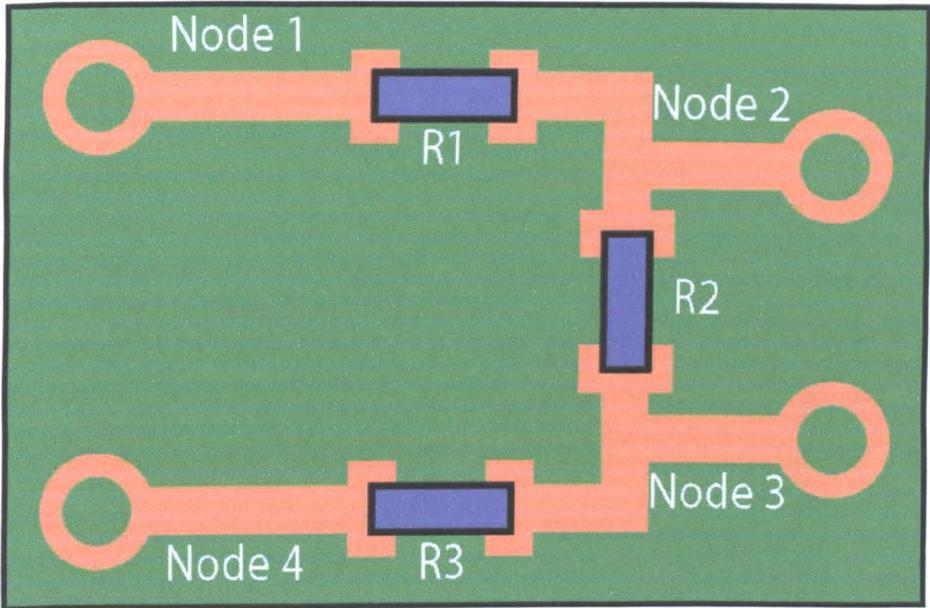
**Figure 8-17 Summary of the Improvements Gained in Circuit Functional Performance Gained from a Reduction in the Tolerance Band of R1**

There are also considerable quality costs associated with ‘hard’ manufacturing defects which were identified during the manufacturing and test analysis stages. These may be significantly reduced through the use of a ‘common sense’ circuit redesign – the replacement of R3 and R4 by a single 20KΩ 1% resistor.



**Figure 8-18 Circuit Diagram of the Modified Potential Divider Circuit**

The modified circuit is shown in Figure 8-18 and the counterpart modified PCB which could potentially be made smaller and has improved defects rates (shown in Figure 8-19 and Figure 8-20) due to better layout leading to increased distances between circuit nodes along with a reduced component count.



**Figure 8-19 PCB for the Modified Circuit**

Nodes	N1	N2	N3	N4
N1	1	10dpmo	1dpmo	1dpmo
N2		1	3dpmo	1dpmo
N3			1	10dpmo
N4				1

**Figure 8-20 The Frequency of Occurrence of Short Circuit Faults**

When this reduction in component count together with improved hard and soft defect rates is combined with the original test the quality costs are significantly reduced as shown in Figure 8-21. Also it should be noted that as R4 is no longer included in the circuit the 'R4 open' fault may no longer occur.

INDEX	FUNCTIONAL FAILURE		SHORT NODES 2-3 (DPMO)		TOTAL (DPMO)		COST (% PRODUCT COST)	
	TYPE I	TYPE II	TYPE I	TYPE II	TYPE I	TYPE II	TYPE I	TYPE II
1	0.01	0.01	NA	3.0	0.01	3.01	0.0100	3.0000
2	0.07	0.07	NA	3.0	0.07	3.07	0.0007	0.0307
3	0.05	0.05	NA	3.0	0.05	3.05	0.0005	0.0305
4	0.00	0.16	NA	0.0	0.00	0.16	0.0000	0.0160

**Figure 8-21 Test Error Occurrence and Cost for Both *Soft* and *Hard* Defects for the Modified Potential Divider Circuit.**

With a total cost of quality of only 3.088% the modified circuit is a significant improvement over the original circuit which had a cost of quality of 30.77%.

## **8.8 Summary**

This simple example presented in this chapter has shown how the eCA technique may be used to identify and reduce quality costs as well as demonstrating the advantages of the integrated analysis approach followed by the technique. This example has shown how the technique presents information in an easy to understand way and allows comparisons to be made between different aspects of a product allowing informed decisions regarding potential product improvements to be reached.

## **9 Case Studies**

This chapter presents four case studies each showing the application of *eCA* to a different problem and highlighting different advantages of the technique. Please note that in some of the following examples detail has been limited or omitted due to commercial agreements.

### **9.1 Automotive Current Monitor**

This section presents an automotive case study and shows how the conformability analysis technique may be used with a commercial circuit simulation package to produce an estimate of circuit capability.

#### **9.1.1 Introduction**

The current monitor circuit is used to monitor the current flowing in a coil and forms part of the feedback loop in an automotive braking system. The current flowing in the coil must be monitored accurately as it provides the only method of assessing the pressure being applied to the brake discs by the hydraulic calliper. The current monitor circuit is given Figure 9-1 which is an extract of a larger circuit, the entire circuit is not given due to commercial considerations. The current monitor circuit consists of a current mirror which is off balanced by the slightly different currents forced to flow down each side of the mirror by the voltage drop across the small current sense resistor. This effect is counter balanced by the third transistor which 'rebalances' the circuit and creates a potential difference at TP755 which is proportional to the current flowing through the current sense resistor.

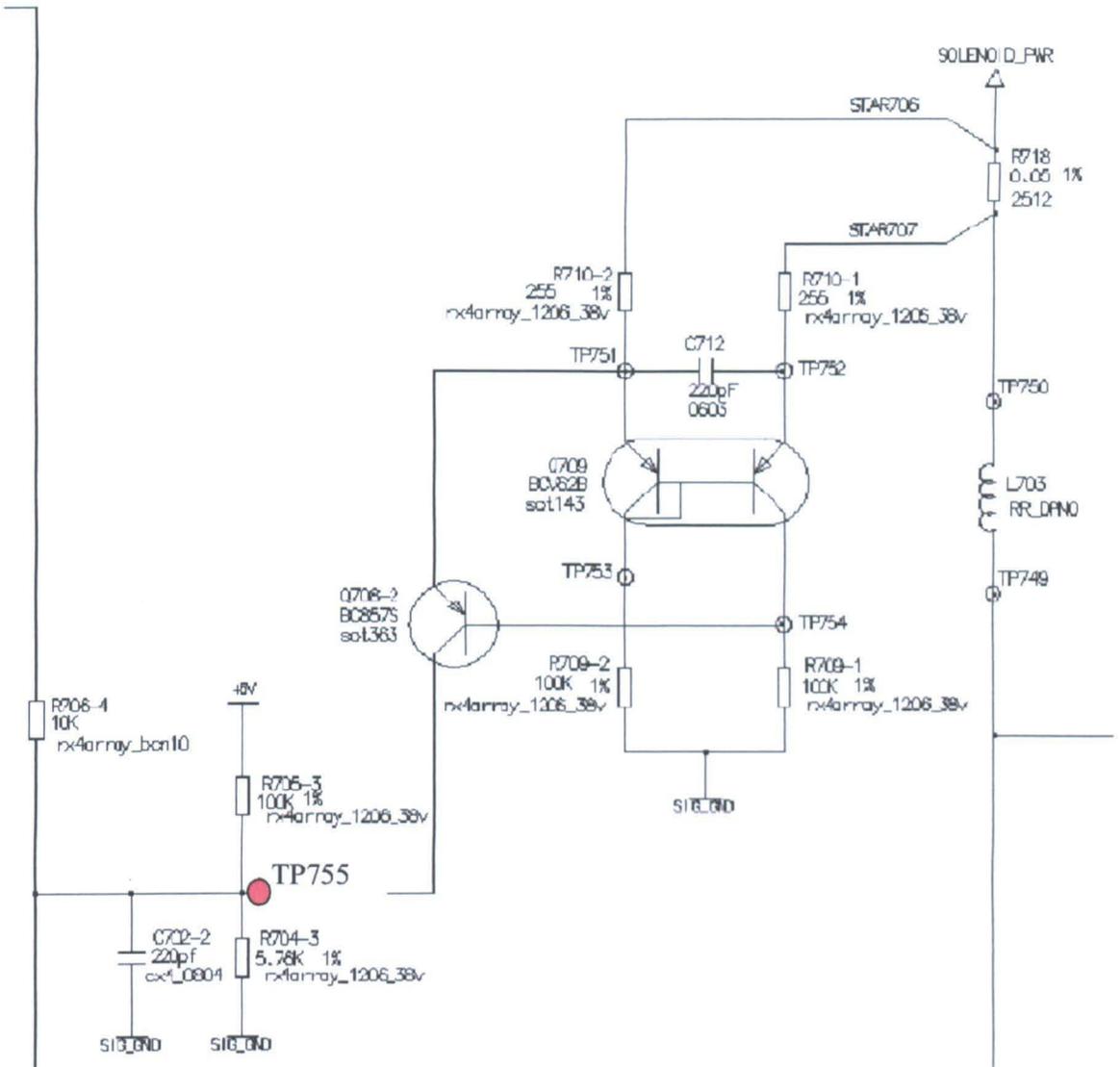


Figure 9-1 Current Monitor Circuit Diagram Extract

### 9.1.2 Description of Simulation Model & Analysis Strategy

The accuracy of a simulation depends upon the quality of the models used. In the case of this circuit the accuracy of a full statistical simulation is severely limited by the lack of a dedicated model for the BCV62B double transistor. This has, out of necessity, been modelled by two discrete devices. This modelling tactic provides credible analysis results in non statistical simulations (i.e. those where no parametric variations are introduced into the circuit) given the assumption that the transistors are well matched. In the case when statistical modelling is applied the differences introduced into the two discrete devices used to model the BCV62B will be sufficient to upset the ‘matching’ between the devices and hence this particular tactic is not suitable for application within a statistical simulation. However as there is currently no better model for the double

transistor device, in order to carry out a statistical evaluation of the circuit it is proposed that the double transistor is treated as a perfect device exhibiting both good matching and no parametric variation of its characteristics. This approach allows the effects of parametric variation of the circuits other components to be assessed but it is liable to underestimate the number of faults which may occur. A further possible inaccuracy of the model occurs in the treatment of resistor tolerance. This is modelled by a normal distribution with  $\sigma$  set to one third of the resistor tolerance, as the distribution is not and may not be truncated at the  $3\sigma$  points around 0.027% of the resistor values generated in a Monte Carlo analysis will lie outside of the resistors tolerance region, this equates to 2700ppm, which when dealing with sensitive circuits could lead to an overstatement of fault occurrence. It should be noted that resistor tolerance limits have been set to 4% within the SABER model instead of the prescribed 1%. This increase takes into account component parametric degradation over the lifetime of the product.

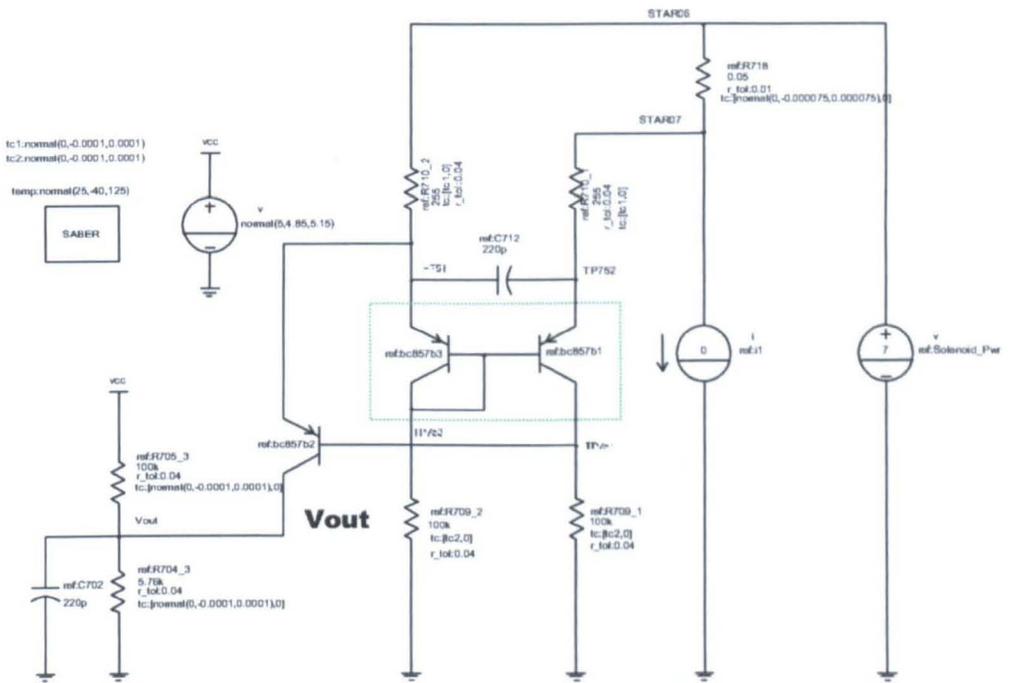


Figure 9-2 Schematic Diagram of the Circuit Model

Thirteen simulation runs were carried out each of which was a 1000 sample Monte Carlo statistical exploration of the circuit, for each simulation run the current supplied by  $i1$  was increased by 0.2A from a minimum of 0.0A to a maximum of 2.4A. The measure of performance used was the voltage at the node marked  $Vout$  in Figure 9-2.

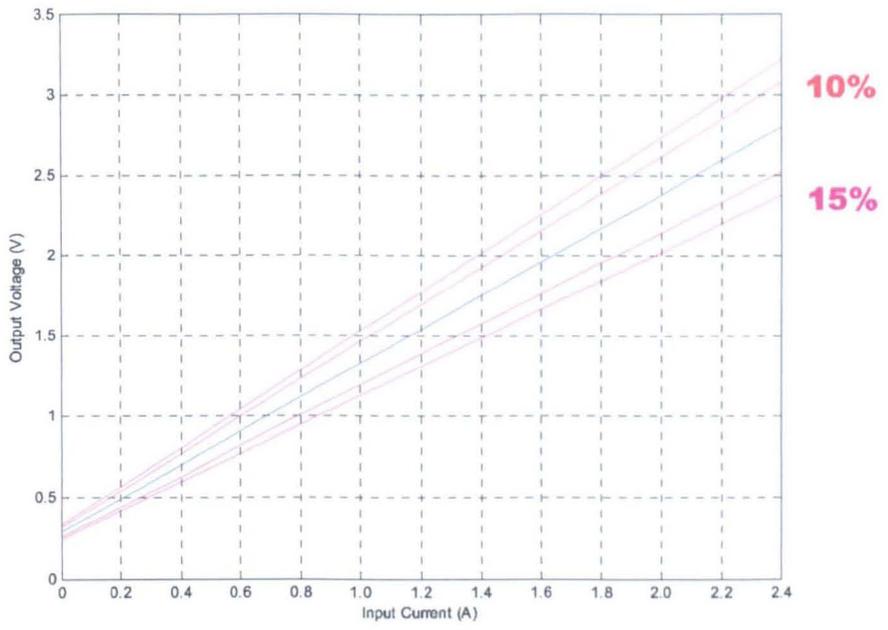
### 9.1.3 Specification Limits

The first problem identified by following the structured analysis procedure dictated by the *eCA* methodology is that the circuit currently has no performance specification limits defined. Hence for the purposes of the conformability analysis the circuit capability was assessed with two different sets of specification limits, firstly they were set to the nominal output voltage +/- 10% for a given input current and secondly to the nominal output voltage +/- 15% these limits are given explicitly for each analysis point in Figure 9-3, and are also represented graphically to show the divergence at higher currents in Figure 9-4.

For the purposes of this analysis the nominal output voltage is defined as the output voltage predicted by the circuit simulator for a given input current when all components take their nominal prescribed values.

Input Current (A)	Nominal Output Voltage (V)	10%		15%	
		LSL	USL	LSL	USL
0.0	0.2916	0.2624	0.3207	0.2478	0.3353
0.2	0.4927	0.4434	0.5419	0.4188	0.5666
0.4	0.7009	0.6308	0.7710	0.5958	0.8061
0.6	0.9103	0.8192	1.0013	0.7737	1.0468
0.8	1.1200	1.0080	1.2320	0.9520	1.2880
1.0	1.3300	1.1970	1.4630	1.1305	1.5295
1.2	1.5402	1.3861	1.6942	1.3091	1.7712
1.4	1.7504	1.5753	1.9254	1.4878	2.0129
1.6	1.9606	1.7645	2.1567	1.6665	2.2547
1.8	2.1709	1.9538	2.3880	1.8453	2.4965
2.0	2.3812	2.1431	2.6193	2.0240	2.7384
2.2	2.5915	2.3324	2.8507	2.2028	2.9803
2.4	2.8019	2.5217	3.0820	2.3816	3.2221

**Figure 9-3 Nominal Expected Outputs and Specification Limits**



**Figure 9-4 Graphical Representation of the Specification Limits**

### 9.1.4 Results

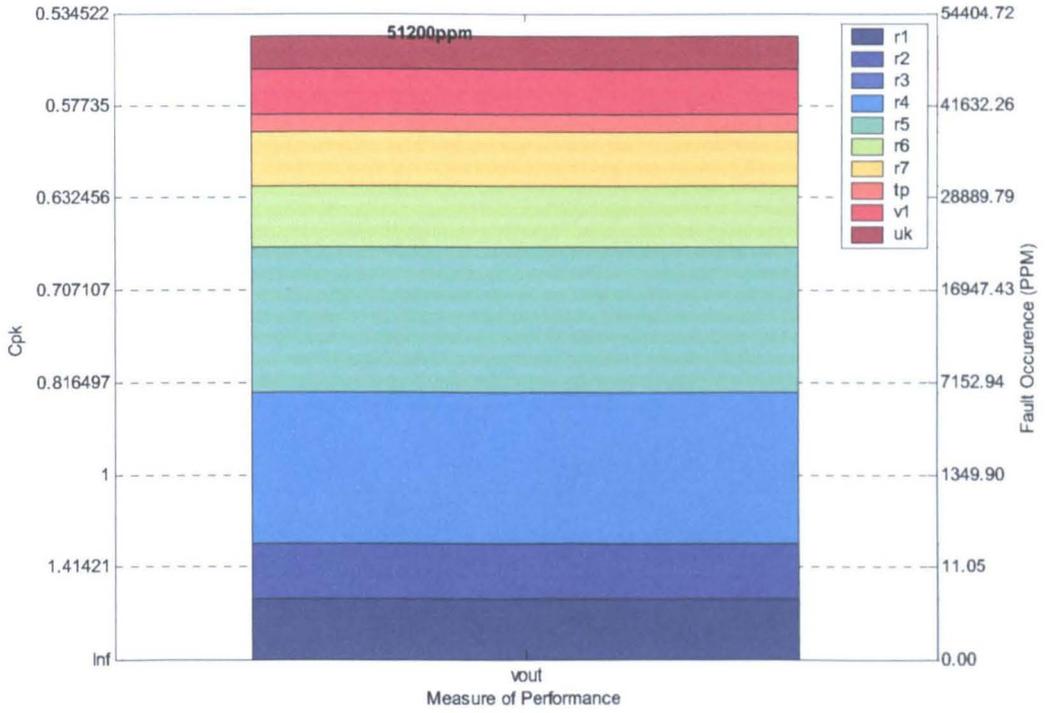
The circuit capability was assessed at a number of different current levels using Monte Carlo analysis and for both of the specification limit sets. The results of this work are summarised in Figure 9-5, example capability breakdowns to compliment this table are presented on the following pages. The capability breakdowns given show how the influence of the various components upon circuit operation changes as the operating point increases. For example the figure given in section 9.1.5.1 shows that the most influential circuit components at this operating point (0.0A) are r4 and r5 yet when the operating point is increased to 1.6A the breakdown shows that the most influential components are r1 and r6.

<i>Current</i>	<i>10%</i>		<i>15%</i>	
	<i>C<sub>PK</sub></i>	<i>DPMO</i>	<i>C<sub>PK</sub></i>	<i>DPMO</i>
0.0	0.58	51200	0.81	7419
0.2	0.6	7960	1.21	136
0.4	0.65	1155	1.52	3
0.6	1.15	278	1.75	0
0.8	1.40	13	2.10	0
1.0	1.37	21	2.03	0
1.2	1.55	2	2.32	0
1.4	1.56	1	2.31	0
1.6	1.59	1	2.38	0
1.8	1.59	1	2.40	0
2.0	1.65	0	2.47	0
2.2	1.67	0	2.49	0
2.4	1.64	0	2.46	0

**Figure 9-5 Summary of Circuit Capability at Different Currents**

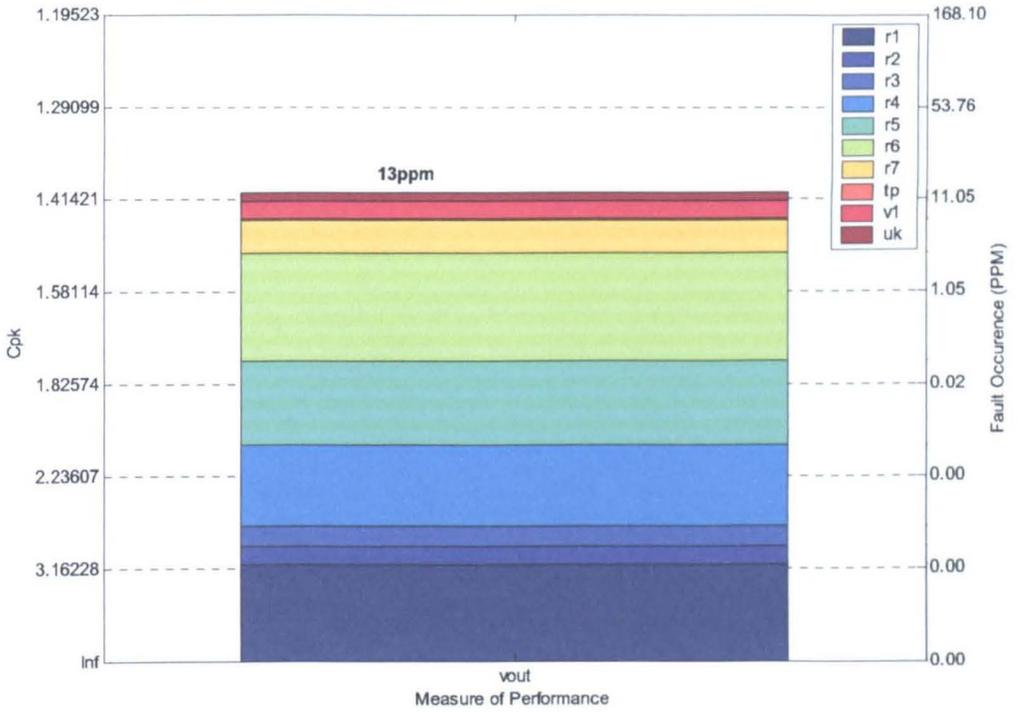
## 9.1.5 Example Capability Breakdowns

### 9.1.5.1 0.0A

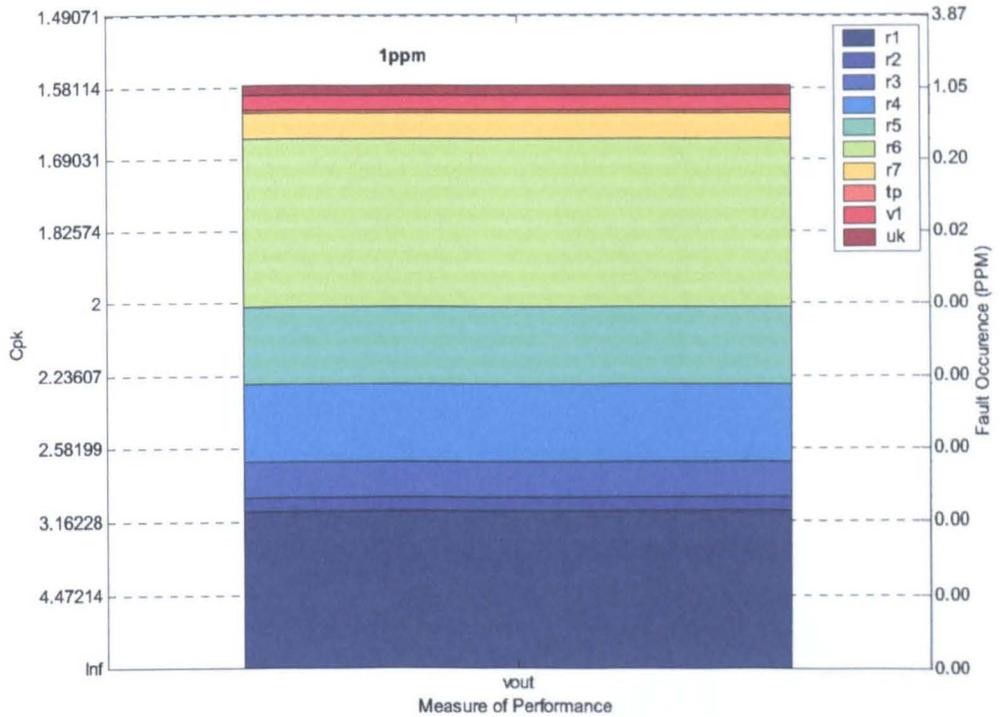


*r1 to 7 = resistors 1 to 7 as shown in Figure 9-2, tp = ambient temperature, v1 = voltage supplied by source v1 i.e. VCC, uk = unknown or unaccounted for effects.*

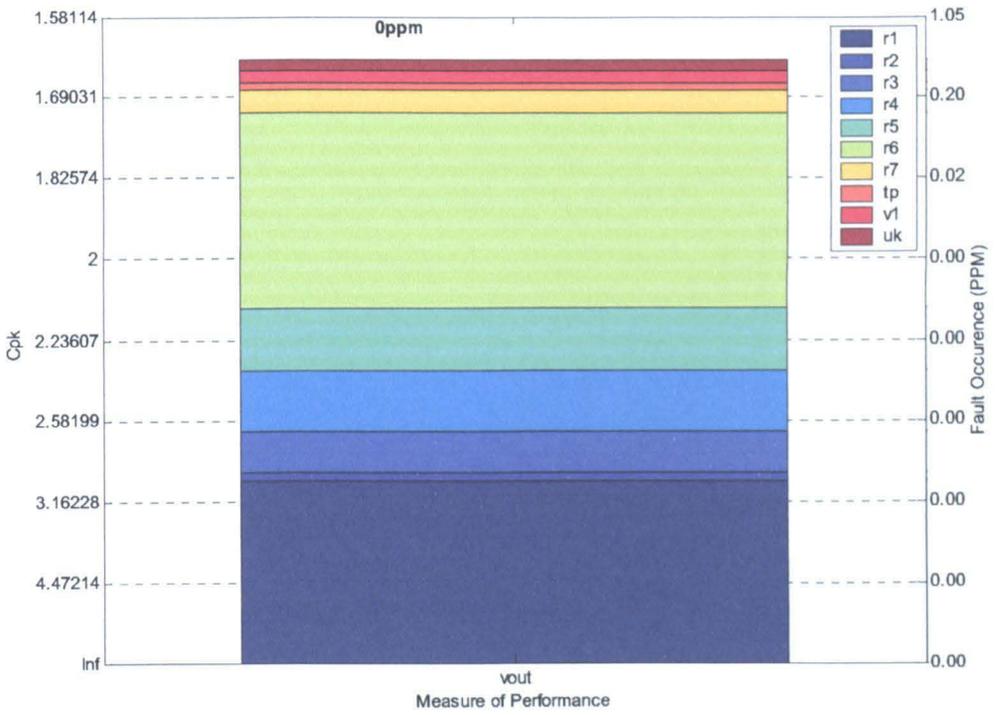
### 9.1.5.2 0.8A



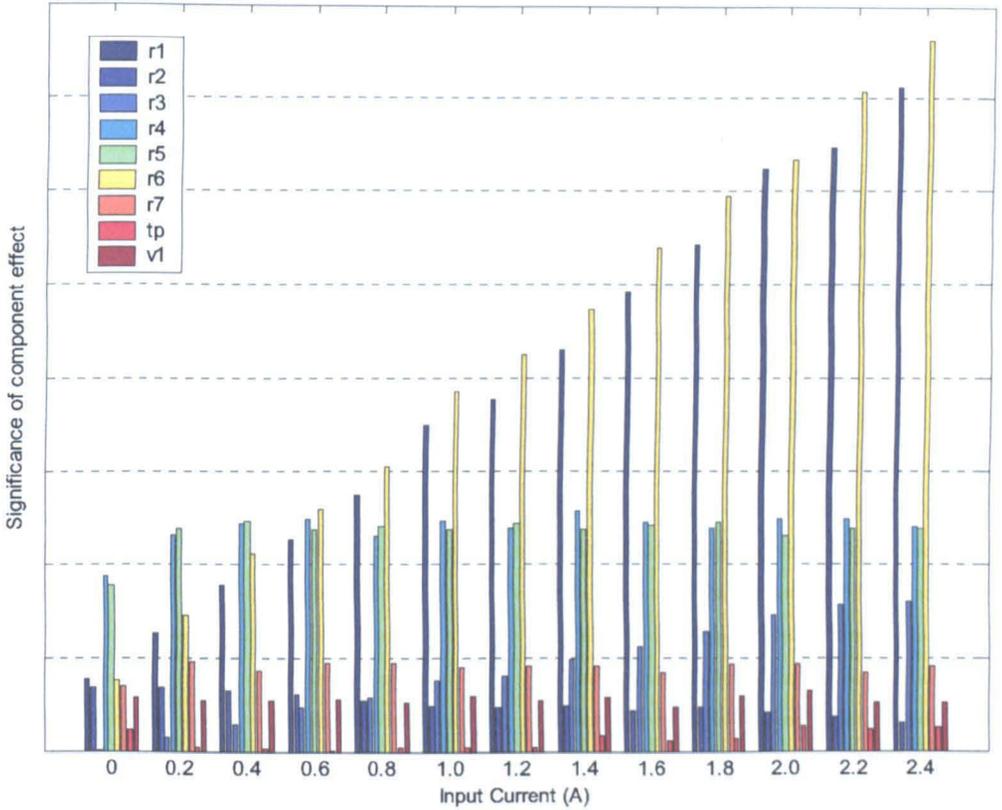
### 9.1.5.3 1.6A



### 9.1.5.4 2.4A



### 9.1.6 Alternative Presentation of Results



**Figure 9-6 Histogram Showing the Increasing Significance of Parametric Variation Within R1 and R6 as Current Increases**

Figure 9-6 gives an alternative presentation of the results showing the relative significance of parametric variation within the circuit upon the circuits output voltage. Each group of bars is plotted to the same scale and a large bar represents a greater influence by a particular controlling factor. Note that the influence of all controlling factors remains constant except for the influence exerted by r1 and r6, which increases with input current.

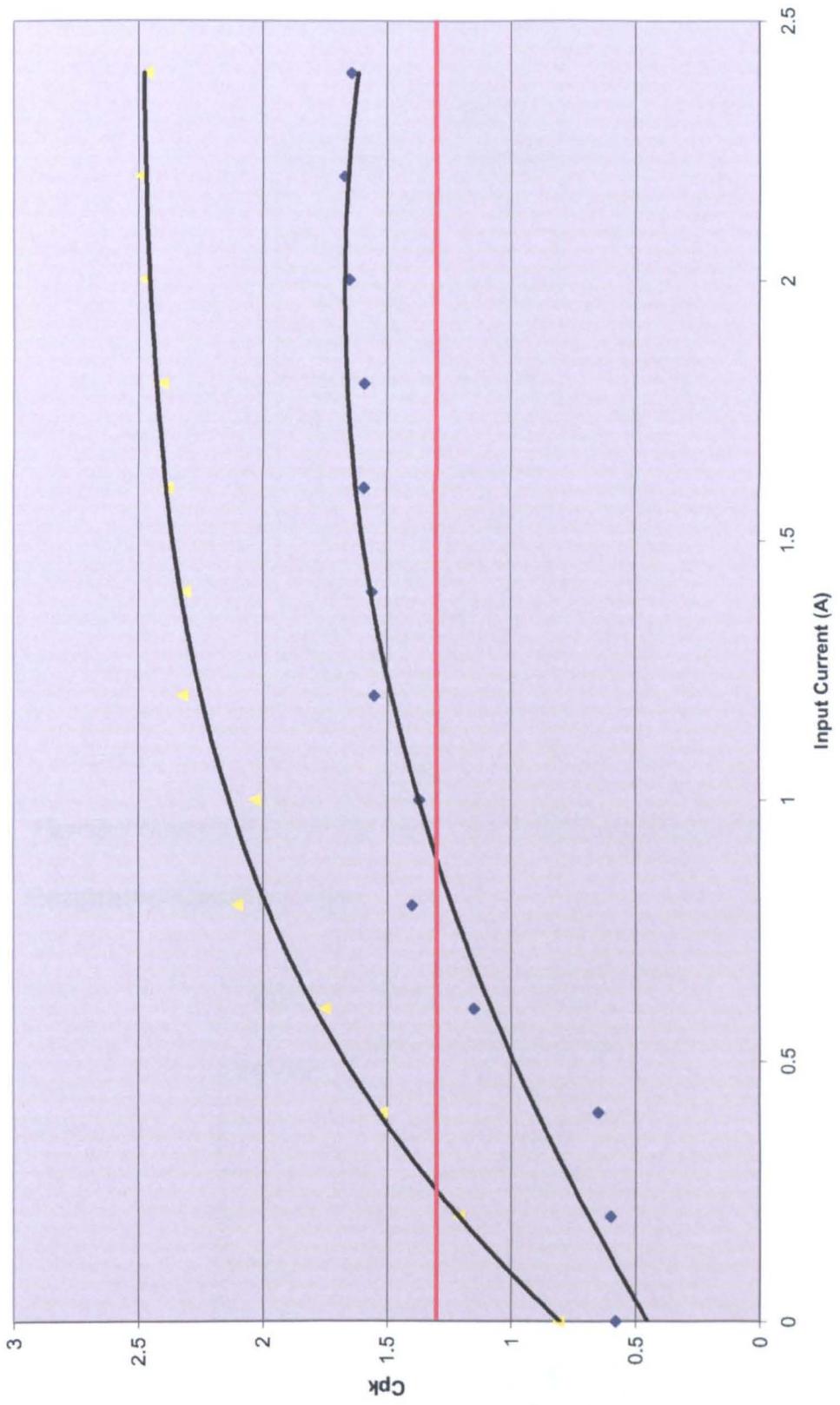


Figure 9-7 Scatter Plot with Trend Lines Showing Current Against  $C_{PK}$  the Yellow Dots Represent the Capabilities with 15% Specification Limits Blue for the 10% Limits (Red Line Indicates a  $C_{PK}=1.33$ )

### 9.1.7 Capability summary for 1% components

	10%	
<i>Current</i>	<i>C<sub>PK</sub></i>	<i>DPMO</i>
0.0	1.75	0
0.2	2.56	0
0.4	3.38	0
0.6	3.89	0
0.8	4.21	0
1.0	4.38	0
1.2	4.53	0
1.4	4.69	0
1.6	5.01	0
1.8	5.20	0
2.0	4.87	0
2.2	5.16	0
2.4	4.99	0

Figure 9-8 Summary of Circuit Capability when Modelled using 1% Components

### 9.1.8 Estimated Quality Costs

<i>DPMO</i>	<i>51200</i>	<i>7419</i>
<i>Severity</i>	<i>Estimated Cost (%)</i>	<i>Estimated Cost (%)</i>
1	0.005	0.0007
2	0.05	0.007
3	0.5	0.07
4	5	0.7
5	>10	7
>6	>10	>10

Figure 9-9 Estimated Quality Costs (% of Product Cost)

### **9.1.9 Discussion of Results**

This conformability analysis has shown that despite the lack of variation in the matched transistor characteristics the model predicts that for low input currents the circuit is not capable, with a predicted capability of only 0.58 with 10% tolerance limits and 0.81 with 15% limits; the predicted capability of the circuit increases with increased current as can be seen from Figure 9-5 and Figure 9-1.

However this estimation of circuit capability should be regarded with caution. Firstly due to the already noted points that the resistors in use in the model have tolerance limits set at 4% and that the Monte Carlo engine in use by SABER is likely to produce component values outside the expected range, and secondly as several of the resistors in use are part of an array it is likely that better value matching will be achieved than that represented within the model. Further to this examination of the capability breakdowns given in sections 9.1.5 to 9.1.5.4 shows that there is considerable scope for improvement of the circuit should the tolerance band of each component be reduced. As the initial simulation modelled the circuit with resistor tolerance bands set to 4% to estimate the effects of component degradation with age it is worth re-examining the results to consider the performance of the circuit taking into account the nominal tolerance band of 1%. The effect of this change was explored in a further analysis and the results are given in Figure 9-8. These results show that the capability of the circuit is significantly higher than when using resistor tolerances of 4%, as shown in Figure 9-5. Note should also be made of the potential costs of these failures, estimated quality costs based upon the analysis of the circuit employing 4% tolerances can be seen in Figure 9-9, for failure severities greater than 4 (10% limits) and 5 (15% limits) the associated failure costs are unacceptable.

### **9.1.10 Conclusion**

Assuming that all components are within their expected tolerance range when initially constructed and that transistor matching is good the circuit will be highly capable, perhaps even overly so. However, when component aging is taken into account the circuit becomes less capable particularly when monitoring low currents with an estimated failure rate for older circuits of 5%. This estimate is however conservative and the actual failure rate due to component aging should be somewhat less than this. Further to this additional analysis is required to understand and model the operation of the double transistor device, the lack of understanding associated with this device was highlighted through the application of *eCA* to this circuit and appropriate actions were taken. The analysis also provided a basis for discussions with the suppliers of the double transistor device with the aim of forcing the suppliers to provide accurate models of the transistor behaviour.

## 9.2 Microprocessor Intelligent Monitor

This section discusses the analysis of a circuit designed to act as a microprocessor Intelligent Monitor (IM). The IM is a mixed signal circuit designed to detect microprocessor faults, such as lockups and crashes, and upon detection reset the system to a known state; this analysis was carried out to determine if the circuit could cause the microprocessor to be reset without cause. As a result of its intelligent monitoring function the circuit performs a safety critical function for the system it is associated with. This case study demonstrates the power of the functional capability analysis module for the reduction of process variability and hence any associated quality costs.

### 9.2.1 Introduction

A schematic diagram of the intelligent monitor is given below and the system operation is as follows: the digital output from the microprocessor is passed through a double integrator circuit which converts the series of 1's and 0's into an analogue voltage. The analogue voltage is then processed in two separate ways. Firstly it is fed back into the microprocessor and digitised, the resulting digital signal is then level compared within the microprocessor and should it be too low a 1 is output from the digital output. If it is too high a 0 is output. Secondly the signal is fed into a window comparator. Should the voltage fall outside the range of acceptable voltages a logical one is produced by the subsequent OR gate and this causes the microprocessor to be reset. This system has the potential to detect two different microprocessor faults:

- A complete crash causing the digital output to stick at one logic level
- A slow response time will cause the microprocessor to fail to control the digital output with sufficient speed

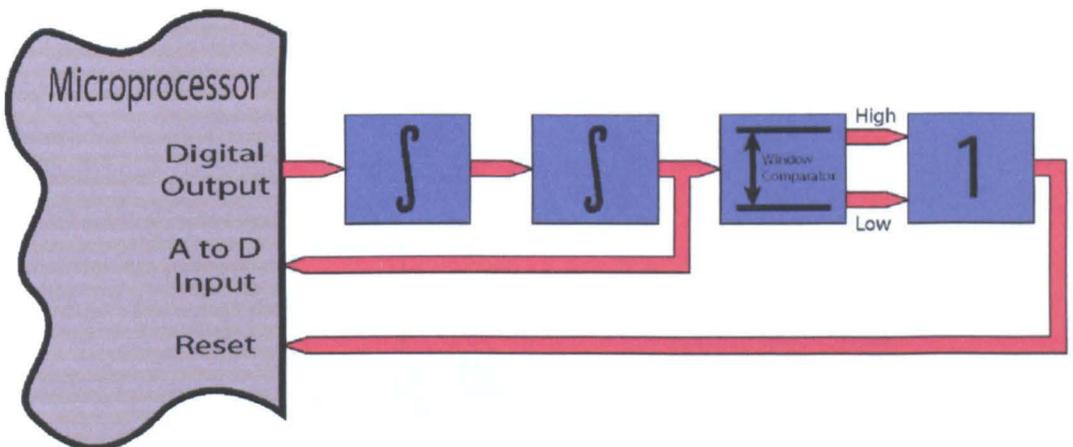


Figure 9-10 Schematic Diagram of Intelligent Monitor Operation

A circuit diagram showing the double integrator, window comparator and OR gate is given in Figure 9-11, it would be possible to model the operation of this circuit in a number of different ways including the use of a commercial circuit simulator such as HSPICE, SABER or Spectre. However, for the purpose of this case study it was determined that the level of detail provided by such a model would be excessive and instead the circuit was modelled using a Simulink macromodel.

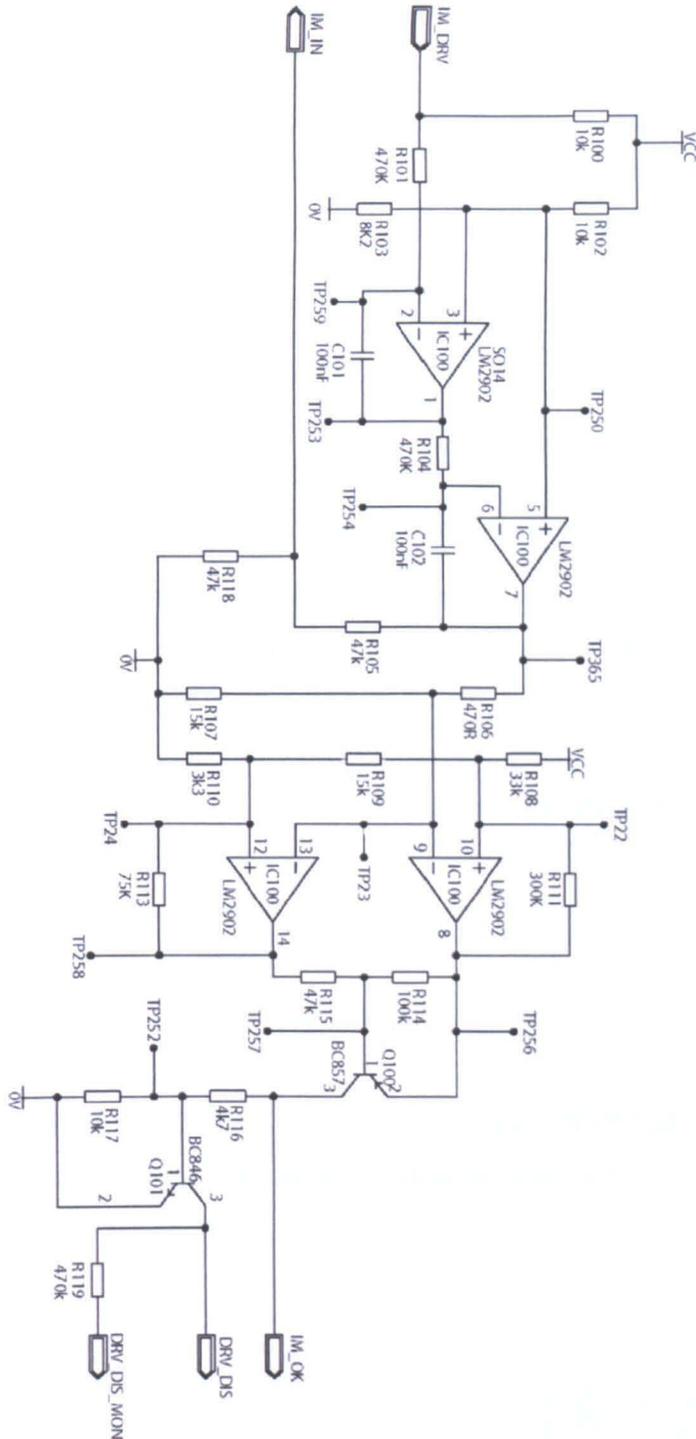


Figure 9-11 Intelligent Monitor Circuit Diagram

<b>Component</b>	<b>Nominal Value</b>	<b>Tolerance</b>
c101	100n F	10%
c102	100n F	10%
r101	560K $\Omega$	1%
r104	470K $\Omega$	1%
r105	47K $\Omega$	5%
r106	470 $\Omega$	5%
r107	15K $\Omega$	5%
r108	33K $\Omega$	1%
r109	15K $\Omega$	1%
r110	3.3K $\Omega$	1%
r111	300K $\Omega$	5%
r113	75K $\Omega$	5%
r118	47K $\Omega$	5%

**Figure 9-12 Intelligent Monitor Circuit Nominal Component Values and Tolerance Limits**

The Simulink model used may be split into three sections:

1. A Matlab script which generates the component values and uses these to derive the voltages and currents controlling the circuit
2. A Simulink model of the intelligent monitor circuitry
3. A Simulink model of microprocessor operations consisting of three subsections:
  - a. A Simulink model of the A to D converter
  - b. A Simulink model of the microprocessor code performing the digital signal comparison
  - c. A Simulink model of Digital Signal controller

The Simulink model is shown below in Figure 9-13, Figure 9-14, Figure 9-15 & Figure 9-16; whilst the parameter generation script is given in Figure 9-17.

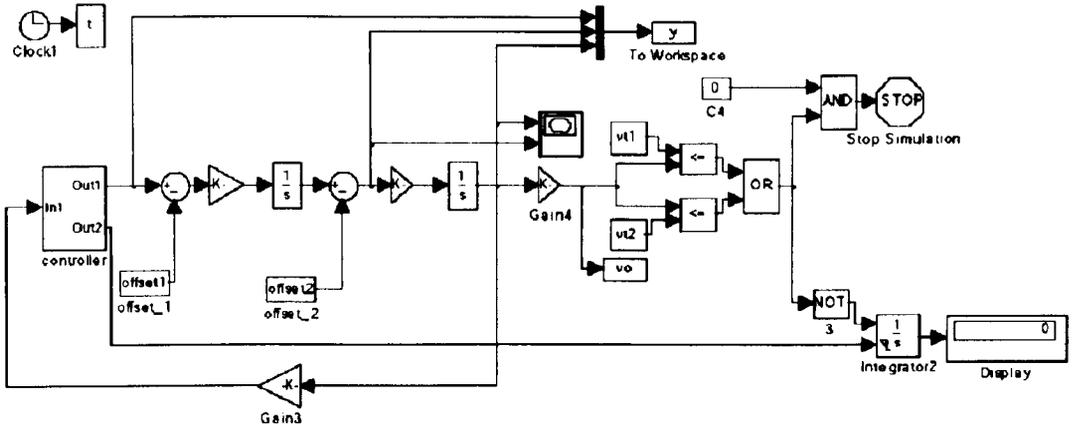


Figure 9-13 Simulink Representation of the IM Circuit

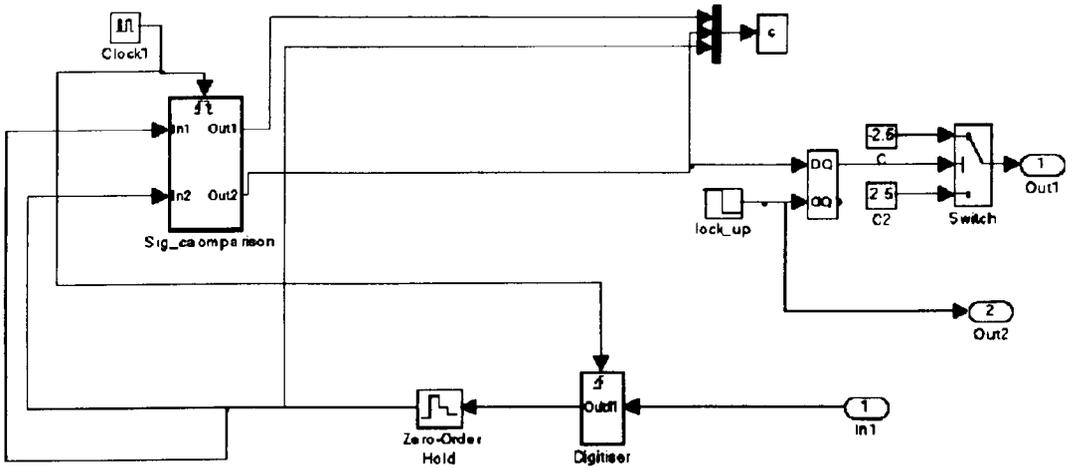


Figure 9-14 Simulink Representation of the Microcontroller Operations

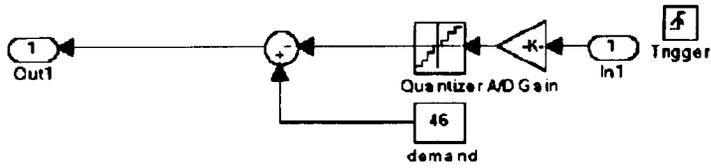
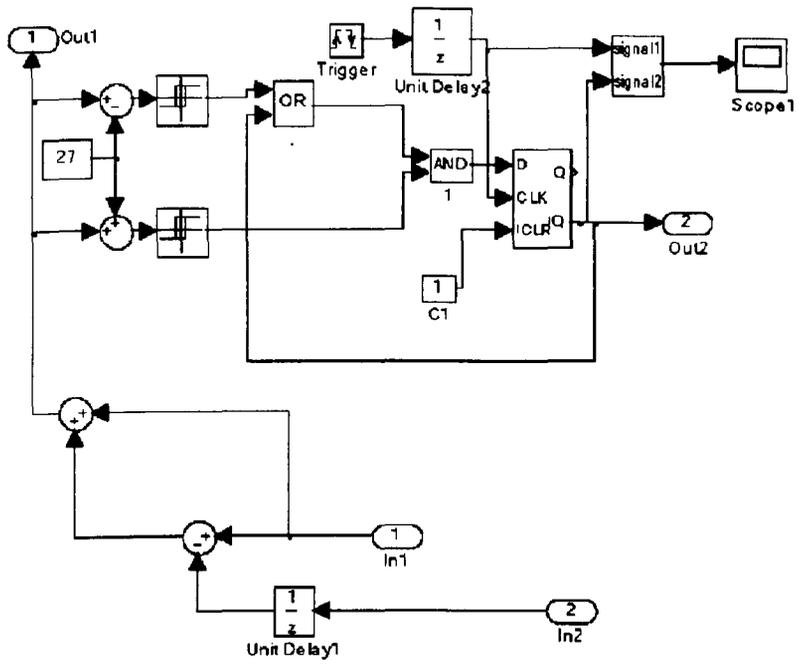


Figure 9-15 Simulink Representation of the A to D Converter



**Figure 9-16 Simulink Representation of the Digital Signal Level Comparison**

```

%GENERATE PASSIVE COMPONNET VALUES
r101=res((470e3),0.01,1,1);
c101=res(100e-9,0.1,1,1);
r104=res(470e3,0.01,1,1);
c102=res(100e-9,0.1,1,1);
r105=res(47e3,0.05,1,1);
r118=res(47e3,0.05,1,1);
r106=res(470,0.05,1,1);
r107=res(15e3,0.05,1,1);
r108=res(33e3,0.01,1,1);
r109=res(15e3,0.01,1,1);
r110=res(3.3e3,0.01,1,1);
r111=res(300e3,0.05,1,1);
r113=res(75e3,0.05,1,1);

%SCHMITT TRIGGER VOLTAGES
vo1=3.6;
vo2=0;

%SUPPLY VOLTAGE
vcc=5;

%INPUT OFFSETS ON INTEGRATORS
input_bias_current_1=normt(0,7.5e-9,-50e-9,50e-9);
input_bias_current_2=normt(0,7.5e-9,-50e-9,50e-9);

```

**Figure 9-17 Circuit Parameter Generation Script**

## 9.2.2 Analysis

The purpose of the analysis carried out was to determine whether the monitor circuit would cause the microprocessor to reset in the absence any defect due to the statistical variation in component parameters.

For the purpose of the analysis two metrics where defined,  $V_{bl}$  and  $V_{bh}$  these are calculated as shown below:

- $V_{bl} = V_{omin} - V_{wl}$
- $V_{bh} = V_{wu} - V_{omax}$

Where  $V_{omin}$  – min o/p voltage of the double integrator

$V_{wl}$  – lower threshold of the window comparator

$V_{wu}$  - upper threshold of the window comparator

$V_{omax}$  – max o/p voltage of the double integrator

Associated with these metrics are specification limits as given below:

	LSL	USL
$V_{bl}$	0	INF
$V_{bh}$	0	INF

Functional Conformability analysis was carried out on the IM system using MC analysis applied to the Simulink model. The statistical simulation is simple and fast to carry out, consisting of calling the parameter generation script  $n$  times and for each of the  $n$  samples running the Simulink model.

### 9.2.3 Results

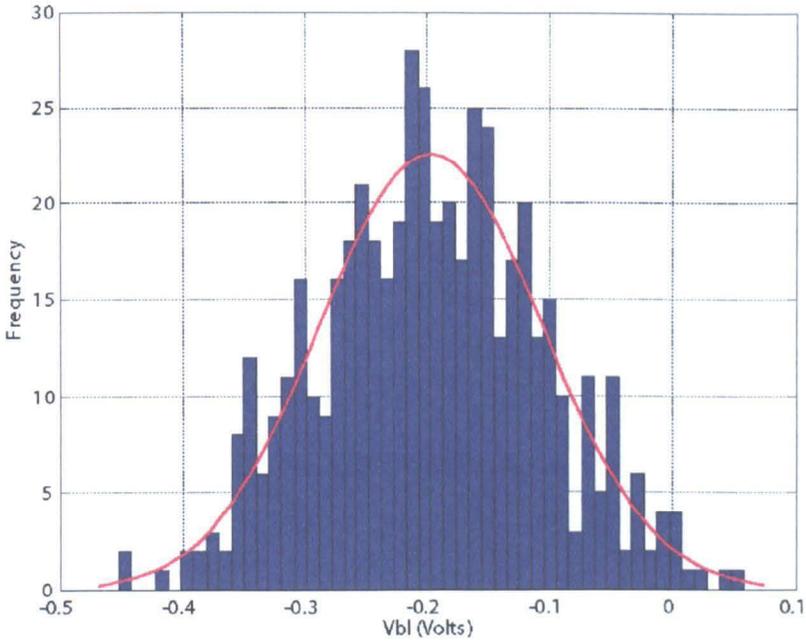


Figure 9-18 Distribution of Vbl for the Specified Component Values and Controller Settings

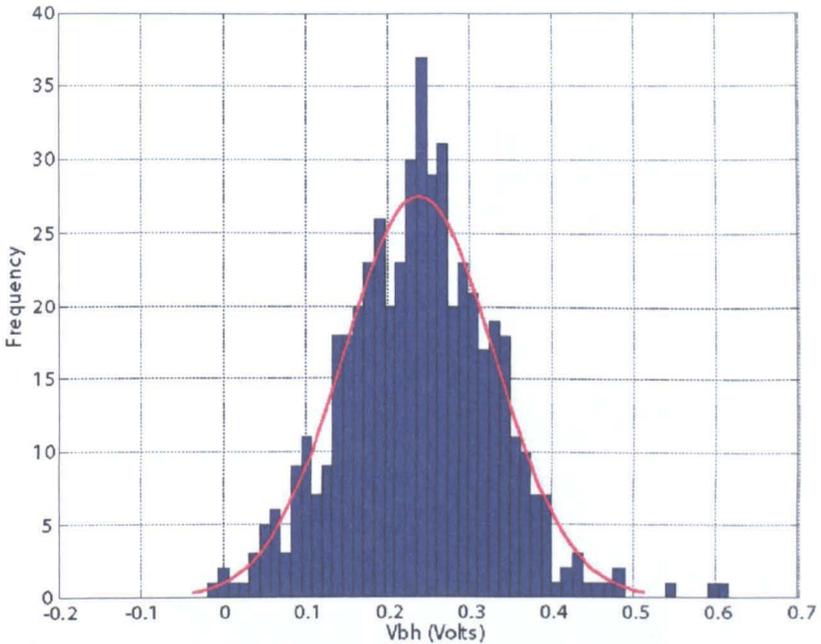
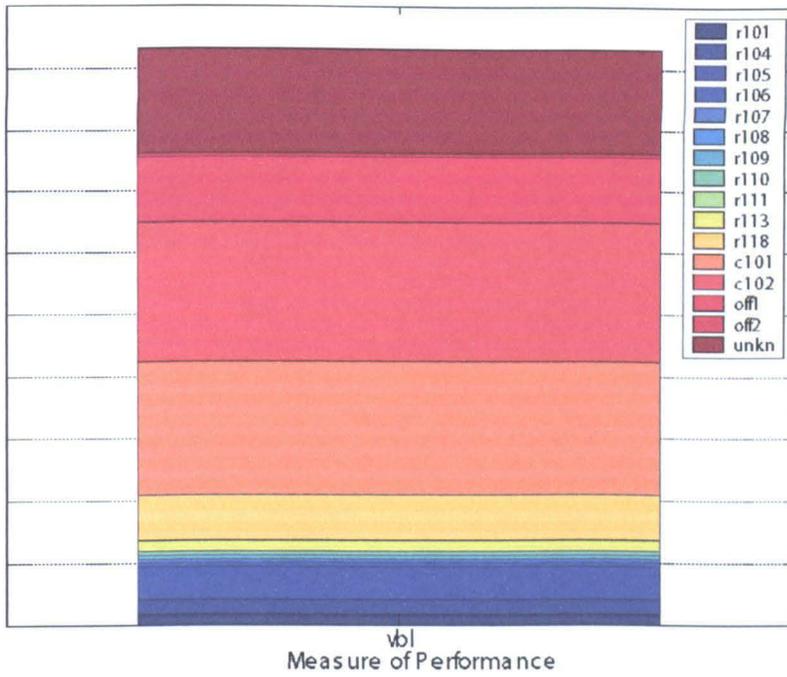
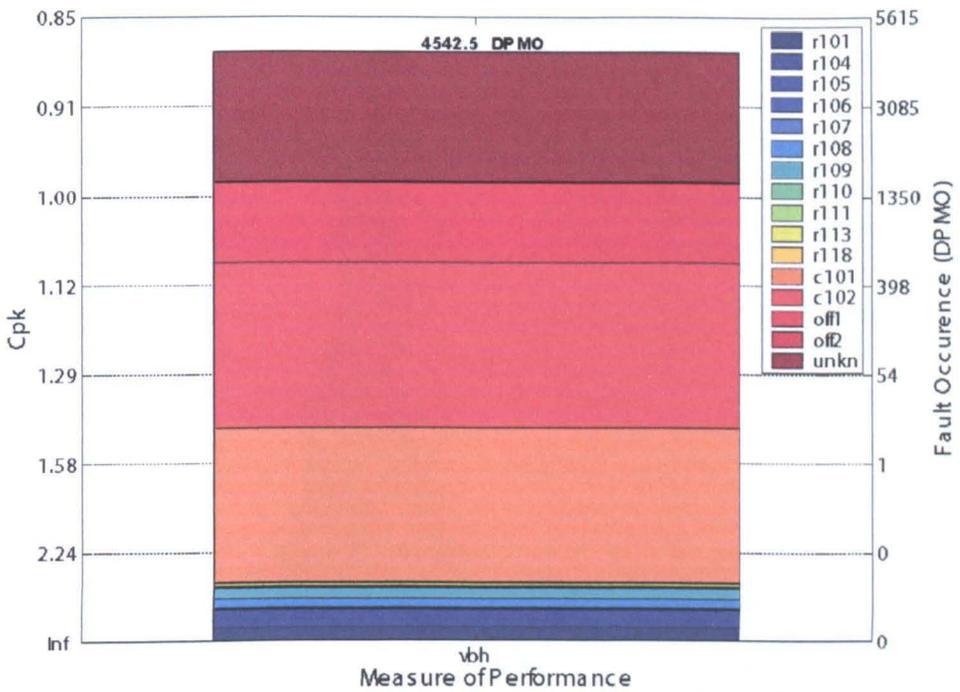


Figure 9-19 Distribution of Vbh for the Specified Component Values and Controller Settings

Figure 9-18 & Figure 9-19 show histograms of Vbl and Vbh for the circuit in its original configuration. It is at once obvious from these histograms that the circuit is not at all capable with respect to Vbl and is reasonably capable with regard to Vbh. The capability breakdowns associated with these distributions are given below in Figure 9-20 and Figure 9-21.



**Figure 9-20 Capability Breakdown for Vbl, Note the Lack of Scale This Due to the Fact That the Mean of the Distribution Lies Outside the Specification Limits and Hence the Product is Not Capable with Respect to this performance Aspect**



**Figure 9-21 Capability Breakdown for Vbh**

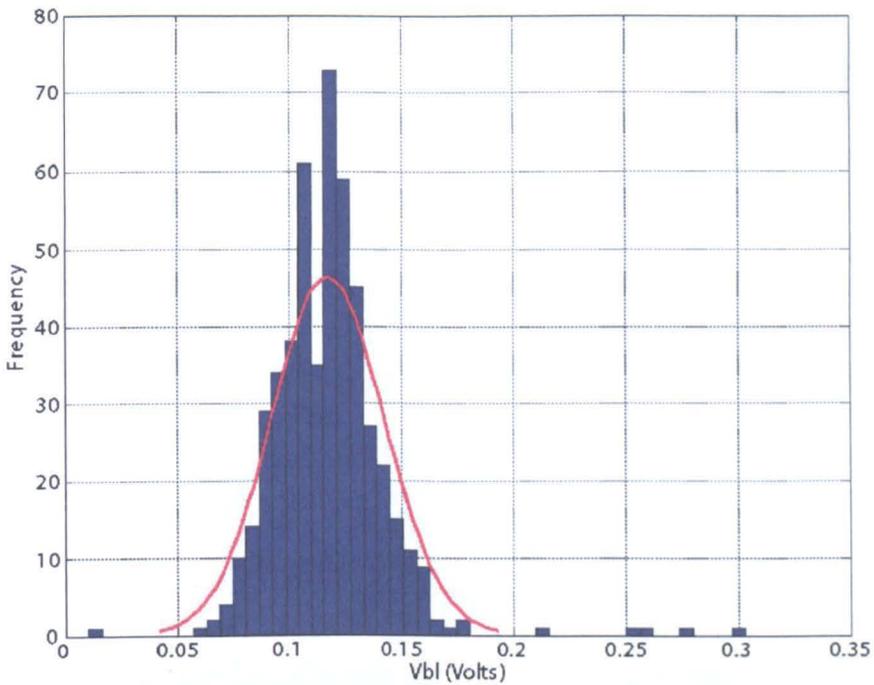
Following the application of the functional analysis module and production of the two capability breakdowns shown above the data generated was fed forward through the eCA analysis framework to the cost estimation module. As a result of the poor level of capability associated with the original design and the safety critical nature of this

product the estimated quality costs at this stage where alarmingly high as shown below in Figure 9-22.

Performance Metric	Defect	Conformance Area			
		Functional			
		Cpk	DPMO	Impact	Cost (%)
Vbl	NA	0.00	1000000.00	8.00	1000000.00
Vbh	NA	0.87	4542.00	8.00	4542.00

**Figure 9-22 Quality Cost Summary for the Original EPB IM Circuit**

Following this initial assessment of the circuit functionality it was decided that the first aspect of the design that should be addressed was the complete incapability of the design with regard to Vbl. Improvement here was obtained by by increasing the gain of the double integrator stage of the circuit. This may be achieved by increasing the size of resistors R101 and R104 by 20%. The success of this strategy is confirmed below by the histograms given in Figure 9-23 and Figure 9-24. It is at once obvious that both the voltage frequency distributions have been shifted positively such that Vbl no longer leaves the acceptable region as defined by the window comparator.



**Figure 9-23 The Distribution of Vbl for the Modified Circuit**

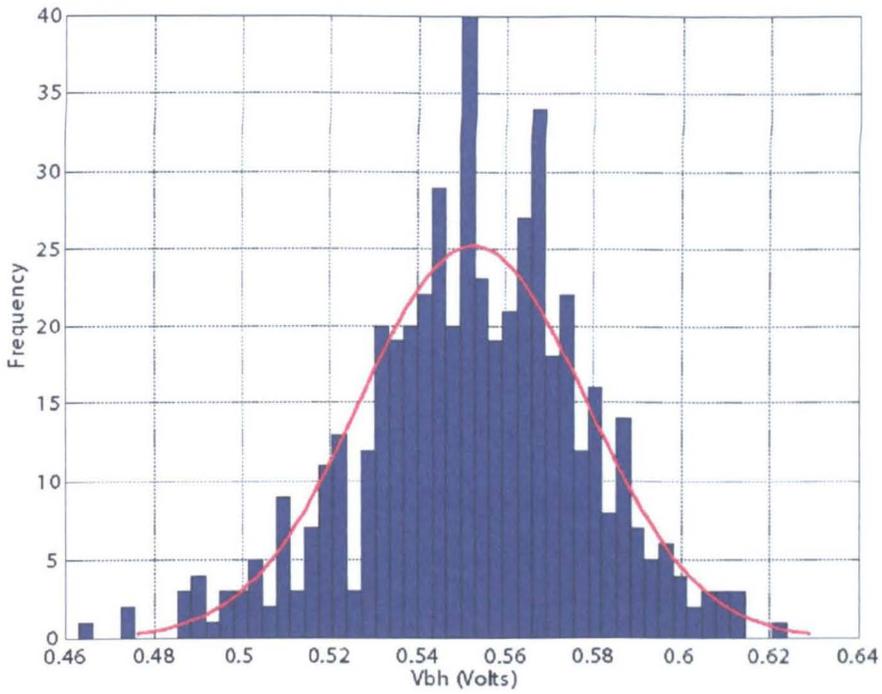


Figure 9-24 The Distribution of vbh for the Modified Circuit

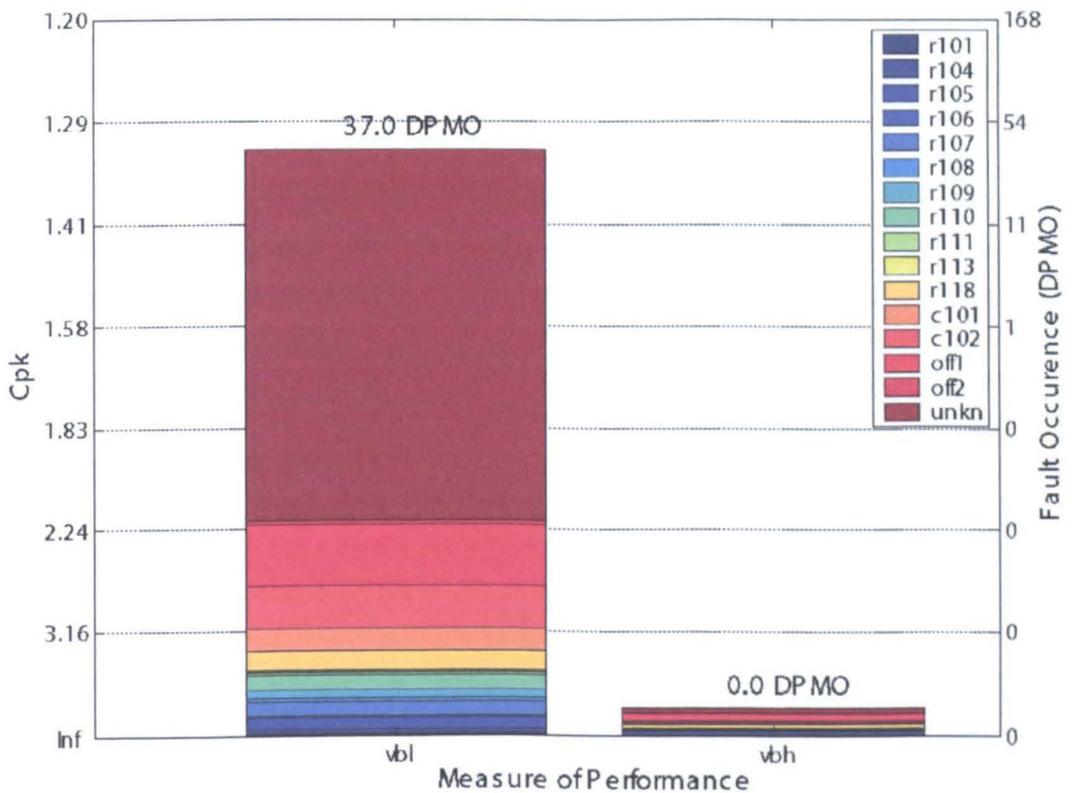


Figure 9-25 Capability Breakdown for the Modified Circuit

Figure 9-25 shows the capability breakdown for the modified circuit. Note the considerable improvement in circuit performance indicated by the significantly reduced defect occurrence rate for both Vbh and Vbl.

This improvement is illustrated by the dramatic reduction in quality costs associated with the circuit as shown in Figure 9-26.

Performance Metric	Defect	Conformance Area			
		Functional			
		Cpk	DPMO	Impact	Cost (%)
Vbl	NA	1.32	37.00	8.00	37.00
Vbh	NA	1.80	0.00	8.00	0.00

**Figure 9-26 Quality Cost Summary for the EPB IM Circuit Following Initial Modifications**

However the level of capability and hence the associated defect rate and quality costs associated with Vbl are still unacceptable. The largest explained contributing factor to the performance of the circuit with respect to Vbl is the offset current of the first integrator. However due to cost considerations we are unable to change the device to a higher performance device which would exhibit a lower offset current. As the option to change the first integrator is unacceptable we must instead reduce the tolerance band of the next most significant devices C101 and C102, currently these are set to 10% they may however be replace with 5% device without significant component cost increases. The effect of this change (option 1) is shown in Figure 9-27. The capability level of both Vbl and Vbh have been further improved. However this improvement does increase the component cost of the circuit by a small amount, an alternative option (option 2) is to reduce the influence of the integrator offset current by increasing the nominal value of the capacitors in the circuit; the result of this change is illustrated in Figure 9-28. A comparison of the quality costs associated with the circuit with respect to the two capacitor related circuit improvements is given in Figure 9-29.

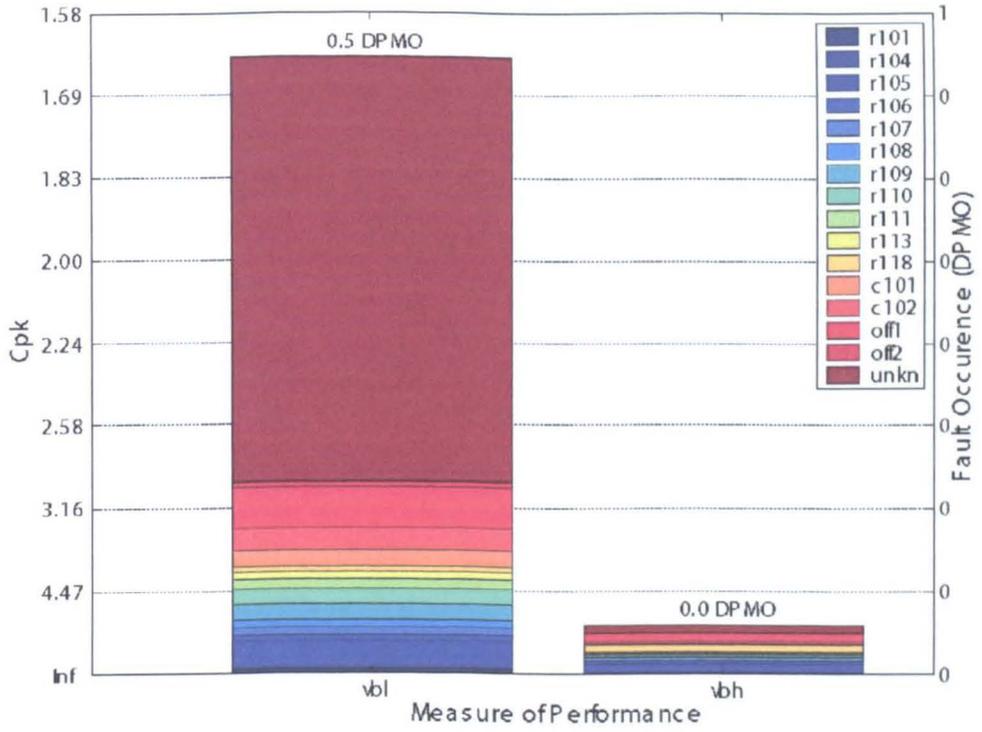


Figure 9-27 Capability Breakdown for the Circuit with Modified Capacitor Tolerance Bands

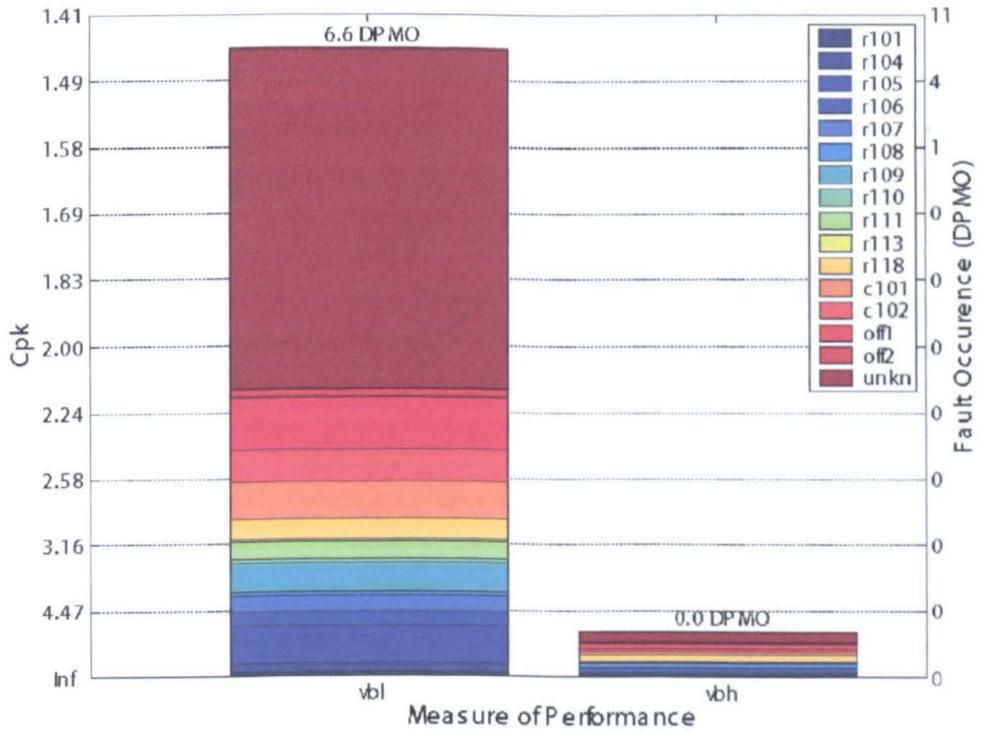


Figure 9-28 Capability Breakdown for the Circuit with Modified Nominal Capacitor Values

	Performance Metric	Defect	Conformance Area			
			Functional			
			Cpk	DPMO	Impact	Cost (%)
Option 1	Vbl	NA	1.63	0.50	8.00	0.50
	Vbh	NA	1.80	0.00	8.00	0.00
Option 2	Vbl	NA	1.45	6.60	8.00	6.60
	Vbh	NA	1.80	0.00	8.00	0.00

Figure 9-29 Comparison of the Quality Costs for the Two Capacitor Related Circuit Improvements

### 9.2.4 Conclusions

This case study has shown the effectiveness of the analysis procedure in indicating the significance of the effect of parameter variations whilst showing which tolerance should be tightened in order to improve capability. It has also illustrated the weakness of the technique in that it does not indicate whether a change to the nominal value of the parameter might also improve capability. Hence it is necessary that the circuit designer properly understand the operation of the circuit in question. This is illustrated by the effect on the circuit due to the change in nominal values of R101 and R104 and also the increased level of capability achieved through the change to the nominal values of C101 and C102 by 20% since this reduces the effect of the input offset currents on the operational amplifiers. As a result of this analysis the circuit implementation was changed such that the nominal values of resistors R101 and R104 and capacitors C101 and C102 were increased by 20%.

### 9.3 Automotive Sensor Signal Conditioning Circuit

The following section describes the application of *eCA* to an automotive sensor signal conditioning circuit. The intended function of this circuit is to convert the noisy sine wave signal generated by the magnetic sensor associated with the circuit into a square wave of an equivalent frequency, suitable for input into a digital component. The particular focus of this analysis was the estimation of the cost of quality associated with the proposed testing procedure.

#### 9.3.1 Functional Model Description

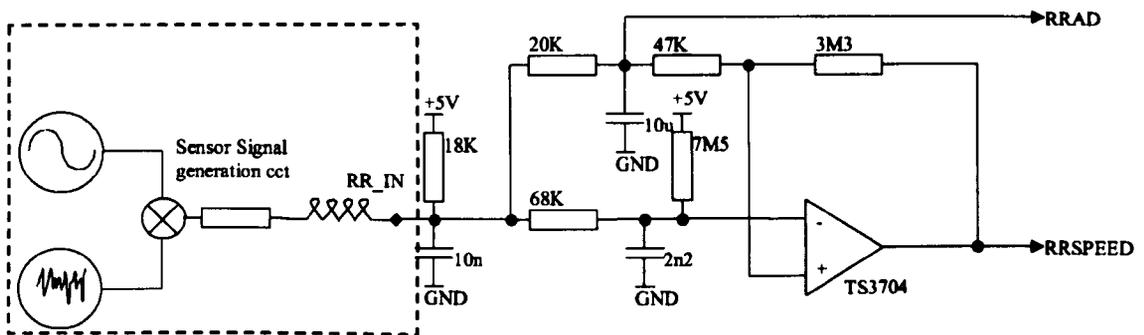


Figure 9-30 Circuit Diagram Showing the Functional Model of the Signal Conditioning Circuit

The functional model of the circuit was created in HSPICE and two different version were used during the course of this analysis. The basic form of the model is shown in Figure 9-30 and it may be divided into two discrete units as described below:

- A model of the sensing elements (highlighted in Figure 9-30 by the dashed box)
- A model of the signal conditioning elements

The sensor model is designed to accurately simulate the real sensor. It contains 5 elements, a sine wave generator, a noise source, a mixing unit, a resistor and an inductor. These are linked as shown in Figure 9-30, the mixer takes the form of an ideal voltage controlled voltage source and uses a polynomial equation of the form  $V_3 = A \cdot V_1 + B \cdot V_2$  to control the output voltage. Hence, the signal to noise ratio can easily be controlled. For the purposes of the functional analysis stage of *eCA* the model was configured as shown with the output from this sensor model used as the stimulus for the signal conditioning circuit as shown in Figure 9-30. In the case of testability analysis stage the sine generator was replaced by a square wave generator, and the resistive and inductive elements removed.

The circuit operation was simulated using a transient analysis, over the period of the analysis the operation of the circuit is monitored using several measure statements as detailed in section 14.1.1. Figure 14-3 shows the component numbering scheme used throughout the analysis.

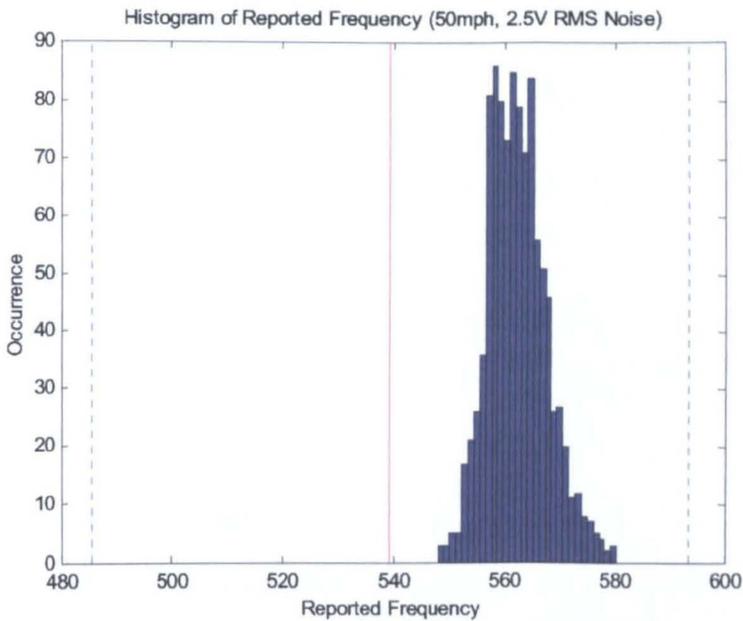
### 9.3.2 Functional Capability

For the purposes of this case study the functional analysis took into account not only the parametric variations associated with each of the circuit components but also the noise associated with the sensing elements of the system.

### 9.3.3 Method

The basis of this analysis is a set of Monte Carlo simulations of the circuit with each sample having a set of component values randomly selected from the range of possible values and an input signal which is representative of the sensor signal at a given speed with additive noise of a set RMS amplitude. The variation in the reported frequency is then compared with the specification limits ( $\pm 10\%$  of the nominal frequency) to calculate the capability of the circuit.

### 9.3.4 Results



**Figure 9-31 Histogram of a Typical Set of Results**

Figure 9-31 shows a typical set of results together with the ideal frequency for that set of results (solid red line) and the specification limits used for the calculation of capability (dashed blue lines). In this case it can be seen that the noise associated with

the sensor signal has caused extra counts to occur, causing the distribution of reported frequencies to be shifted upwards. The results of this functional analysis are given in the conformability matrix shown in Figure 9-34, however the analysis may be summarised sufficiently by noting that the circuit is particularly capable with a value of  $C_{PK} > 2$ .

### **9.3.5 Test Capability**

For the purpose of this analysis only short and open faults across the passive components were considered. Occurrence rates for these defects were not available so no manufacturing analysis was attempted.

### **9.3.6 Method**

First the netlists for the faulty circuits were prepared by altering the original netlist. Shorts were represented by placing a low value resistor (1 ohm) between the nodes to be shorted and opens by simply removing the component in question. After preparing the defective netlists, each version of the circuit (19 in total) was simulated using a 100Hz 5V square wave input signal with 1 volt RMS noise and the 18 defective circuits compared to the defect free circuit. The results from each faulted circuit were examined to assess if they could be discriminated from the defect free circuit using the proposed test. For the majority of faults the behaviour of the circuit was predictable and independent of component parameter values. Several faults resulted in behaviour, which was dependent upon parametric variation. These were simulated using Monte Carlo analysis to allow an estimate of the occurrence of test errors to be calculated; in each case the test limits (90 and 110 Hz) specified in the supplied test specification were used.

### **9.3.7 Fault Free Circuit**

With the specified test the occurrence of Type I errors is 0. This is not unexpected as the test signal applied to the circuit is of a much larger amplitude with respectively less significant noise than the real input signal.

### **9.3.8 Initial Analysis – Fault Screening**

Based upon the small sample simulations of the faulty circuits the results in Figure 9-33 were produced. Example waveforms can be found in section 14.1.2.

### 9.3.9 Further Analysis of Probabilistic Faults

Based upon the Monte Carlo screening simulations of the faults which are dependent upon parameter values, the predicted occurrence of Type II test errors are given in Figure 9-32.

Component	Fault	Type II Error Occurrence(PPM)
R858	Open	0
R859	Short	0
R860	Short	885702
C807	Short	888340

**Figure 9-32 Type II Test Error Occurrence**

This indicates that the test is in fact capable of detecting an open on R858 and a short on R859, but is very poor at detecting a short on R860 or a short on C807. The costs resulting from these test errors are detailed in the conformability matrix given in Figure 9-34.

Figure 9-33 Summary of the Test Screening Results

<i>Component</i>	<i>Fault type</i>	<i>Typical Output Frequency (Hz)</i>	<i>Comments</i>	<i>Detectable ?</i>	<i>Effect of Noise</i>
R858	Short	0	TP378 follows 1V triangle wave on TP270 with offset of approx 50mV so op amp inputs never cross	Yes	None
	Open	45	TP270 remains approx 0V but RRSPEED produces spike whenever RR_HI crosses zero. For particular noise amplitude & frequency could get in spec output frequency	Yes	Small count when noise forces input above threshold
R859	Short	104	Removes the hysteresis of the circuit and causes too many pulses due to the effects of noise.	Maybe	Small over count
	Open	0	TP376 and RRSPEED are stuck at 5v, no pulses are produced despite TP378 rising above 5v	Yes	None
R860	Short	104	Removes the hysteresis of the circuit and causes too many pulses due to the effects of noise.	Maybe	Small over count
	Open	0	Stuck at 5v	Yes	Small over count
R861	Short	0	Stuck at 5v	Yes	None
	Open	100	RRSPEED is as expected for an un faulted circuit	No	None
R862	Short	123	Reduces the noise filtering ability of the circuit causing too many pulses to be generated	Yes	Over count
	Open	0	Once the voltages at TP378 and TP376 cross over the output sticks at 0v	Yes	None
R863	Short	20	Stuck at 0v	Yes	None
	Open	100	RRSPEED is as expected for an un faulted circuit	No	None
C807	Short	20	Produces hysteresis around 0v, an output pulse is generated whenever the noise on the signal forces TP378 below 0v	Yes	Counts when noise forces input below 0v
	Open	2Khz	TP376 follows the input signal	Yes	Causes Massive Over count
C808	Short	0	Stuck at 5v	Yes	None
	Open	100	RRSPEED is as expected for an un faulted circuit	No	None
C809	Short	0	Stuck at 5v	Yes	None
	Open	100	RRSPEED is as expected for an un faulted circuit	No	None

Performance Metric	Defect	Conformance Area															
		Functional				Manufacture				Test (Type I)				Test (Type II)			
		Cpk	DPMO	Impact	Cost (%)	Cpk	DPMO	Impact	Cost (%)	Cpk	PPM	Impact	Cost (%)	Cpk	PPM	Impact	Cost (%)
Signal Conversion at 2 mph	NA	>2	0.00	5.00	0.00												
Signal Conversion at 10 mph	NA	>2	0.00	5.00	0.00												
Signal Conversion at 20 mph	NA	>2	0.00	5.00	0.00												
Signal Conversion at 30 mph	NA	>2	0.00	5.00	0.00												
Signal Conversion at 40 mph	NA	>2	0.00	5.00	0.00												
Signal Conversion at 50 mph	NA	>2	0.00	5.00	0.00												
R858	Short													5.00	0.00	5.00	0.00
R858	Open													5.00	0.00	5.00	0.00
R859	Short													5.00	0.00	5.00	0.00
R859	Open													5.00	0.00	5.00	0.00
R860	Short													5.00	0.00	5.00	0.00
R860	Open													0.00	885702.00	5.00	885.70
R861	Short													5.00	0.00	5.00	0.00
R861	Open													0.00	1000000.00	5.00	1000.00
R862	Short													5.00	0.00	5.00	0.00
R862	Open													5.00	0.00	5.00	0.00
R863	Short													5.00	0.00	5.00	0.00
R863	Open													0.00	1000000.00	5.00	1000.00
C807	Short													0.00	888340.00	5.00	888.34
C807	Open													5.00	0.00	5.00	0.00
C808	Short													5.00	0.00	5.00	0.00
C808	Open													0.00	1000000.00	5.00	1000.00
C809	Short													5.00	0.00	5.00	0.00
C809	Open													0.00	1000000.00	5.00	1000.00

Figure 9-34 Conformance Matrix

	Conformance Area				
	Functional	Manufacturing	Test (Type I)	Test (Type II)	Test (ALL)
Total DPMO / PPM	0.00	NA	0.00	5774042.00	5774042.00
Representative Capability	5.00	NA	5.00	0.00	0.00
Total Associated Cost (% unit cost)	0.00	NA	0.00	>100	>100

Figure 9-35 Quality Cost Summary

### 9.3.10 Conclusions

From the data contained in the summary matrix presented in Figure 9-35 we can see that there is no cause for concern associated with the functional capability of the circuit. However the test capability analysis shows that there are potentially large quality costs associated with the proposed test method. that the proposed test is not capable of detecting the absence of R861, R863, C808 or C809 and will only detect a short on R860 or a short on C807 in approximately 11% of cases.

It would thus be appropriate to consider further testing directed at identifying these faults. The cost effectiveness of such testing would depend upon the probability of these faults occurring. Further investigation would be appropriate into the effect of differing signal and noise levels on the test signal and on potential faults other than shorts & opens on the passive components.

## **9.4 Torque and Angle Sensor**

This section describes the application of *eCA* to the Electric Power Steering (EPS) Torque and Angle Sensor. The analysis of the generation 1 (Gen. 1) sensor was performed as part of a green belt project to help verify the use of the *eCA* technique upon this complicated electro mechanical system. An overview of the torque sensor concept is provided in Appendix D. It should be noted that due to commercial considerations the level of detail presented in this section has been limited, for example actual costs have been omitted.

### **9.4.1 Introduction**

The Gen.1 sensor analysis was performed as part of a green belt project and demonstrates the application of the *eCA* process within the DMAIC framework. In this situation the DMAIC framework provides the support required by the *eCA* technique in terms of basic problem analysis and data gathering and verification. It also provides a means to ensure that any problems identified by the technique are acted upon. The analysis consisted of an assessment of the manufacturing capability of the sensor to determine the quality costs associated with the variation in the manufacturing processes. A selection of the DMAIC documentation is provided in Appendix E to set the context of this analysis.

### **9.4.2 Modelling Technique**

As the functionality of the torque sensor is dependent upon the spatial positioning of the various sensing elements, it was decided that physical modelling would be the most appropriate method for the assessment of manufacturing capability. Accordingly it was decided to develop and validate an existing geometric model produced for the purposes of algorithm development. The model is Matlab based and represents the passage of light through the sensing elements onto the Linear Array Device (LAD) thereby providing a simulation of sensor operation. The electrical operation of the LAD is modelled by converting the calculated light intensity levels seen at each of the 128 LAD pixels into a corresponding voltage, this voltage is then quantised to simulate the effect of quantisation error at the ECU input.

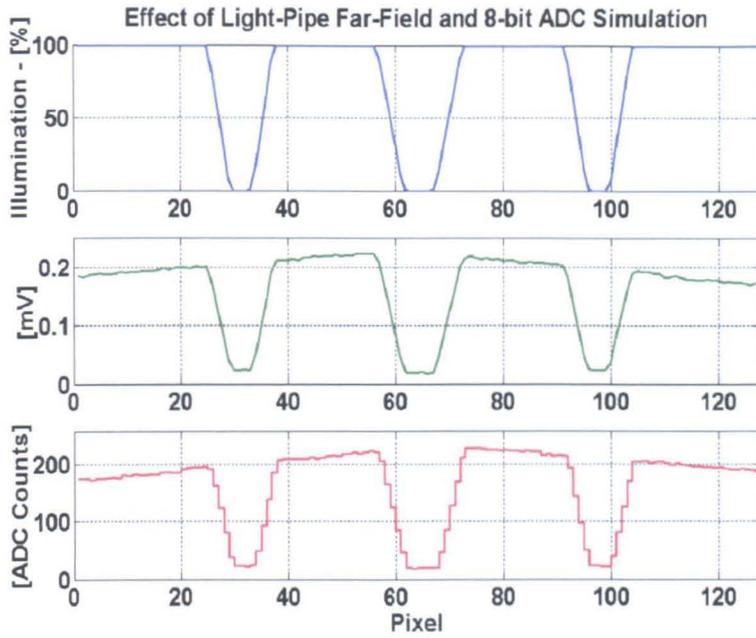


Figure 9-36 LAD and ADC Simulation

This geometric model of the sensor is complemented by a Matlab implementation of the ECU algorithms used to process the electrical signal output by the LAD into a corresponding torque signal.

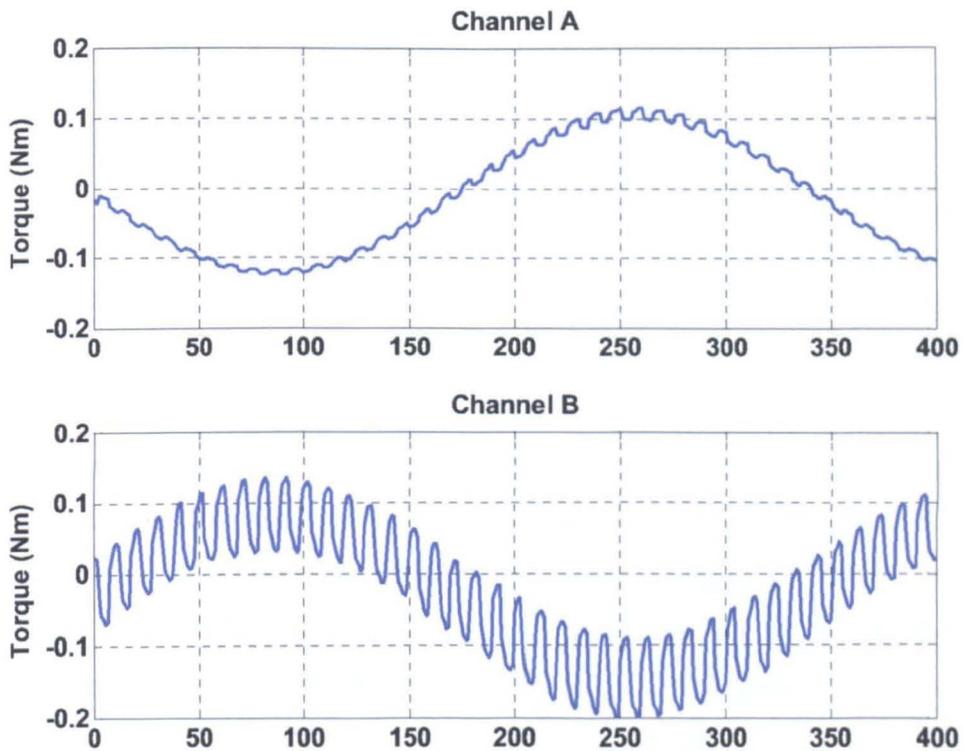


Figure 9-37 Example Channel Torque Signals

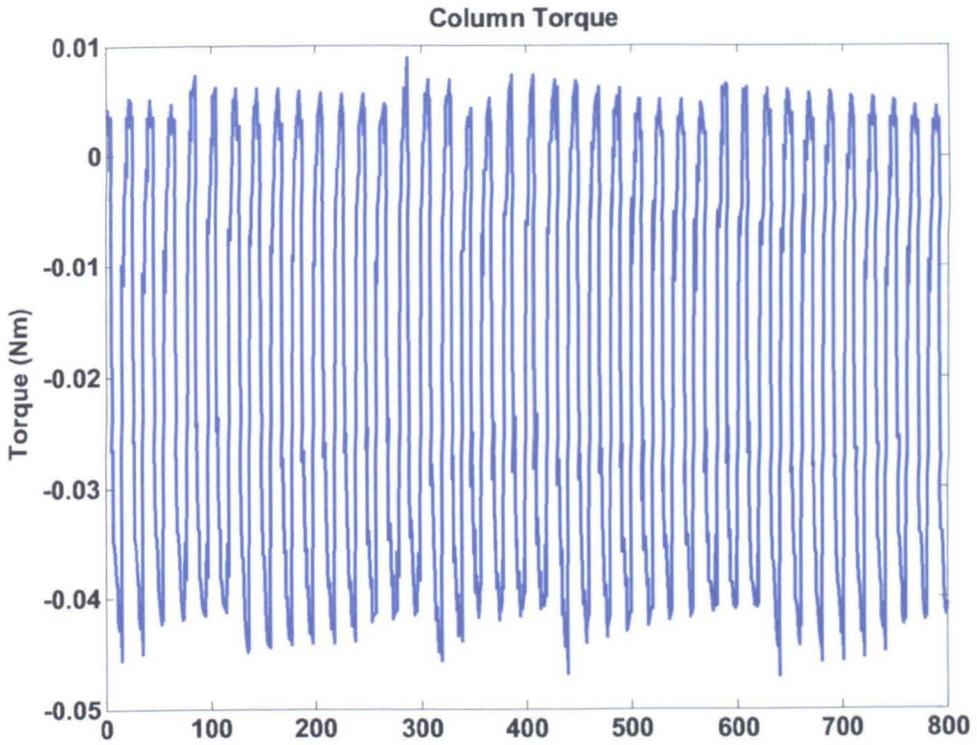


Figure 9-38 Example Column Torque Signal

### 9.4.3 Manufacturing Capability Analysis

The manufacturing capability analysis was completed through the application of a Monte Carlo style statistical analysis to the system using the Matlab model of the sensor. For each sample of the population the geometric position of each sensor component was specified according to an appropriate statistical distribution. Each distribution was specified such that it represented the process performance of the particular manufacturing process used to place that sensor component. At each Monte Carlo analysis point the model was controlled so that the sensor was manipulated in a way similar to that at expected at the end of line test stage of the sensor production process. The simulated sensor data was then processed using the Matlab implementation of the ECU processing algorithms and certain metrics were taken from the data to evaluate the performance of the sensor in a particular configuration.

### 9.4.4 Performance Metrics

For the purpose of this analysis four performance metrics were used:

- Zero Torque Offset – The DC component of the column torque signal, this must be minimised as it reduces the effective range of the sensor
- Channel Torque Runout – The absolute range of a channel torque signal for a shaft rotation with zero torque input. This should be minimised as a large value reduces the effective range of the sensor.
- Column Torque Runout – The absolute range of the column torque signal for a shaft rotation with zero torque input. This should be minimised as a large value reduces the effective range of the sensor.
- High Frequency Torque Ripple – A high frequency component of the column torque signal, this ripple must be minimised as it degrades driver ‘feel’.

### 9.4.5 Results

Performance Metric	Defect	Conformance Area			
		Manufacture			
		Cpk	DPMO	Impact	Cost (%)
Disc Runout	Exceed Limits	0.75	12477.00	3.00	0.12
Channel Torque Runout	Exceed Limits	0.71	16194.00	3.00	0.16
Zero torque Offset	Exceed Limits	0.77	10713.00	3.00	0.11
HF Torque Ripple	Exceed Limits	0.77	10412.00	3.00	0.10

Figure 9-39 Manufacturing Analysis Results

Figure 9-39 gives the basic results of the manufacturing analysis, showing the capability of the manufacturing processes to produce a sensor meeting its specification with respect to each of the performance metrics in use. As the sensor is currently in production a comparison was made between these results and the EOL test yield. This comparison demonstrated the accuracy of the manufacturing defect rate predicted by *eCA*.

An estimate of the quality costs associated with these failures was then made using the conformability analysis matrix, the results of this are given in Figure 9-40, in addition to an estimate of the manufacturing quality costs should a six sigma process be achieved.

Summary Table by Single Area					
	Conformance Area				
	Functional	Manufacturing	Test (Type I)	Test (Type II)	Test (ALL)
Total DPMO / PPM	NA	49796.00	NA	NA	NA
Representative Capability	NA	0.55	NA	NA	NA
Total Associated Cost (%)	NA	0.50	NA	NA	NA

Cumulative Summary Table						
	Conformance Area					6 $\sigma$ Worst Case
	Functional	Manufacturing	Test (Type I)	Test (Type II)	Test (ALL)	
Total DPMO / PPM	NA	49796.00	NA	NA	NA	3.4
Representative Capability	NA	0.55	NA	NA	NA	1.50
Total Associated Cost (%)	NA	0.50	NA	NA	NA	0.00

Cost Summary Table		
	Current	6 $\sigma$ Worst Case
Unit Cost (£ to produce)	11.74	11.74
Quality Cost per unit (£)	0.06	0.00
Quality Cost per 1,000,000 units (£)	58460.50	399.16
<b>Excess Quality Cost (£)</b>	<b>58061.34</b>	

Figure 9-40 Torque Sensor Manufacturing Quality Cost Summary

### 9.4.6 Conclusion

The analysis was performed within the DMAIC framework showing that *eCA* can be easily integrated into a standard six sigma project. Through the application of *eCA* using a physical modelling technique the expected failure rates and quality costs associated with the manufacture of the Gen. 1 torque sensor were accurately estimated.

## 10 Discussion, Conclusions and Further Work

### 10.1 Review of the Objectives

The principle objective of this work was to develop both the techniques and methodology for the assessment and estimation of the quality costs associated with the design, manufacture and test of electronic products. The estimate produced by the developed methodology was not expected to be figure accurate to the ‘pounds and pence’ level but rather a ‘ball park’ figure giving a quick indication and good feel for any potential quality issues. The main focus of the work, within this objective, was on the underserved mixed-signal electronics sector; and the drive of this focus was to produce techniques and methodologies which provide feedback directly to product designers and producers, relating design decisions regarding function, manufacture and test to any associated quality costs. Given the wide range of activities the methodology must serve, a key feature is that the methodology is consistent across all three domains both in terms of ease of application and metrics used. Further to this the developed methodology should be flexible enough to allow application as a stand-alone tool or within existing product development frameworks. The presentation of results should be such that any problems may be quickly diagnosed and, where possible, potential solutions indicated.

### 10.2 Review and Assessment of the Framework

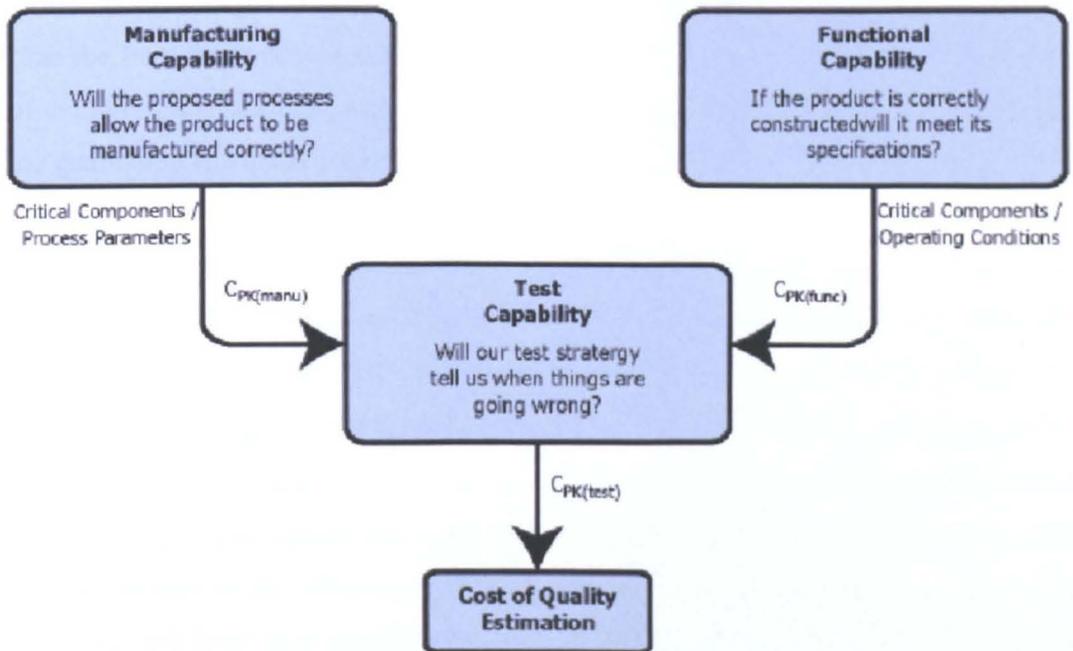


Figure 10-1 The eCA Framework

The three module framework shown in Figure 10-1 provides the structure required by the *eCA* methodology. The framework allows *eCA* to address the three key areas of an electronic product or system where quality costs may be introduced:

- Functionality
- Manufacturability
- Testability

The framework's modular format provides a consistent, flexible and simple format which allows an electronic system to be analysed in a number of different ways. Hence this ensures that emphasis of analysis may be placed upon the different aspects of quality associated with the electronic system as required. Further to this the consistency of the framework is supplied and enhanced through the use of  $C_{PK}$  and DPMO as common metrics applied to each module.

When assessing the framework against the requirements placed upon it to cover a number of domains whilst remaining consistent and flexible it is obvious that the most significant limitations of the approach lie in the assessment of test capability, which requires both the assessment of functional capability and manufacturing capability (or a prediction of the expected defect spectrum), as inputs in order to drive the assessment system.

In summary we can say that the framework is potentially very flexible, allowing independent assessment of both functional and manufacturing capability. At the same time the framework provides a completely consistent metric system prescribing the use of the interchangeable  $C_{PK}$  and DPMO metrics, which provide a simple method for both the qualitative and quantitative assessment of quality costs.

A key aspect of the *eCA* framework is its flexibility which allows it to be used in a number of different situations. The framework compares favourably with established techniques such as TQM and Six Sigma because which are commonly criticised for their prescriptive tightly structured nature [B25]. Although this tight structure does have a number of advantages, including standardisation, the *eCA* framework shares these, whilst also allowing a potentially significant level of customisation, which is unmatched by other methodologies. Further to this, the standardised systematic nature of Six Sigma and TQM will limit their applicability in knowledge-based companies (e.g. research and advanced technology organisations). These are typically characterised by unpredictable

and quickly changing requirements [B9]. Within such an environment it is difficult to apply the standard techniques which typically require a large amount of preliminary work before any analysis may begin and then only within a project structure. As a result of this they are not well suited to a quickly changing and continuously renewing process. In contrast to this the *eCA* framework requires only minimal preparatory work and although it may be applied within a project structure, such as DMAIC, it is equally suited to being used as a ‘quick to apply’, free standing and self contained analysis procedure.

### 10.3 Review of the Functional Capability Module

The functional capability analysis module employs the standard Monte Carlo statistical analysis technique for the assessment of the products performance space. Although this is potentially a computationally expensive option, compared to alternative techniques, it does provide a better coverage – cost ratio. Along side this advantage the Monte Carlo technique is both relatively simple to apply and understand as well as allowing the application of optimization techniques to increase computational speed if required by the user.

The performance analysis employed by *eCA* implements capability analysis using the  $C_{PK}$  metric supported by an automated curve fitting process and culminating in a stacked capability breakdown. This linear process shown in Figure 10-2, is both simple and fast to understand and use. The module is completed through the use of the capability breakdown to display and diagnose the ability of the system under study to conform to its specification.

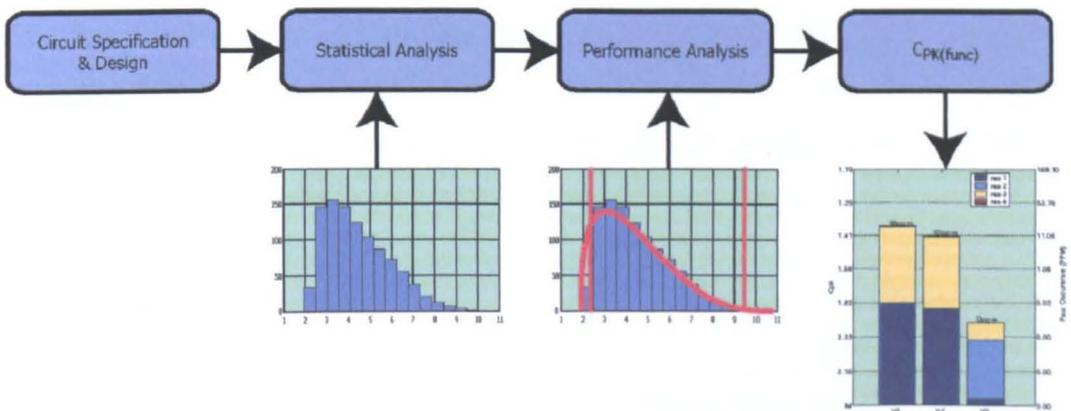


Figure 10-2 The Functional Capability Analysis Process

Compared to standard capability analysis procedures, which deal only with normal curves, the *eCA* technique, which is based on the use of a curve fitting procedure, has a

number of obvious advantages including greater ease of use. Less obviously, as the analysis is based around the actual data rather than a manipulated or transformed data set (as is common within standard techniques), any conclusions that are reached are directly applicable to the process in question rather than the 'transformed' process represented by a manipulated data set. This is particularly advantageous as it allows a quicker and simpler path to the drawing of conclusions leading to actions and improvements. One disadvantage of the application of a curve fitting procedure is that it may make it difficult to estimate the effects of a shift in the process mean, associated with design changes, without resorting to additional statistical analysis. In addition to this, the current DPMO estimation procedure supplied with the *eCA* Matlab Toolbox assumes a Normal distribution when estimating failure rates, this should be corrected in future versions of the software.

The functional analysis module satisfies the requirements for ease of use and information feedback. The main difficulty, risk and cost associated with the application of this analysis module rests with the requirement to accurately model the performance of the product. However, with increasingly powerful modelling tools and computers this is unlikely to be a problem. Furthermore, anecdotal evidence gathered from engineers who have been exposed to the tool suggests that they did not see this as a limiting factor. In fact, with the general preference of engineering organisations to reduce the risk inherent in the development of new products through the use of simulation tools, it would appear that this requirement for performance modelling should face little opposition.

The functional analysis module has proved to be extremely flexible in application, accepting data from a number of different sources. This is demonstrated by the various case studies, presented in chapter 9, which have included analysis carried out using the following commonly available analysis systems:

- SABER
- Matlab
- Simulink
- HSPICE
- PSPICE
- SPECTRE

The application of the curve fitting technique, included to allow the calculation of capability from non-normal data, has been proven to be both useful and easy to operate. Several of the case studies provided non-normal data and the technique was in fact necessary to allow quick analysis of this data. It also proved accurate when compared to more complex methods for the calculation of capability from non-normal data, such as data transforms. The capability breakdown forms the final, and perhaps most significant, stage of the functional analysis module. The breakdown has been shown to be extremely useful when assessing the performance of an electronic system. The case studies have demonstrated the power of this graphical presentation technique and the fact that it allows the controlling factors of a system to be optimized to improve performance.

The square-linear nature of the histogram is particularly useful as it allows decisions regarding different potential tolerance combinations to be made quickly from the graphical presentation without the need to consult detailed numerical data. Further to the basic capability histogram, the recasting of the data as quality cost data allows the system optimization to be targeted such that the changes producing the biggest cost savings may be introduced. This feature has proved to be particularly popular with project engineering teams who must often carefully balance project budgets to give the 'biggest bang for the buck'.

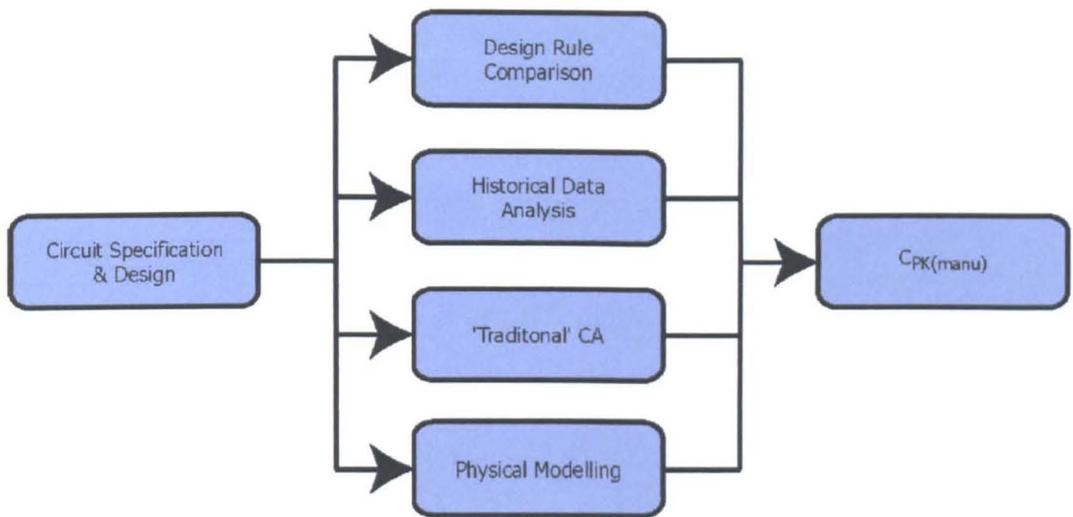
The obvious limitation of the capability breakdown technique is its assumption of linear characteristics over the intended operating range of a system. This assumption is implicit in the use of multiple linear regressions to derive the response surface associated with each of the performance metrics. Although in many cases this assumption should prove to be valid as it is often a design feature of electronic systems. However, in other cases the assumption of linearity may cause the derivation of capability breakdowns to be inaccurate; this will not affect the reliability of the calculated capability index associated with each performance metric.

To some extent the functional capability module has similar aims to established techniques such as DOE and Taguchi analysis. It does, however, present some significant advantages over these techniques, notably in respect to the simplicity of the representation of the effects of several factors upon several different measures of performance. Despite this it does lack the ability of DOE based analyses to present the

effects of multiple factor interactions. In fact, this information is embodied in the data collected and it would be possible, through the development of suitable additional analysis tools, to present this information in a clear and appropriate manner. Furthermore, unlike the standard experimental procedures employed by contemporary quality methodologies, which are on the whole based around the use of DOE style analysis and hence only analyse a system at two or three factor levels. This functional analysis module, which is based on Monte Carlo analysis, takes explicit account of the probability distributions of system factors. Finally, the *eCA* analysis could be considered to complement Taguchi by providing a 'voice of the process' to be heard along side the 'voice of the customer'. This could plausibly lead to a rationalisation of the demands Taguchi driven robust design can place on the processes associated with an electronic system.

#### **10.4 Review of the Manufacturing Capability Module**

The *eCA* manufacturing capability analysis module provides a flexible framework able to accept data from a number of sources, as demonstrated by Figure 10-3. It is potentially the simplest of the three main *eCA* modules, with the analysis of design rules and historical data providing direct access to manufacturing defect occurrence rates. The option to apply the 'traditional' form of conformability analysis in order to gain capability data is particularly suited to the analysis of any mechanical components; ranging from boxes and enclosures through to actuators in more complex electronic systems. The final route available with which to assess manufacturing capability is to apply a physical modelling technique to the product under study. This option is particularly applicable to the assessment of mechatronic components and systems. It also has the advantage that it will allow the *eCA* software tools to be applied within this analysis module in a similar way as for functional analysis. This is the case in this situation as the physical modelling is essentially the same as the simulation carried out as part of the functional analysis.



**Figure 10-3 The Manufacturing Capability Analysis Process**

The number of assessment routes open to an engineer applying this module may at first appear complex. However, the complexity of modern products and production systems demand this variety. The choice of options creates a flexible module capable of assessing the production routes of most products with relative simplicity. Historical data will provide perhaps the best indication of manufacturing capability, although, as mentioned previously, it will also carry the burden of requiring data validation. This should not prove too great an obstacle, especially within a company with an active quality policy. Of course, such historical data will not necessarily be available when new processes or component packages are introduced and so some analysis using, for example, physical modelling, may be required. The ability of the module to use physical modelling as a means to assess capability with the assistance of the *eCA* software, is a particularly strong aspect of this module. Engineers following this route will have access to the benefits of the software including the capability breakdown, which should allow relatively simple diagnosis of any potential or current quality issues.

The manufacturing capability module has been successfully applied to several case studies as described in chapter 9, and was particularly successful when applied to the torque sensor. In the case of the torque sensor analysis *eCA* was employed to provide feedback to the design team regarding which aspects of the manufacturing process and manufacturing defect compensation algorithms should be improved to provide the most efficient use of time and money. The module was applied iteratively to the product using a simulation based around a Matlab geometric model and ECU algorithm implementation.

### 10.5 Review of the Test Capability Module

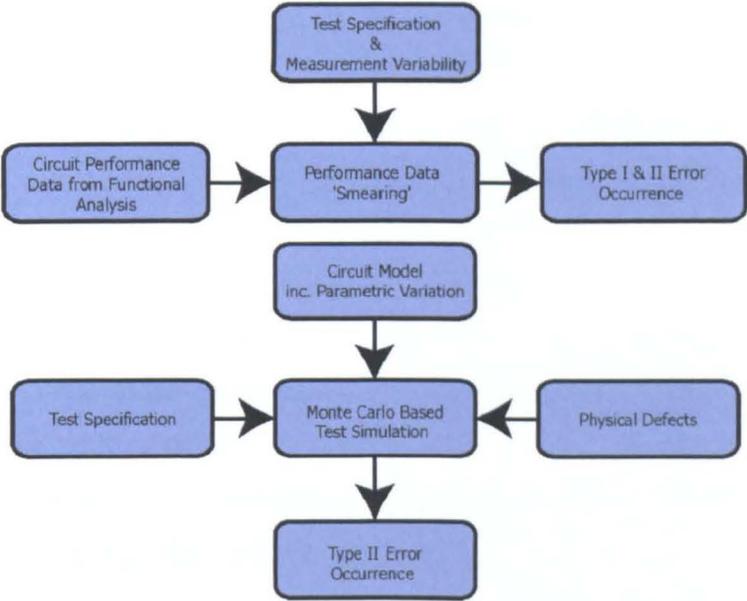
The test capability analysis module is both the most complex and least flexible module of the eCA process. The requirement of the module to diagnose both forms of potential test error (Figure 10-4) leads to a three stage process as shown in Figure 10-5. The first stage of the test analysis process is to determine the test performance space when exposed to a circuit containing no ‘hard’ defects. This may be achieved in two different ways:

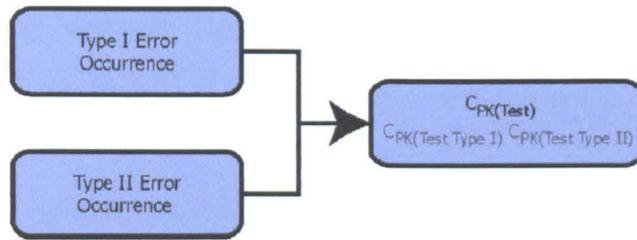
- An analysis (post processing) of the functional analysis data
- A new simulation using the functional analysis model

The route followed will depend upon the exact nature of the functional analysis carried out. If the system stimulus used in the functional analysis was comparable to that to be used in the test analysis and if suitable performance data was stored it is likely that post processing of the functional analysis data will be sufficient. However should this not be the case a new performance space simulation will be required modelling the desired test process.

	Pass	Fail
Defect Free Circuit	OK	Type I
Defective Circuit	Type II	OK

Figure 10-4 Test Error Classification





**Figure 10-5 Overview of the Test Capability Analysis Module, Showing the Three Main Steps to Calculating Test Capability**

The second stage of the test analysis process is more complex, requiring that the user either manually implements fault simulation or uses an automated fault simulation package such as ANTICS [B75;B76]. Such packages are capable of injecting defects into a circuit using a library of defect models. Each defective circuit model should then be simulated using a Monte Carlo type approach. As this procedure may lead to a large number of pointless simulations, for example when a circuit is clearly non-functional due to the induced defect, it is suggested that a small sample screening run is carried out prior to a larger sample run when defect diagnosis is less clear cut. Once both analysis stages are complete the module combines the results from both stages to determine the expected number of DPMO for the testing procedure. This figure may then be converted into an equivalent representative  $C_{PK}$  value as desired.

Implementing the test analysis procedure is a complex process that requires care at each stage and has a number of potential problems. The most obvious and serious of these is the requirement for either laborious work to develop models of defective circuits or specialist fault simulation software. Secondly the procedure may incur a large computational cost when a circuit or system, and hence its associated defect spectrum, is large. The *eCA* test analysis takes a relatively simplistic view of the various defects a circuit may experience with the initial analysis making the assumption that defects are mutually exclusive. This is a potentially questionable assumption given that, due to poor process control, many defects occur in clusters. However, as the aim of the process is to produce a ‘ball park’ estimate of quality costs it is an adequate representation particularly given that it is relatively unlikely that a circuit or system containing multiple defects would produce a test error.

Overall, despite the relative complexity of the module, when compared to the other *eCA* modules the test capability assessment module is both effective and reasonably simple to apply given the difficulty of the assessment task. Although the presentation of results

is not graphical, as with the functional and manufacturing capability assessment modules the results are presented clearly in a format which is suited to the task of test error diagnosis.

### 10.6 Review of the Conformability Matrix

The conformance matrix provides engineers with a means to assess both the quality costs due to failures in any of the assessed aspects of a design and the total expected quality cost for the design, providing a simple means of collecting and summarising the data generated during the analysis. The matrix may be split into three distinct sections each of which is completed using the data generated by one of the eCA analysis modules. The first section, completed once the functional analysis has been carried out, gives an indication of the performance of the circuit or system if manufactured as defined by its technical documentation with no unexpected or unintended parametric variation. The second segment of the matrix contains the information generated during the manufacturing section of the analysis and the final section contains the information generated by the test analysis stage.

Performance Metric	Defect	Conformance Area															
		Functional				Manufacture				Test (Type I)				Test (Type II)			
		Cpk	DPMO	Impact	Cost (%)	Cpk	DPMO	Impact	Cost (%)	Cpk	PPM	Impact	Cost (%)	Cpk	PPM	Impact	Cost (%)
Metric 1	NA																
Metric 2	NA																
Metric 3	NA																
Metric 4	NA																
Metric 1	Defect a																
Metric 2	Defect a																
Metric 3	Defect a																
Metric 4	Defect a																
Metric 1	Defect b																
Metric 2	Defect b																
Metric 3	Defect b																
Metric 4	Defect b																
Metric 1	Defect x																
Metric 2	Defect x																
Metric 3	Defect x																
Metric 4	Defect x																

Figure 10-6 The Main Body of the Matrix

The information is then summarised in the three summary tables shown below.

Summary Table by Single Area					
	Conformance Area				
	Functional	Manufacturing	Test (Type I)	Test (Type II)	Test (ALL)
Total DPMO / PPM					
Representative Capability					
Total Associated Cost (%)					

Cumulative Summary Table						
	Conformance Area					Worst Case
	Functional	Manufacturing	Test (Type I)	Test (Type II)	Test (ALL)	
Total DPMO / PPM						
Representative Capability						
Total Associated Cost (%)						

Cost Summary Table	
	Current
Unit Cost (£ to produce)	
Quality Cost per unit (£)	
Quality Cost per 1,000,000 units (£)	
Excess Quality Cost (£)	

Figure 10-7 The Matrix Summary Tables

These both summarise the data generated by the analysis and provide a comparison with a system which performs to Six Sigma quality levels.

The matrix has proven to be a satisfactory method for the display and analysis of the data generated by the *eCA* tool as demonstrated in chapter 8. The main part of the matrix can, at first, seem overwhelming but this is counteracted by the use of the smaller summary tables which clearly present the generated data distilled down to a few figures which are able to penetrate to the heart of most problems. The use of Impact (severity) figures to allow cost of quality estimates to be made is an exceptionally powerful aspect of the conformance matrix for several reasons, but most importantly because it allows design changes and improvements to be prioritised on a cost-benefit basis.

### **10.7 Review of the Cost Model**

Although appearing basic, the cost model employed by the *eCA* methodology derived from that used in the mechanical form of conformability analysis, is powerful and able to provide a good estimate of the quality costs likely to be incurred by a defective design or process. Despite the fact that the predicted costs will not be accurate to the 'Pounds-Pence' level they do meet the aims of the research as they provide a good indication of the quality costs associated with a system. Unlike other cost models, such as the quadratic quality loss function proposed by Taguchi, the *eCA* cost model is aimed at the producer of a system and not at a customer. Therefore it may be argued that in the same way as the Taguchi model is the 'voice of the customer' the *eCA* model is the 'voice of the process'.

Further to this the *eCA* model may also be used in reverse to determine the appropriate level of system capability for a particular CTQ function. By considering the cost map given in chapter 4 we can see that given a CTQ function which has a particular Impact (severity) level associated with it we must attain a particular process capability in order to obtain an acceptable level of associated quality cost.

### **10.8 Review of the Methodology Validation**

The *eCA* methodology has been validated through practical application to a series of industrially provided case studies and is now in use within an industrial engineering environment. Each case study analysis was carried out by the author in a parallel with a

second analysis carried out by the case study provider using conventional analysis tools. After each case study feedback was provided regarding the usefulness of the *eCA* analysis and a comparison was made to the data gained using the conventional analysis procedure. To date the majority of the methodology validation work has concentrated on the functional and manufacturing capability modules, with only one case study examining the effectiveness of the methodology in estimating the quality costs associated with test process failure.

The case studies have shown that the *eCA* methodology is able to provide useful and accurate information regarding the likely quality costs associated with the non-conformance of an electronic system to its specification. Further validation should take the form of large projects exercising the full range of the *eCA* tool set on a single system or system component.

### **10.9 Summary of Potential Areas of Application**

In common with CA, the flexibility of *eCA* means that the technique may be applied for a number of different purposes including the following:

- *eCA* may be applied to a system as part of a capability study in order to determine the level of capability associated with the system as a whole or one of the components of the system.
- *eCA* may be applied to estimate the quality costs associated with a system, to determine the level of acceptability or for comparative purposes.
- *eCA* may be used to help specify the acceptable nominal values and tolerance ranges of system components
- The methodology may be used to optimize a test process.

### **10.10 Industrial Application**

As with the standard form of CA *eCA* has been adopted by TRW Automotive. The methodology is being introduced to the company through the Six Sigma training courses and as a service offered by TRW Conekt. The technique has been applied to a number of different products and has played a major role in the development of the next generation optical torque sensor. The tool is currently used by a small group of engineers, in conjunction with the author. To achieve wider application of the *eCA* methodology a set of comprehensive training materials must be created and the analysis software must be developed to a commercial standard.

## **10.11 Conclusions**

This thesis has presented the development of a new methodology and a set of supporting tools for the assessment of the potential quality costs associated with electronic systems known as Electronic Conformability Analysis. The methodology was developed and tested by application to a number of industrially provided case studies some of which have been presented here. The methodology is flexible and is suitable for application within an industrial environment to systems which range in complexity from basic analogue and mixed signal circuits to complex microprocessor based systems. Furthermore the methodology is not dependant upon any single performance analysis technique and it is also independent of the level of abstraction at which the analysis is performed. This flexibility allows the technique to be applied iteratively through out the system design process completing more detailed analyses as a design progresses. Further to meeting the stated aims the developed tools and techniques also provide the indirect benefits including improved 'design quality', reduced numbers of design iterations, increased manufacturability and more efficient engineering processes.

The tools presented with the methodology provide a clear and concise means of displaying the results of the assessment exercise. They supply the designer with an intuitive guide to the areas in which a system must be improved to reduce quality costs, as well as providing a guide to which improvements will result in the greatest cost benefits.

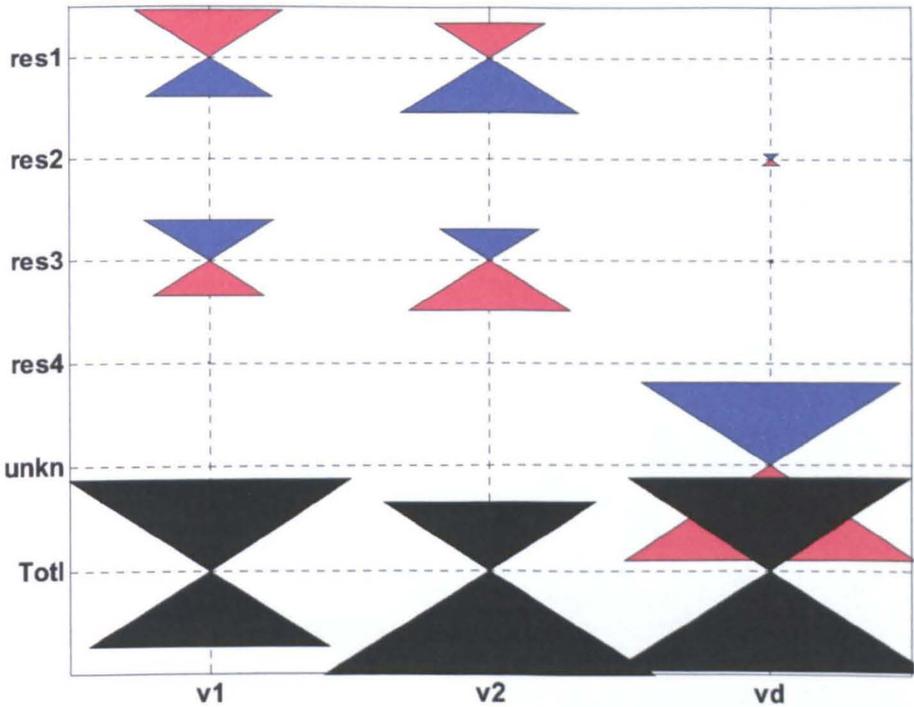
The *eCA* methodology may be applied in the form of a 'stand alone' analysis where it is able to quickly produce an estimate of both the capability of a system and the associated quality costs. Additionally, *eCA* may be applied in support of other methodologies for example it may form part of the analysis phase of a Six Sigma style project, or be used to identify those system parameters which should be subjected to a detailed DOE analysis.

The developed methodology has been evaluated on a range of commercial products and has been found to give accurate predictions of both the occurrence of defects and the associated quality costs. It has been shown to give a good guide to the key system parameters which must be controlled or modified in order to improve the level of quality associated with a system. This practical application of the methodology in an industrial setting has produced a number of benefits for the companies involved which

have resulted in improvements in the capabilities of the systems analysed and a reduction in the associated failure costs.

### 10.12 Further Work

There are a number of areas of the *eCA* methodology and tool set which require further work. Significant improvements would be made to the toolset should it be expanded to provide analysis options detailing the effects of multiple factor interactions. Efforts should also be made to allow the analysis to take into account non-linear relationships. Additionally, greater use could also be made of the existing information provided by the current linear analysis, for example additional graphical representations such as that shown in Figure 10-8 could be developed. This illustration shows how the gradient of the response surface could be used to indicate how the nominal value of a system component could be modified to improve functional capability. In the illustration the black 'bows' are proportional in size to  $C_{PK}$  whilst the smaller coloured bows are proportional in size to the contribution made by a particular component to the corresponding function. If the red half of the bow is largest it indicates that to improve the capability of a particular function the nominal value of the component should be reduced and vice versa for the blue half.



### **Figure 10-8 Modified Capability Breakdown**

Initially the main thrust of any additional work carried out on the *eCA* methodology must be an improvement of the integration of the three modules forming the *eCA* framework. This may be most effectively achieved through the provision of more comprehensive software tools. Such tools would be required to provide greater flexibility of analysis than the current Matlab Toolbox and they should automate the generation of analysis programs and interface with commercial simulation and modelling tools. An improved software suite should also include automatic report generation and on-line help. In addition to facilitating further adoption of the methodology through improvements in the *eCA* software tools, a wider adoption of the methodology would be achieved through the development of suitable training materials for use in an industrial environment.

## 11 Publications

*A Conformability Analysis Based Test Strategy*

I.M.Bell, J.M.Gilbert, D.R.Johnson

IEEE International Mixed Signal Test Workshop 2001

*Design, Manufacture and Test – Quality Cost Estimation*

J.M.Gilbert, D.R.Johnson, I.M.Bell

IEEE 3<sup>rd</sup> International Symposium on Quality Electronic Design, San Jose, USA, 2002

*Design Quality Estimation for Electronic Circuits*

J.M.Gilbert, I.M.Bell, D.R.Johnson

Engineering Design Conference, London, UK, 2002

*Conformability Analysis Based Test Quality Cost Estimation*

I.M.Bell, J.M.Gilbert, D.R.Johnson

IEEE International Mixed Signal Test Workshop 2002

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## 13 Appendix A: Matlab Toolbox

### 13.1 Introduction

The purpose of the Matlab Toolbox is to simplify the application of the eCA methodology to a product. The toolbox contains a number of functions written to simplify the tasks and calculations carried out as part of the analysis procedure along with a GUI based implementation of a software demonstrator to provide an integrated route through the analysis procedure.

### 13.2 Function Descriptions

The following sections give a brief description of the purpose of each of the functions included in the eCA toolbox.

### 13.3 Curve Fitting

Name	Purpose
<code>basic_term</code>	Calculates the coefficients used to describe the shape of the performance data, these are the foundation of the curve fitting procedure. It also calculates $k$ the Pearson coefficient which is used to determine which curve type will best fit the data.
<code>typeone_variab</code>	Calculates the specific variables used by the Type I Pearson curve, along with the range of the data.
<code>typeone_eval</code>	Evaluates the Type I Pearson curve over the specified data range for the predetermine curve coefficients, the function outputs a PDF for the curve over the specified range.
<code>typefour_variab</code>	Calculates the specific variables used by the Type IV Pearson curve, along with the range of the data.
<code>typefour_eval</code>	Evaluates the Type IV Pearson curve over the specified data range for the predetermine curve coefficients, the function outputs a PDF for the curve over the specified range.
<code>typesix_variab</code>	Calculates the specific variables used by the Type VI Pearson curve, along with the range of the data.
<code>typesix_eval</code>	Evaluates the Type VI Pearson curve over the specified data range for the predetermine curve coefficients, the function outputs a PDF for the curve over the specified range.

ks_test	Carrys out a Kolmogorov – Smirnov test, checking the fit of a curve to a discrete data set
occurance	Calculates the rate of defect occurrence for a non-normal distribution

### 13.4 Capability and Defect Occurrence Calculation

Name	Purpose
nonnorm_capable	Calculates an equivalent $C_{PK}$ for a non-normal distribution, using points on the distribution which equate to the same probability found at $\pm 3\sigma$ .
occur	Given a $C_{PK}$ value this function calculates the probability of a process producing a defect.
occurence	Given a $C_{PK}$ value this function calculates the rate of occurrence of defects that may be expected.
capability	Given a defect occurrence rate (ppm) this function calculates the equivalent $C_{PK}$ value.
test_error	Given a set of performance and test limits along with expected levels of noise for each measurement this function estimates the occurrence of Type I and II test errors.

### 13.5 GUI Based Functions

Name	Purpose
ca_assess	Starts up the GUI based <i>eCA</i> software and configures all of the variables required.
splash	Displays a ‘Splash’ screen for the software
cctcpkgui	This is an interactive dataset loading and variable selection window.
cctcpkswitch	‘Switch Yard’ function for the <i>eCA</i> toolbox this function is used to determine what should happen when an action is requested from a GUI
fault_param_choice	Allows the user to select a subset of the performance measures and parameters for the conformability analysis
cctcpk	Function to manage the actual conformability analysis process, from the confirmation of specification limits

	through to the plotting of capability breakdowns.
histgui	GUI to display a histogram of the performance data together with the performance specification limits. The function will only allow the analysis to proceed if suitable specification limits are set.
getspeclims	GUI to manage the editing of performance specification limits, the function will only allow the analysis to proceed once suitable specification limits are set.
curvefitaba	Function to manage the curve fitting process, from the selection of the appropriate curve type to the application of appropriate scaling factors to prevent unexpected outcomes.
curvedisp	GUI to display the data with both a normal and non-normal fitted distribution to allow the user to chose the appropriate distribution to use for the calculation of capability.
incapplota2	Function to generate and plot the capability histogram.

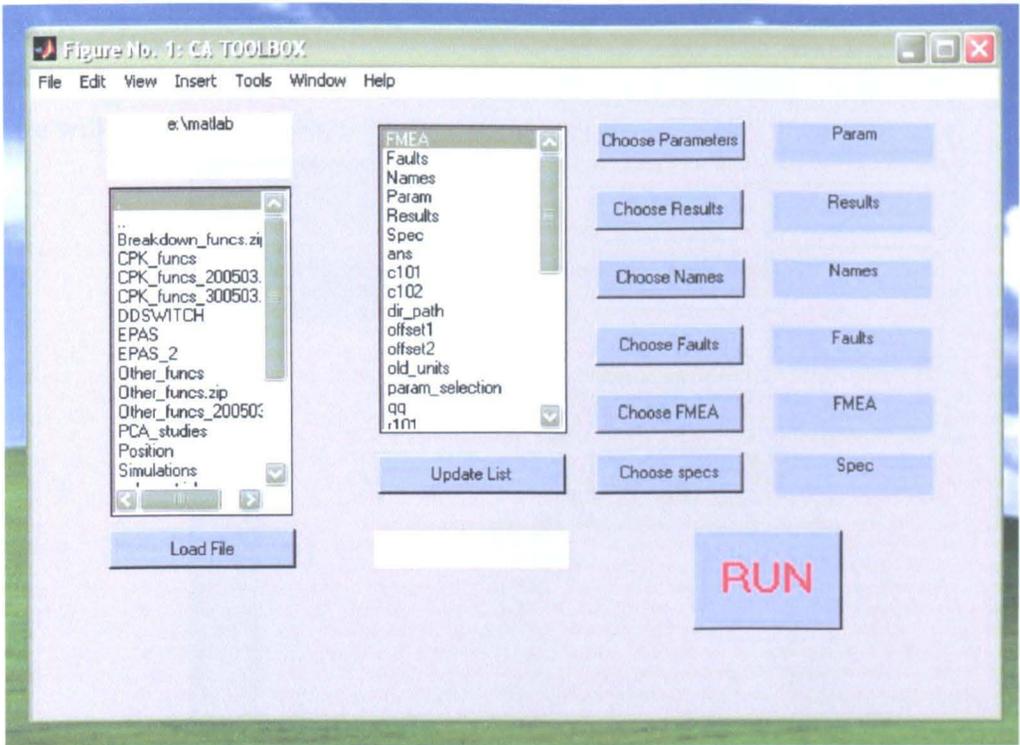
### 13.6 A Quick User Guide to the eCA Toolbox

This section gives a quick introduction into the use of the eCA toolbox functions, before any analysis can begin the data described in Figure 13-1 must be available in the main Matlab workspace or in a saved data file.

Variable Name	Description
Param	An $n \times m$ array containing the values of each of the parameters used during the performance analysis experiment, where $n$ is the number of samples and $m$ the number of parameters.
Results	An $n \times p$ array containing the values of each performance measure for each sample, where $p$ is the number of performance measures.
Names	An $m \times s$ vector of strings each of which is the name of one parameter where $s$ is the size of each string
Faults	An $p \times t$ vector of strings where each string is the name of one of the performance measures and $t$ is the length of each string
Spec	A $p \times 2$ array containing the upper and lower specification limits for each performance measure.
FMEA	A $p \times 1$ array containing the failure Impact (Severity) for each performance measure.

Figure 13-1 Basic Data Requirements

The analysis procedure is started by typing `ca_assess` at the command prompt followed by pressing the continue button on the splash screen. The interactive parameter loading dialogue will now appear (Figure 13-2), you may now either browse to and load the Matlab data file containing the variables specified above using the listbox on the left hand side of the window and then continue by pressing RUN. Or alternatively if they are already available in the workspace the analysis is continued by pressing RUN. If the variable names used differ from the default values specified above the appropriate variables may be selected using the listbox on the right hand side of the window in combination with the appropriate selection buttons.



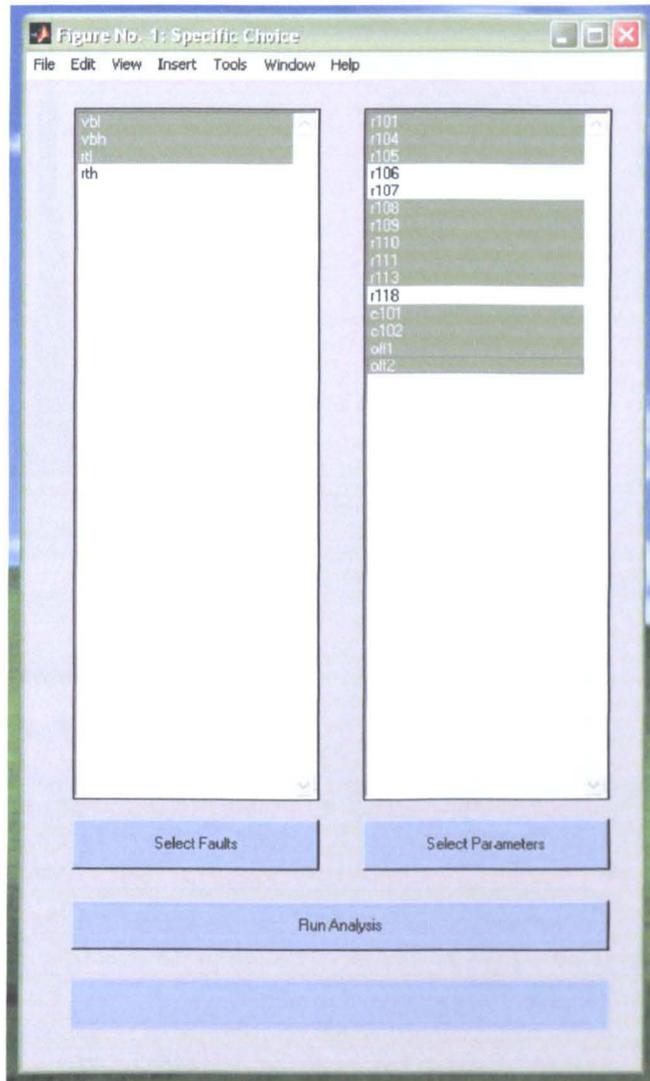
**Figure 13-2 Interactive Variable Loading and Selection Dialogue Box**

Once the Run button has been pressed the analysis will continue to the Performance area and analysis parameter subset choice dialogue box as shown in Figure 13-3. To use the dialogue box make the appropriate selections using the normal Ctrl, Shift windows selection procedure and then press the Select Faults, Select Parameters and Run Analysis buttons to continue.

Once the Run Analysis button has been pressed the Histogram editing window will open, this window shows the first performance histogram together with the appropriate specification limits. The histogram can be redrawn with a different number of bins (the default is 50) by entering the appropriate number in the box at the lower left corner of the window and pressing the Redraw button. If the specification limits as they stand are acceptable press the Accept Spec Limits button, alternately to change the specification limits press the Alter Spec Limits button. Pressing the Alter Spec Limits button will start up the Specification Limit editing dialogue, this allows new lower and upper limits to be chosen and then checks them to ensure they are valid. Once satisfactory limits are set press the Enter Spec Limits button to continue.

Upon continuing two windows will open, the main window illustrated in Figure 13-6 shows two data models the upper model is a person curve fitted to the performance data whilst the lower model is a normal curve fitted to the same performance data. The window has two buttons which are used to select the appropriate model, model choice is

aided by the quartile-quartile plot displayed with the appropriate KS statistic in the second window, Figure 13-7. The Specification limit confirmation and data model choice will be repeated as required for each selected performance measure.



**Figure 13-3 Performance Specification and Parameter Subset Choice Dialogue Window**

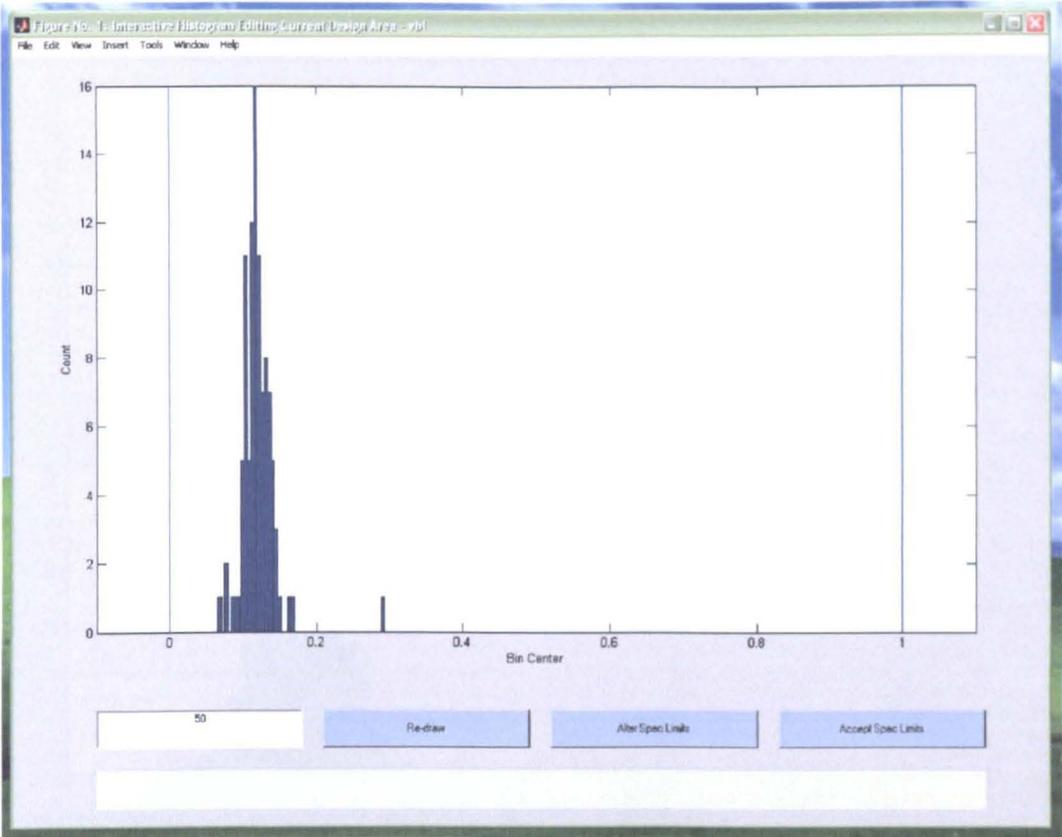


Figure 13-4 The Performance Distribution and Specification Limit Viewing Window

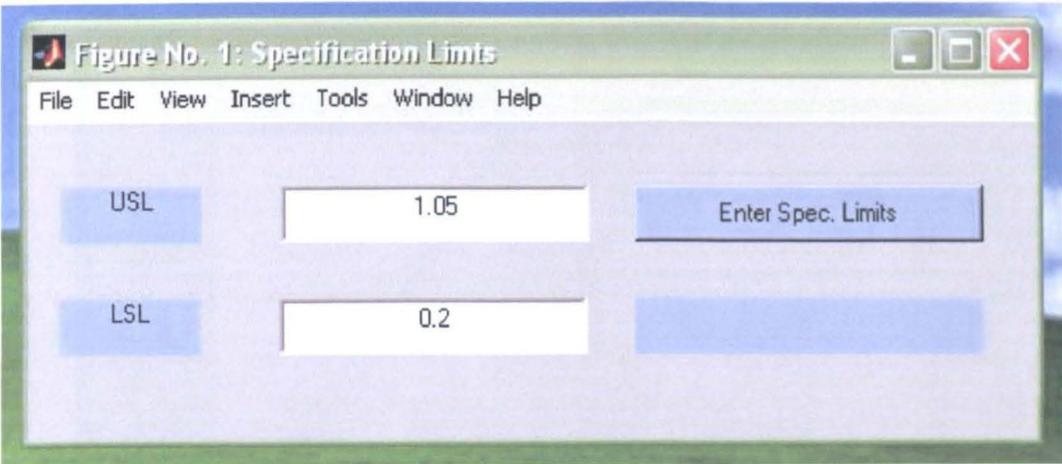


Figure 13-5 The Specification Limit Editing Dialogue

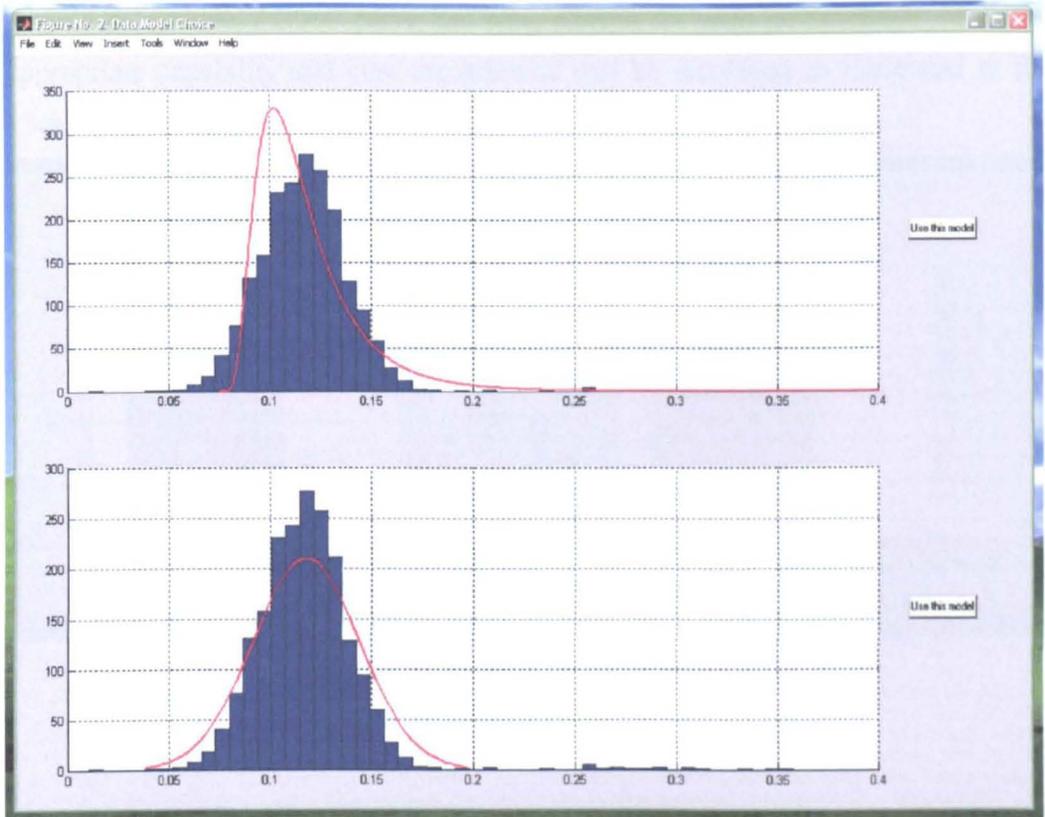


Figure 13-6 Curve / Data Model Choice Dialogue

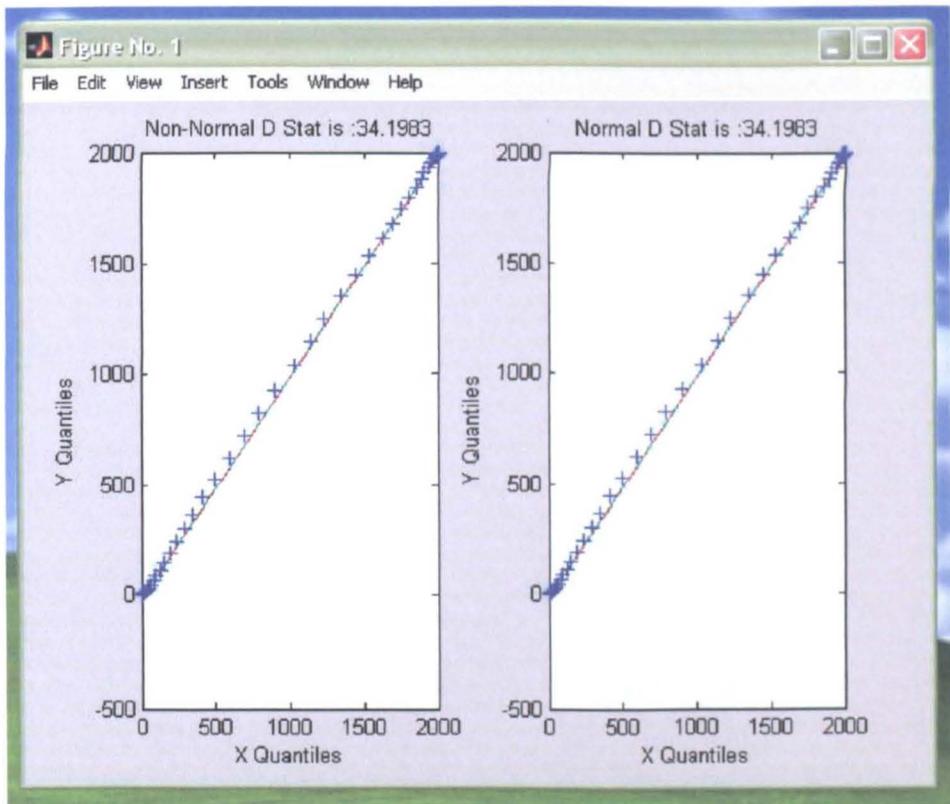


Figure 13-7 Quartile-Quartile Plot Window with Associated KS Test Statistic

Once a data model / fitted curve has been chosen for each performance measures the appropriate capability and cost breakdowns will be displayed as illustrated in Figure 13-8.

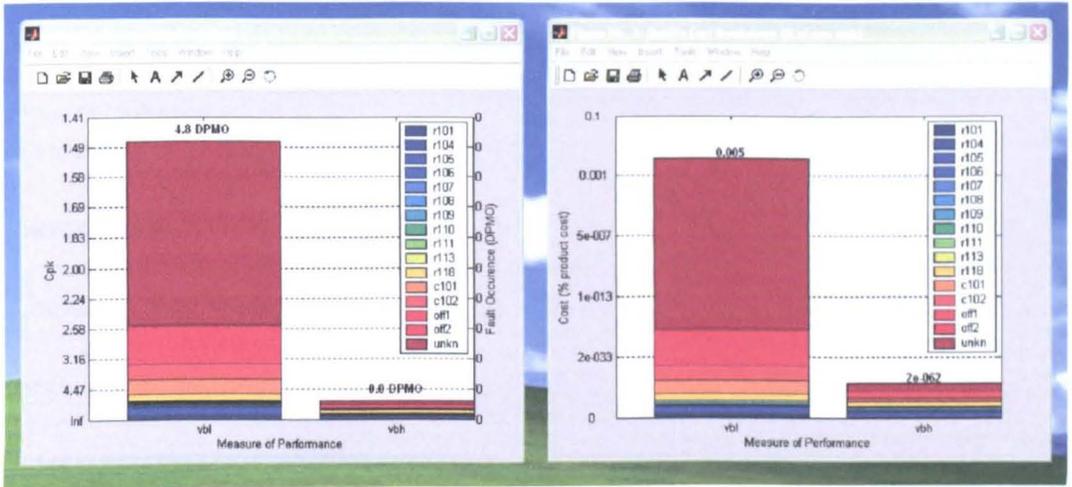


Figure 13-8 Capability and Cost Breakdowns

# 14 Appendix B : Signal Processor HSPICE Models

## 14.1.1 HSPICE Model

```
Windstar Wheel Speed decoder TRW Case Study
*David johnson
*17/10/01

.WIDTH OUT=132

.OPTIONS POST CSHUNT=1f

*taken out fast

*****
*CHOOSE DATA DRIVEN ANALYSIS*
*****
.TRAN DATA=noise UIC

*****
*THE MEASUREMENTS TO BE TAKEN*
*****

.MEASURE TRAN speed PARAM='mph'
.MEASURE TRAN sp_frq PARAM='frq'
.MEASURE TRAN amplitude PARAM='ampli'

.MEASURE TRAN cross_time WHEN V(RRSPEED)=0.5 TD=20m FALL='(frq*(1.1-20m))'
.MEASURE TRAN frequency PARAM='(frq*(1.1-20m))/(cross_time-20m)'
.MEASURE TRAN ct_in WHEN V(speed_in)=0.1 TD=20m FALL='(frq*(1.1-20m))'
.MEASURE TRAN f_in PARAM='(frq*(1.1-20m))/(ct_in-20m)'

.MEASURE TRAN res858 PARAM='R_858'
.MEASURE TRAN res859 PARAM='R_859'
.MEASURE TRAN res860 PARAM='R_860'
.MEASURE TRAN res861 PARAM='R_861'
.MEASURE TRAN res862 PARAM='R_862'
.MEASURE TRAN res863 PARAM='R_863'

.MEASURE TRAN cap807 PARAM='C_807'
.MEASURE TRAN cap808 PARAM='C_808'
.MEASURE TRAN cap809 PARAM='C_809'

*****
*READ IN THE NOISE AND COMPONENTS*
```

```

*****
*SET THE PARMETERS*
*****

.IC V(TP270)=2.9
.param sens_res=25.670K sens_ind=3.525
.param const=0.833 mph=50
.param frq='(mph/60*777)*const' ampli=3.286
.param noise_amp=1

*****
*CIRCUIT INPUTS AND SENSOR VARIABLES*
*****

*VIN speed_in 0 PULSE(5 0 0.005 1N 1N 0.005 0.01)
VIN speed_in 0 SIN(0 ampli frq 0 0 0)

r1 speed_in 0 1

VNOISE noise_in 0 PWL(TIME, pv)

r2 noise_in 0 1

EX mixed_out 0 POLY(2) speed_in 0 noise_in 0 0 1 noise_amp

RSENSOR mixed_out sensor_out sens_res
*LSENSOR S1 sensor_out sens_ind

*****
*CIRCUIT NETLIST*
*****

VCC VCC! 0 DC=5V

RIN sensor_out RR_HI 2K

R861 RR_HI VCC! R_861
C809 RR_HI GND C_809

C807 TP270 GND C_807

```

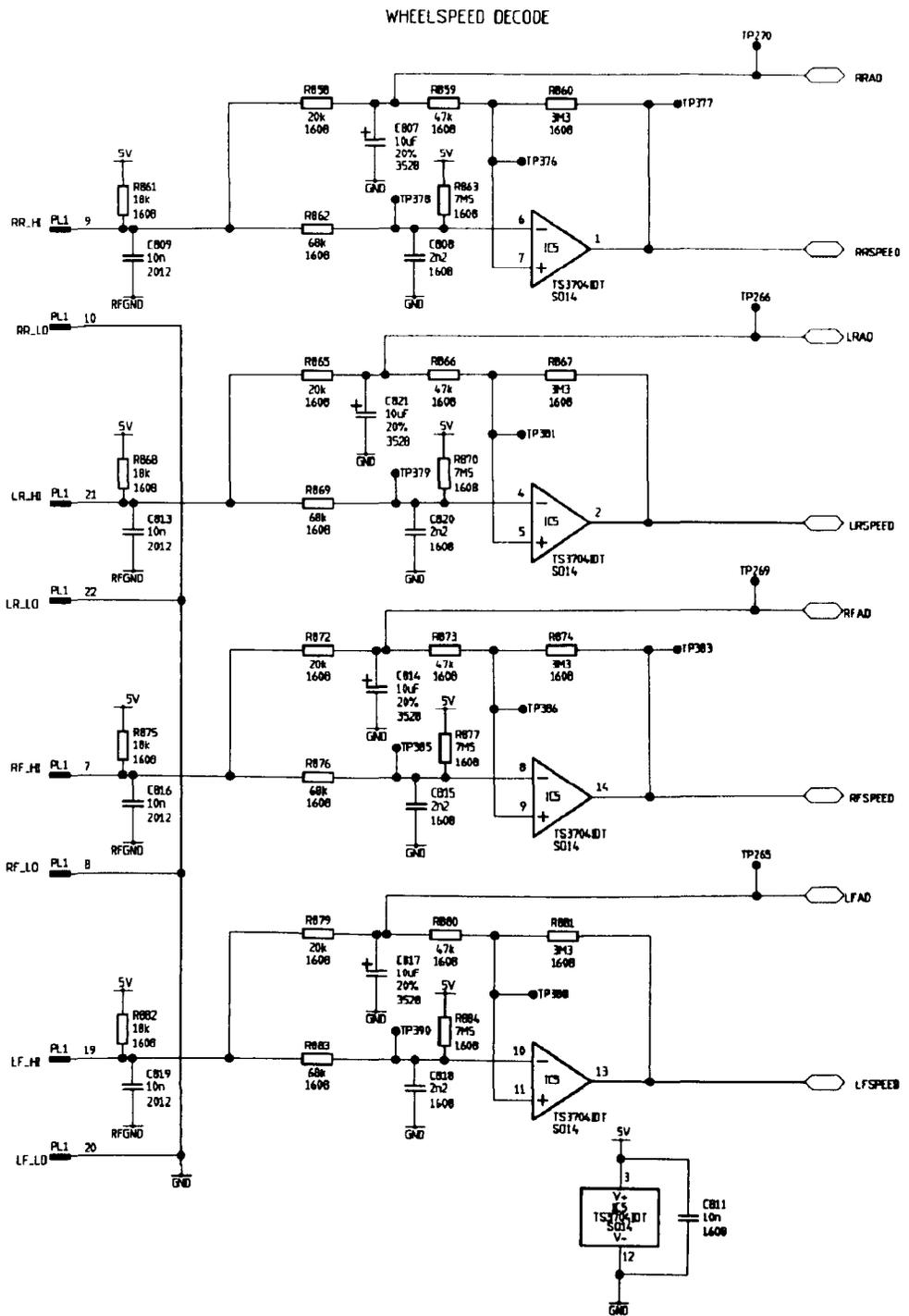
**Figure 14-1 HSPICE Netlist for the Circuit Shown in Figure 9-30 Including Sources as Used in the Functional Analysis**

```

** Macanal, Analog macromodels generator, v.1.0
** J. REMY, SGS THOMSON, ANACA Grenoble, Aug. 1992.
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
.SUBCKT TS3704 1 3 2 4 5 (analog)
*****
.MODEL MDTH D IS=1E-11 KF=1.050321E-32 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 0 2 0 1
EIN 16 0 1 0 1
RIP 10 11 6.500000E+01
RIN 15 16 6.500000E+01
RIS 11 15 1.939046E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 13 14 DC 0
IPOL 13 0 100E-06
CPS 11 15 8.16E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 1.200000E+00
FCP 4 5 VOFP 0.00
FCN 5 4 VOFN 0.00
FIBP 2 0 VOFN 2.000000E-08
FIBN 0 1 VOFP 2.000000E-08
* AMPLIFYING STAGE
RG1 5 19 2.8E+05

```

**Figure 14-2 TS3704 Macromodel**



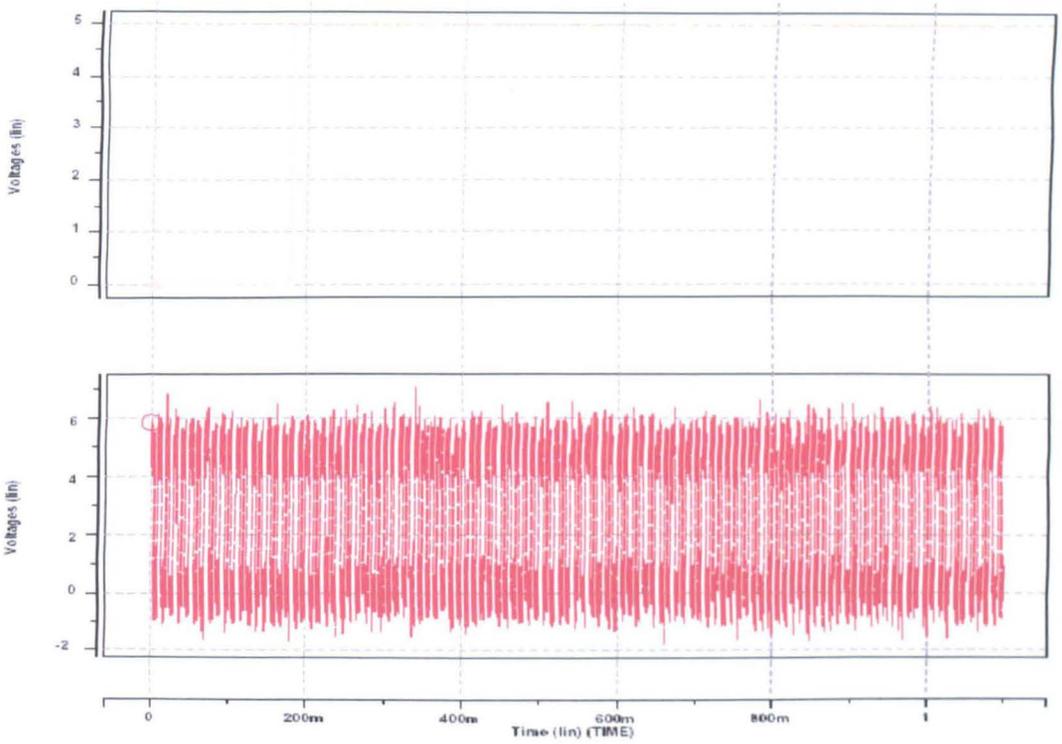
**Figure 14-3 Circuit Diagram Provided by TRW Showing the Component Numbering System Used in the Signal Conditioning Circuit Analysis**

## 14.1.2

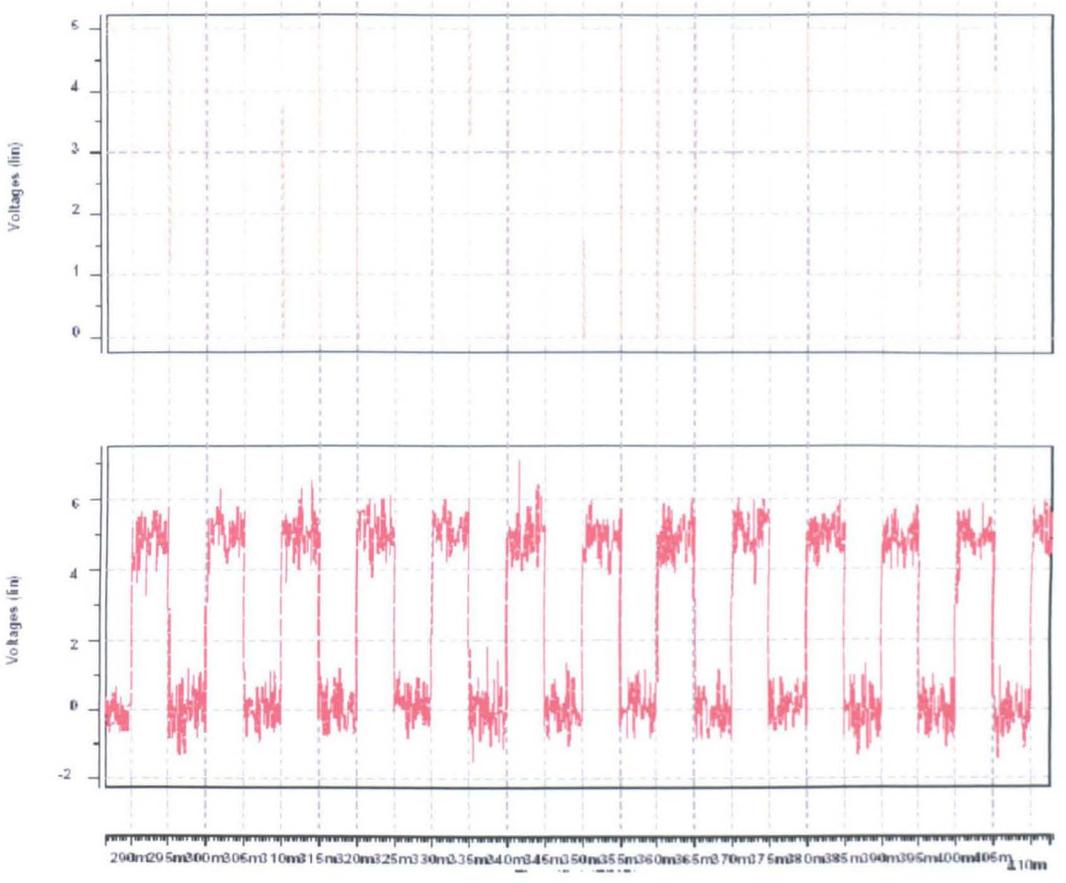
## Example Testability Analysis Results

Component: R859

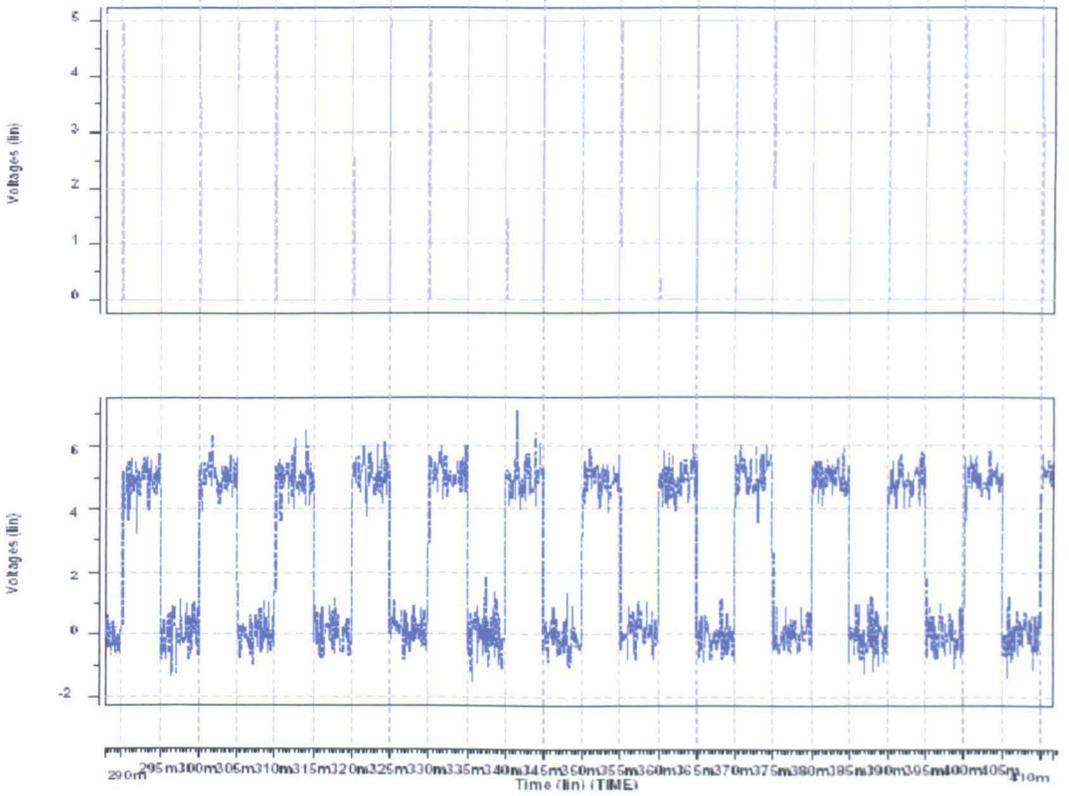
Open (Orange: RRSPEED)



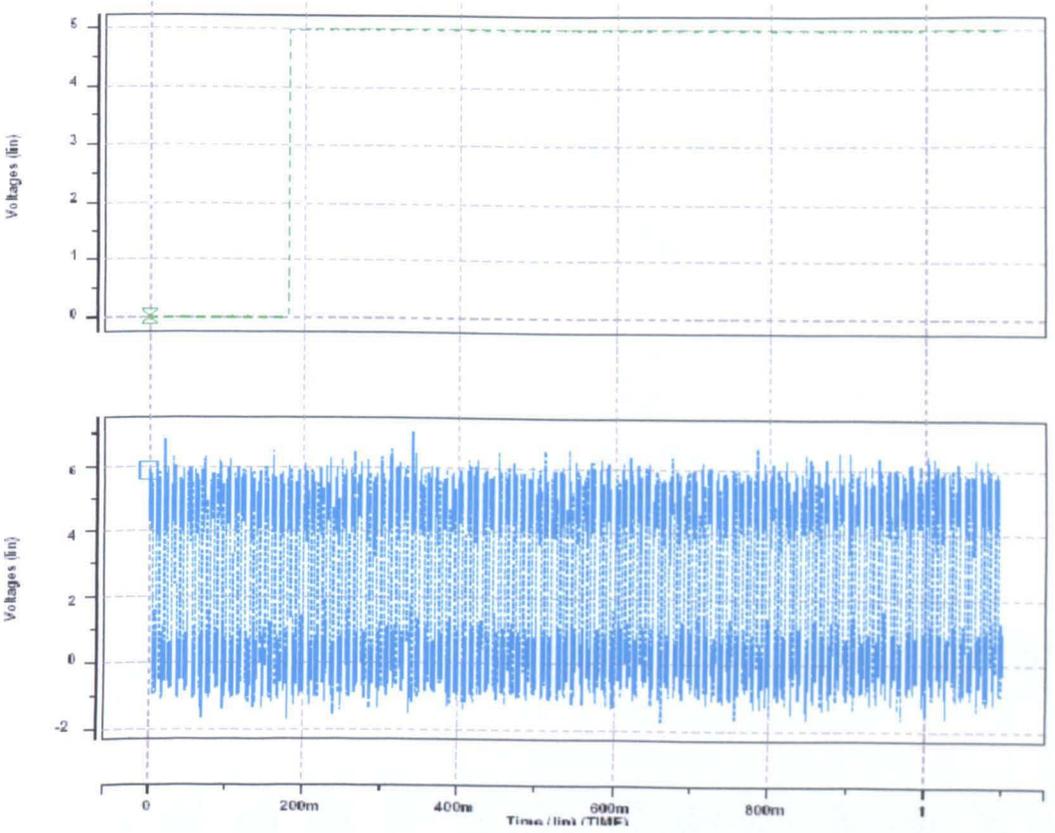
Short (Orange: RRSPEED)



Component: R860  
 Open (Purple: RRSPEED)

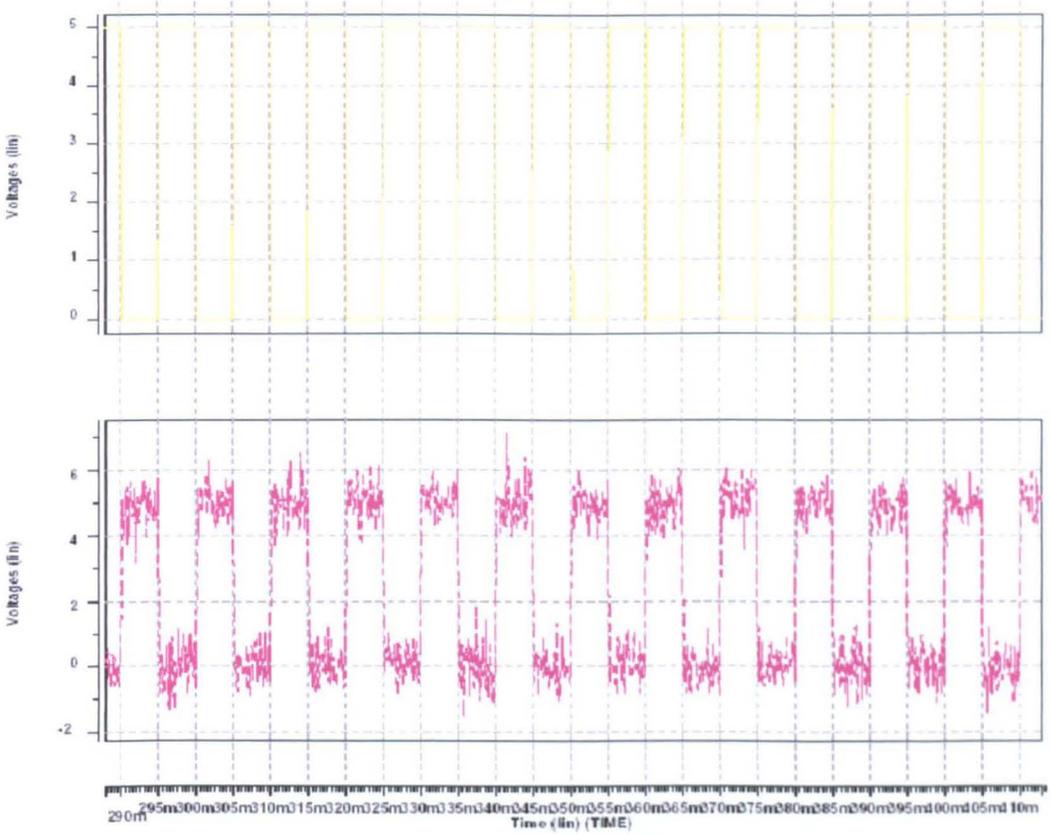


Short (Green: RRSPEED)

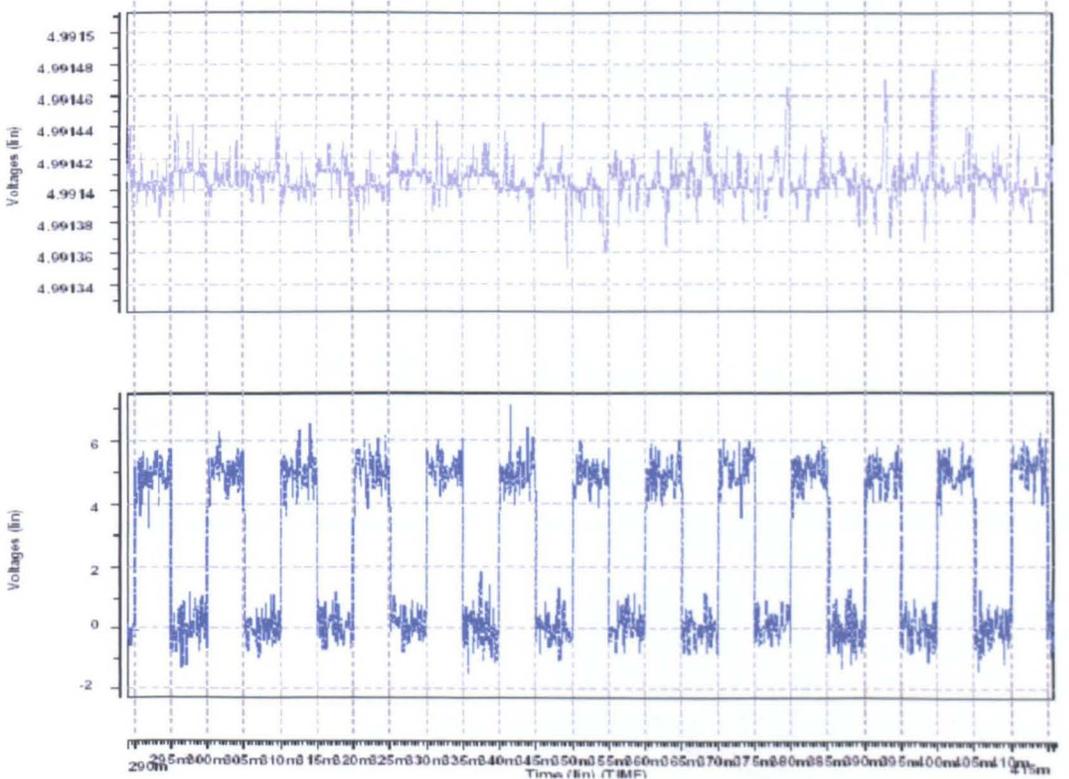


Component: R861

Open (Yellow: RRSPEED)



Short (Purple: RRSPEED)



# 15 Appendix C: Torque Sensor DMAIC Material

## 15.1 Project Charter

Save v.3)	<b>Project Charter</b>				
	<b>Torque Sensor Conformability Analysis.</b>				
Updated by: John Priddy	Issue: 05	Last saved: 31-Jul-03			

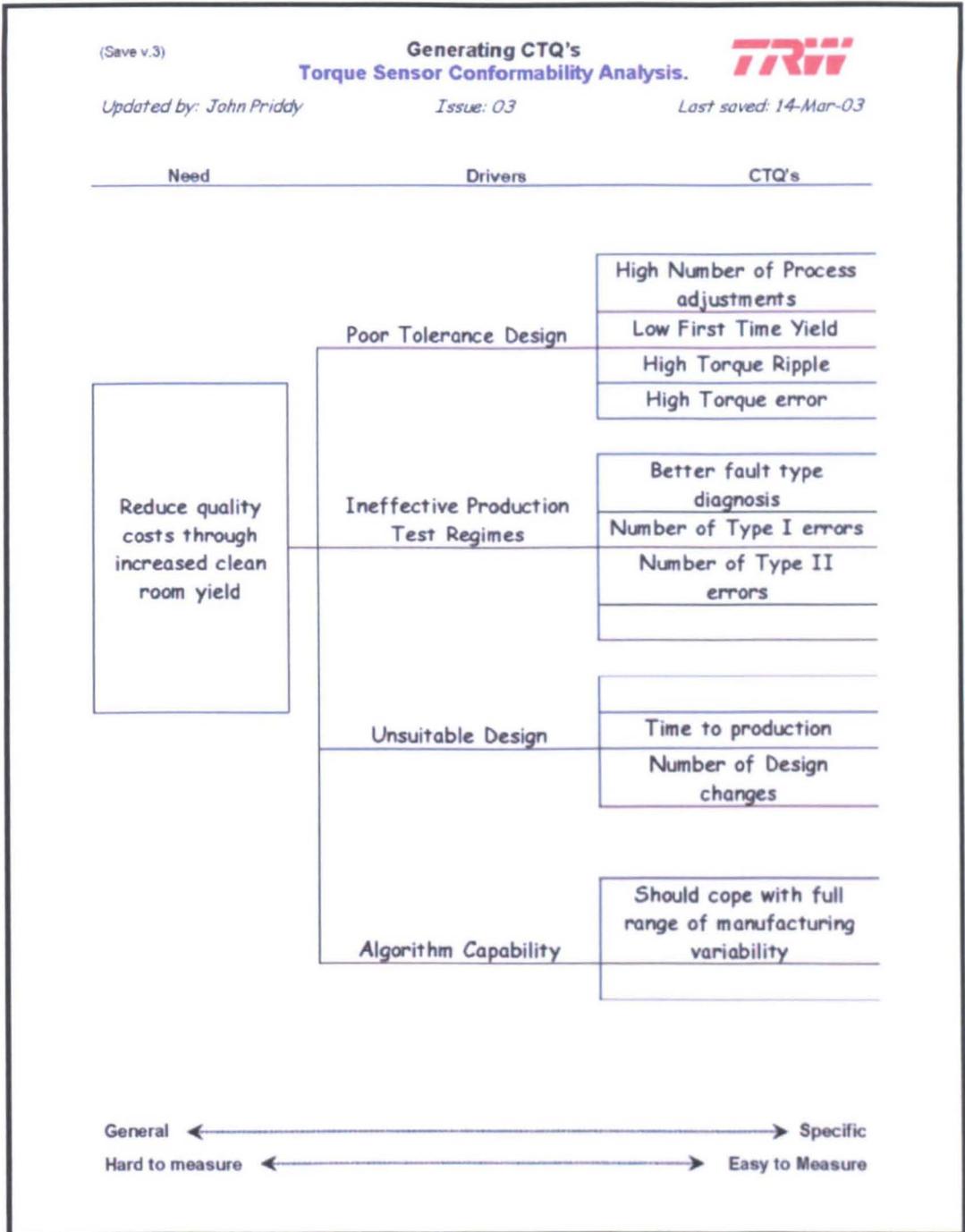
<b>Project Name</b>	Reduce Quality Costs for the EPAS Gen2.5 Torque Sensor	<b>Business / Location</b>	ECS Shirley
<b>Green Belt</b>	John Priddy David Johnson	<b>Telephone Number</b>	0121 627 3185 0121 627 3824
<b>Master Black Belt</b>	William Furse	<b>Telephone Number</b>	0121 627 4054
<b>Champion</b>	Phil Browne	<b>Telephone Number</b>	0121 627 4574
<b>Start Date:</b>	1 <sup>st</sup> March 2003	<b>Target End Date:</b>	31 <sup>st</sup> July 2003

Project Details					
<b>Project Description</b>	Apply electronic Conformability Analysis to the EPAS Gen2.5 Torque Sensor to enable the identification and reduction of quality costs Increase probability of high yield on EPS Gen2.5 Torque Sensor production.				
<b>Business Case</b>	High quality costs associated with EPAS Gen1 torque Sensor must be avoided for Gen2.5. eCA provides a method for the assessment and assignment of quality costs. Hence a successful implementation of the technique will provide a methodology for the reduction of future quality costs. Yield problems experienced by the EPS Gen1 torque sensor are likely to recur on Gen2.5 owing to similarities in design & proposed processes. Scrap rate for Gen1 from the clean room at Holford is currently ~10% (£16.6k per week)				
<b>Problem Statement</b>	How to predict the quality costs likely to be experienced by the EPAS Gen2.5 torque sensor relative to previous generations Identify likely causes of poor yield on EPS Gen2.5 Torque Sensor through analysis of Gen1				
<b>Process &amp; Owner</b>	ECS				
<b>Scope</b>	<b>Start:</b>	Analysis of the design / manufacturing interface			
	<b>Stop:</b>	Determination of product quality costs, at end of clean room, & recommendations for change to design, processes and algorithms. Due to the scope of the 'umbrella' robustness project the main focus for change will be algorithmic improvements. Recommendations for change will be passed to Conekt and improvements will be controlled by Phil Browne.			
	<b>Includes:</b>	Application of eCA, TRW Processes			
	<b>Excludes:</b>	Model Validation, System Design, Mechanical Design, Algorithm Design, Supplier Issues. In-service or system level manufacturing failures. Optical characteristics			
<b>Project Goals</b>	<b>Metric</b>	<b>Baseline</b>	<b>Current Gen1</b>	<b>Goal</b>	<b>Entitlement</b>
Reduced Quality Costs	DPMO out of clean room (per test metric).	As current		TBD	TBD
<b>Expected Business Results</b>	Increased awareness of the impact of design decisions in association with production and test capabilities. Identified future work for GB pipeline				
<b>Expected Customer Benefits</b>	Decreased product quality costs through advance knowledge of likely problem areas. Increased system reliability.				

<b>Team members</b>	John Priddy, David Johnson, Dave Wilkinson, Peter Duncan, Ray Halmshaw, Tim Sworn, Rob Pinnock, Gavin Brown
<b>Support Required</b>	Dave Ward, Garry Morley, John Farmer, R. Bachelor, S. Twilton
<b>Risks or Constraints</b>	Poor tolerance and manufacturing data, unrealistic model performance, Delays in model validation.

## 15.2 Critical To Quality Feature Assessment



## 15.3 SIPOC Analysis

(Save v.3)

### SIPOC Torque Sensor Conformability Analysis.

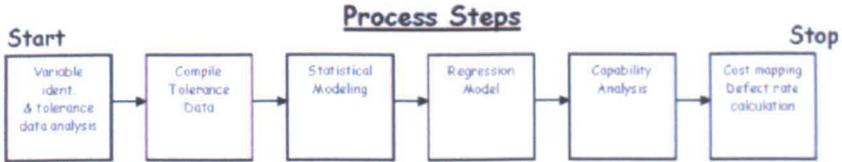


Updated by: David Johnson

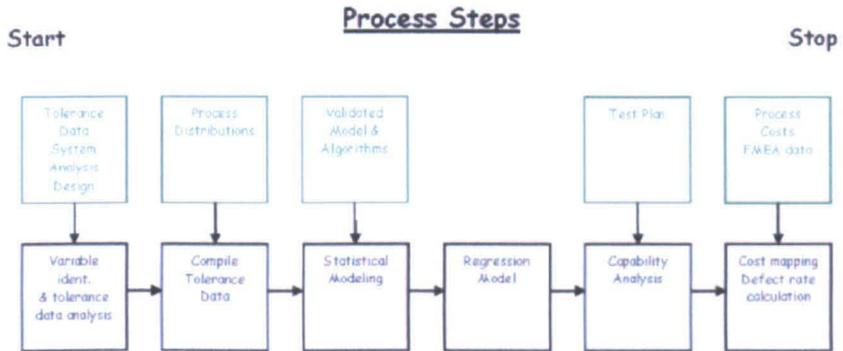
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Last saved: 18-Jun-03

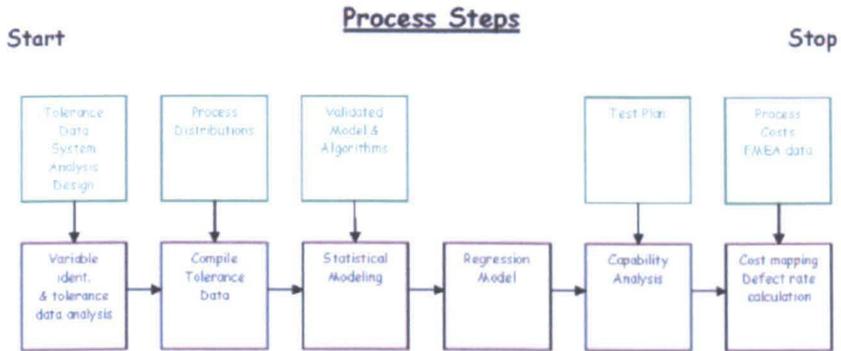
Supplier	Inputs	Process	Outputs	Customers
Holford / Shirley	Product Design & Specification	<i>electronic Conformability Analysis</i>		
Holford	Process & Test Plan		Product Capability	Holford / Shirley
Shirley	Validated Model & Algorithms		Capability Breakdown	Holford / Shirley
Holford	Tolerance Data & Stack analysis		Defect Rates	Holford / Shirley
Holford	FMEA Data		Cost of Quality	Holford / Shirley
Holford	Process Capabilities		Implementation documentation	ECS
Holford	Process Costs			
Shirley	Systems Analysis			



Supplier	Inputs	Process	Outputs	Customers
Holford / Shirley	Product Design & Specification	<i>electronic Conformability Analysis</i>	Product Capability	Holford / Shirley
Holford	Process & Test Plan		Capability Breakdown	Holford / Shirley
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Holford	Tolerance Data & Stack analysis		Cost of Quality	Holford / Shirley
Holford	FMEA Data		Implementation documentation	ECS
Holford	Process Capabilities			
Holford	Process Costs			
Shirley	Systems Analysis			



Supplier	Inputs	Process	Outputs	Customers
Holford / Shirley	Product Design & Specification	<i>electronic Conformability Analysis</i>	Quality Metrics	Holford / Shirley
Holford	Gen1 Manufacturing Data		Implementation documentation	ECS
Mere Green	Gen1 Manufacturing Data		Model Critique	ECS / RCOMPAS
Shirley	Validated Model & Algorithms			
Shirley	Systems Analysis			
RCOMPAS	eCA Tools			



Analysis of eCA activities required for Green Belt Project

Cause and Effect Analysis of: High Quality Costs Associated with EPS Gen 1 Torque Sensor

Stage	Potential Cause	Cause Detail	Comments	Keywords	Action	
Sensor Design	Customer demand Design Concept	Customer or Holford	Are there any specific reqts, e.g. dual channel, non-sliding contact elements, torsion bar stiffness?	Requirements	Query T. Burton et al	
		Need for algorithmic correction	Some aspects of design can not be controlled through tolerance spec., few are automatically compensated. Algorithmic correction is applied to most parameters, some others are corrected via fine tuning @EOL.	Algorithm	TBD	
	Components	Intolerance to contaminants		Virtually any contamination of the LAD/DAD leads to a fault being detected.	Contamination	Owned by Holford project
					Fault tolerance Design	Future project
		Discs	Design for this component is virtually fixed. However there may be scope for modification if benefits warrant it.	Design	Owned by Mech. Design	
		LAD/DAD	Specification for this component is virtually fixed. However, the true reqts for this component are not fully known/documented	Requirements	Owned by System Design	
		Shaft	Design for this component is virtually fixed.	Design	Owned by Mech. & Optics Design	
		Light pipe & carrier (Gen 2 only)	Design for this component is virtually fixed. However there may be scope for modification if benefits warrant it.	Design	Owned by Mech. Design	
		LED	Specification for this component is virtually fixed. However, the true reqts for this component are not fully known/documented	Requirements	Owned by System Design	
	Fault tolerance Sensitivity to variation	PCB assembly	Design for this component is virtually fixed. However there may be scope for modification if benefits warrant it.	Design	Owned by Elec. Design	
		Sensor Housing	Design for this component is virtually fixed. However there may be scope for modification if benefits warrant it.	Design	Owned by Mech. Design	
		Sub-Optimal Design	Any detected fault causes the torque & pos. sensing to cease	Fault tolerance Design robustness	Future project	
		Tight tolerances required	Too many of the sensor mechanical parameters are crucial to its overall conformance to specification.	Parameters	TBD	
Demanding Man. process Tight spec.		Processes required may be more expensive than automotive standard	Man. Proc. Costs	TBD		
		The requirements spec. may be tighter than necessary.	Requirements	Owned by System		

	Unvalidated model		Sensor design was based on a geometry for which there were unknown parameter interactions	Parameters & Interactions	Design TBD
	Historical reasons	Parochial dev. not fully documented or justified	Sensor and algorithms under the control of 2 people – no evidence of peer-reviewing and largely piecemeal – single dimensional, analysis	Algorithm	TBD
			Algorithm design based on unproven model	Algorithm & Unproven model	TBD
System Design	Customer demand		Are there any specific reqts inherited from the system level	Requirements	Query T. Burton et al
	Interfaces	Shaft to bearing alignment	Upper Column support is a pressed steel fabrication. Its dimensional precision and accuracy is not compatible with the sensor. However the magnitude of its effect is unknown	System loads	Future project
	No noise isolation	Driver/steering wheel	Radial (or axial?) loads on the steering wheel are transferred into the sensor. Insufficient Upper Column stiffness?	System loads	Future project
		Gear	Unsteady load into sensor (tooth frequency). Load causes some bending/distortion of shaft/IBC and changes in friction.	System loads	Future project
		Vibration	Magnitude of vibration transferred from the system into the sensor is unknown	System loads	Future project
		Intermediate shaft reaction forces	The intermediate and sensor bottom shaft centre lines are not co-axial. Hence torque reaction forces will put bending forces into the sensor. These may be large.	System loads	Future project
Manufacture	Materials	Plastic parts	Contamination is believed to be solely due to internally 'stored' debris.	Contamination	Owned by Mech. Design
		Batch changes	Unknown effect	Process variability	TBD
	Process	Hofford Process capabilities	Process flow defined by necessary assemblage sequence. Are processes capable for tolerances requested.	Process capability	TBD
		Mere Green	Process flow defined by necessary assemblage sequence. Are processes capable for tolerances requested.	Process capability	TBD
		Emicron – discs	Inadequate Cpk	Process capability	Under investigation (John Lewis)
		Melaxus – LAD/DAD (Supplier?) Shaft	Unknown effect – supplier capability unknown	Requirements	TBD
		CTP Coil – Light pipe & carrier (Gen 2 only)	Capability study done (with R.Bachelor) – supplier capability estimated from SPC data appears to be good	Requirements	System design
			Under discussion (optics not fully understood – requires Conelk study) – supplier capability unknown	Process capability	Requires specialist supplier
				Requirements	Owned by R.H/R.P

		LED	Unknown effect – supplier capability unknown	Process capability Requirements	TBD
		PCB assembly	Unknown effect – supplier capability unknown	Process capability Contamination	TBD
		Others	Plastic parts (process does not remove all debris – leading to internal contamination)		Owned by Mech. Team
	Machines	Holford clean room	Single flow production – no machine differences Unknown capability – any validation of this? Unknown calibration status	Machine calibration Process capability	TBD
		Mere Green	Dual flow production – unknown machine differences although these should be small as both lines were initially characterised against a single reference Unknown $P_{PK}$ although $C_{PK}$ seems good Unknown effect (maybe none) – shift patterns?	Machine calibration Process capability	TBD
	Personnel			Process variability	TBD
Test	Process	Holford – Single test point	Test sequence rationale unknown End of clean room test, spec. – 50840014.	Test sequence	Any validation of this? TBD
		Mere Green – Single test point	End of line test, spec. 59305375.005 (LAD sub-assembly alignment)	Test sequence	Any validation of this? TBD
	Machines	Holford – system ECU?	Unknown effect (maybe none) – any validation of this? Unknown calibration status Unknown capability	Machine calibration Process capability	TBD
		Mere Green	Unknown calibration status – Datacon equipment was initially calibrated against a single machine Unknown capability	Machine calibration Process capability	TBD
	Measurements	Holford	Based on system algorithms (and hence unproven). Faults detected may be potentially inaccurately identified.	Algorithms	TBD
		Mere Green	Affected by environment, particularly temperature fluctuations which exist at this site due to a lack of climate control Unknown effect (maybe none) – shift patterns?	Temperature Environment Process variability	TBD
	Personnel				
Environment	Contamination		Believed to be insignificant contamination from outside. Is believed to be solely due to internally 'stored' debris not removed during the pre-clean room air wash	Contamination	Owned by Holford project
	Temperature		Unknown effect (maybe none)	Fault tolerance	Owned by validation prog.
	Vibration		Unknown effect on disks (main suspect), will interact as cause of release of contamination.	Contamination	Owned by Holford project
	Humidity		Unknown effect (maybe none, maybe condensation is cause of fault detection)	Fault tolerance	Owned by validation prog.
	Orientation		Primary effect is as a cause of release of contamination	Contamination	Owned by Holford

Special Causes	Supplier fire	Emicon	The true capability of disk manufacture has not yet been realised, but the new facility should improve the situation	project Known & planned process improvement
<b>Affinities:</b>				
Key words picked from comments column for those items not already being addressed elsewhere (identified by TBD in Action column)				
Design	Model	Unproven view of the effects of sensor geometry and light source representation (model not formally validated)		Sensor construction inter-dependencies prevents problem simplification but creates tolerance stack-up. System is heavily reliant on both algorithmic and automatic correction (due to diametric opposed sensing elements). It is not possible, with complicated parameter relationships, to identify key parameters and dimensions through Pareto analysis.  Requires multi-dimensional analysis (e.g. DoE, Monte Carlo)  Not possible to create optimal design using piecemeal approach. However, our approach creates a path to optimisation (though no optimisation performed)
	Algorithm	Algorithm and mech. design based on unproven model 'on-line' algorithmic correction is applied to most parameters, some others are corrected @EOL by setting 'fine tuning' algorithm parameters appropriately. Sensor and algorithms under the control of 2 people – no evidence of peer-reviewing and largely piecemeal – single dimensional, analysis		
	Tolerances/Params (interactions)	Too many of the sensor mechanical parameters are crucial to its overall conformance to specification. Sensor design was based on a geometry for which there were unknown & complicated parameter interactions		
	Robustness	Poor design robustness (non-optimal) Some aspects of design can not be controlled through tolerance spec., few are automatically compensated		
Manufacturing issues	Machine calibration	Hofford processes single flow production hence no machine differences MG processes dual flow production hence some machine differences Unknown process m/c calibration status Hofford & MG test processes have unknown effect Unknown test calibration status		Process costs driven by design – no evidence of design/process matching.  Unknown test capability Hofford & MG.
	Man. Proc. Costs	Processes required may be more expensive than automotive standard		Unknown supplier capability

Process capability	Holford & MG process flow defined by necessary assembly sequence. Holford & MG machine capabilities unknown Are processes capable for tolerances requested. LAD/DAD, LED & PCB Unknown effect – supplier capability unknown	Unknown contributions from process variables: MG – batch, line, personnel, temperature  Holford Cpk/Ppk (m/c & overall)? Mere Green Cpk/Ppk (m/c & overall)?
Process variability	Shift patterns – unknown effect Batch changes – unknown effect	
Test sequence	Test sequence rationale unknown Holford end of clean room test, spec. – 50840014. and based on system algorithms (and hence unproven). Faults detected are not accurately identified MG end of line test, spec. 58305375.005	
Environment	Affected by environment, particularly temperature fluctuations which exist at this site	

**Conclusions:**

The sensor design analysis requires a holistic approach covering both 'pure design' aspects (such as the optimal arrangement of sensing elements) and the effects of manufacturing process variation; as the complexity of the sensor requires that the effect of manufacturing process upon its performance must be accounted for. However, not all manufacturing issues need to be investigated only those factors which affect sensor geometry (e.g. not contamination), and hence the predictable performance of the sensor, should be investigated with a view to determining both sensor robustness and conformance to performance specifications.

Focus on Holford clean room and Mere Green LAD assembly. Specify what is and what is not included in data collection plan.

Do not consider test capability – assume capable (can not split as there are only two tests, one at each EOL)

**Data Collection Plan to include:**

Mere Green –

Batch, line, personnel, temperature/environmental influences

Process capability (Cpk, Ppk ?)

Process Validation documentation as proof of test capability.

Holford –

Process capability (Cpk, Ppk ?) overall only as testing is EOL only (maybe Station 5 Cpk can be derived from EOL test data?)

Process Validation documentation as proof of test capability.

Supplier capability –

Are the effects of this small? If so then justify removing from the analysis.

LED

LAD/DAD

PCB

### Analysis of eCA activities required to support EPS robustness programme

Derivation of requirements of robustness programme pertinent to JP/DJ

Objective:

- To ensure robustness of Gen 2.5 torque sensor design (JP/DJ)
- To verify the design against specifications
- To provide information for software implementation & manufacturing (JP/DJ)
- To model the sensor and validate the software strategy/design

Deliverables:

Product & Process Design Documentation

Performance Specification (based on Gen 2.1) (JP)

Design & Software Specification (JP)

Reviewed and validated sensor model

Signal Processing & Algorithm Scheme in Simulink

Conformability Matrix showing costs versus manufacturing tolerance options (JP/DJ)

Hardware Sensitivity Analysis & Test Results

Improved General Assembly Drawing with Critical to Function (CTF) items

This project will be planned and executed to achieve the objectives and deliverables by adopting the specified lifecycle and minimising the identified risks.

- Formalisation of System Requirements (JP)
- Formalisation of System Design (align with top level EPS System definition TBC) (JP)
  - Hardware – Light source, sensing and comms functional requirements :
  - Software – signal processing requirements
  - Mechanical. – Disks and mounting for all sensing elements
  - External – constraints placed on sensor interface components (e.g. housing)
- Optical Model Validation and Sensitivity Analysis
  - Enable validation of sensor performance models, experimentally examine tolerance limits resulting from sensor sensitivity to relative component positions
  - Develop torque sensor test rig
  - Review torque sensor geometry analysis
  - Assessment of the existing optical model performance against experimental data
  - Modify optical model to correctly reproduce the experimental data
- Thermo-mechanical Sensor Modelling/Analysis
  - Develop sensor FE model to predict mechanical response of sensor to temperature & vibration. The initiation and completion of this work package will depend upon the findings of the experimental work.
- Estimation of the Cost of Quality (COQ) for the sensor design using the validated model (JP/DJ)
  - Apply electronic Conformability Analysis to the sensor to determine the COQ for the device. (Using the collected data and validated sensor model.)
  - Outputs an assessment of the COQ for the sensor indicating both poorly capable and overly capable design features with regard to manufacturing processes.
- Sensor software strategy development
  - Convert ECU software model from Matlab to Simulink (To enable auto code generation)
  - Algorithm assessment and proving : current design intent
  - Algorithm Development : (timing and effort to be specified pending initial findings)
  - Validation of final algorithm against test specification.
- Product Costs
  - Update Process & Product Costs

- Design Review

Peer Review co-ordinated and implemented by D.Wilkinson and R Helmshaw. Design change to then be reviewed with mechanical design team.

Limitations of robustness exercise without GB/eCA

Model validation & DoE based sensitivity analysis provides:

Some awareness of parameter interactions and sensitivity. However, the extent of the knowledge gained is limited because DoE tests only at design tolerance limits and ignores the probabilistic aspect of manufacturing capability or process distribution (implicit assumption of  $Cpk \sim 1.3$ ), because of this the analysis does not identify true device sensitivity. The consequence of this is a biased significance of factors and causes badly prioritised algorithm changes

Additionally the absence of formal integrated manufacturing involvement (relies on verbal testimony) does not improve the design for manufacture. A likely consequence is [a need] to assume that algorithms can fix everything.

Results:

More effort required to develop algorithms- some of which is wasted effort and development priorities may be poorly weighted.

Benefits of robustness exercise with eCA

Monte Carlo simulation targets, explicitly, process distribution and provides a more reliable sensitivity analysis. A comparison to quantify the benefits, of including this analysis, is only possible if true process capabilities are known. Qualitatively the benefits are:

- Allows comparison between algorithm effort and process change (though to fully realise the potential benefits this would require cost functions for both process change and sensor effect on system).
- Targeted effort in algorithm improvements to match available manufacturing capability
- Minimise code space.
- Identify areas to relax tolerances.
- Identification of areas which require better process control

### Comparison of required Green Belt & EPS robustness programme activities

There is a strong cross correlation between the requirements of the EPS robustness exercise and the areas covered by the green belt project.

A particularly concerning potential failure of the EPS robustness exercise which excludes the application of eCA is the lack of consideration of the interaction between design and manufacture and the resulting effects upon the ability of the Torque Sensor to meet system requirements consistently and satisfactorily. As described in the *Analysis of eCA activities required to support the EPS robustness programme* the programme excluding the application of eCA to the Torque Sensor will have potentially serious shortfalls, which may be summarised as:

- Poor understanding of the multidimensional performance space
- Lack of understanding of parameter influence and interaction
- Poorly targeted algorithm improvements
- No capability to suggest manufacturing changes that will lead to quality improvements

The inclusion of eCA into the robustness program facilitated by the Green Belt project will enable these points to be addressed, as determined in the *Analysis of eCA activities required for Green Belt Project* the project activities will provide a number of benefits including those summarised below:

- A view of the intended product performance space
- A view of the manufactured products performance space
- An understanding of the influence of and interaction between product parameters upon the performance space

From the conclusions of the Green Belt project Cause and Effect analysis we may determine that the sensor analysis must be approached from a holistic standpoint. The analysis must cover both the design of the sensor and the associated manufacturing issues. This is opposed to a typical approach which would partition the analysis into two separate exercises. We must also note that the design and manufacturing issues to be addressed must be limited to those directly influencing product robustness ('robustness' is defined as the level sensitivity of the product to parametric variation). Further widening the scope to include other issues would limit the effectiveness of the project.

A potential approach which may be taken to address both the requirements of the Green Belt project and Robustness Programme is to apply Electronic Conformability Analysis to the sensor. This would enable us to determine both the current level of conformity of the device and suggest areas of potential improvement. The technique may also be applied in an iterative manner to give an indication of the success of any modifications (in increasing product robustness) made to both the sensing hardware and/or software.

Through analysis and direct interpretation of the data generated by the application of eCA the majority of the issues associated with the EPS torque sensor robustness programme may be addressed.

This analysis leads us to a set of specific issues which must be included in an analysis of the EPS torque sensor, these are:

- The effect of manufacturing variation upon sensor conformance to specification
- An identification of the areas of sensor hardware best modified to improve sensor robustness
- A prioritisation of the significance of the variation of manufacturing processes upon sensor performance
- A prioritisation of sensor parameter variation introduced by probabilistic manufacturing process variation in terms of its effects upon sensor performance, and hence an indication of which as to which areas algorithm improvement work is best directed
- An indication of the true requirements which must be placed upon manufacturing processes

This analysis also leads to a conclusion regarding what should be excluded from an analysis of the torque sensor as carried out within the green belt project acting under the 'umbrella' of the robustness project:

- The investigation of supplier related quality issues beyond determination of the reported parameter or process distributions

- The investigation of manufacturing measurement systems beyond establishing previous verification or flagging potential future work
- The analysis of the light generation and transmission components beyond verification of the basic characteristics
- Detailed recommendations for design, algorithm and process improvements and changes beyond establishing 'weak' areas where improvements should be targeted. Further work should be left to the appropriate expert.
- Design geometry optimisation
- LED and DAD electrical performance variation

In summary through a comparison of the requirements of both the Torque Sensor Green Belt project and the Torque Sensor Robustness Programme, this document has introduced a method to address the requirements of both along side an identification of areas which must be included and excluded from any analysis.

## 16 Appendix D: Optical Torque and Angle Sensor Overview

EPS applications require a means of determining both the level and direction of driver input steering wheel torque. In TRW's column mounted systems this function is provided by an optical torque sensor located between the motor gear and the upper steering column. Torque sensing is achieved by measuring the relative displacement of the steering column input and steering rack output shafts using two concentrically mounted metal optical encoder discs. These discs are attached to, and rotate with, their respective shafts which are attached to either end of a torsion member. The same sensor components are also capable of accurately measuring changes in steering column and motor gear angular position. This capability permits the EPS motor to be driven as a brushless AC machine when used in conjunction with three Hall Effect rotor position devices mounted at one end of the motor rotor. A unique index feature incorporated into the optical discs allows the relative position of the shaft to be determined.

### 16.1 Gen. 1 Sensor

The Gen. 1 torque/position sensor is dual path device with two separate light emitting diodes acting as light sources and for two independent Linear Array Detectors (LAD's) each consisting of 128 pixel arrays mounted in diametric opposition either side of the input/output shaft as shown below in Figure 16-1.

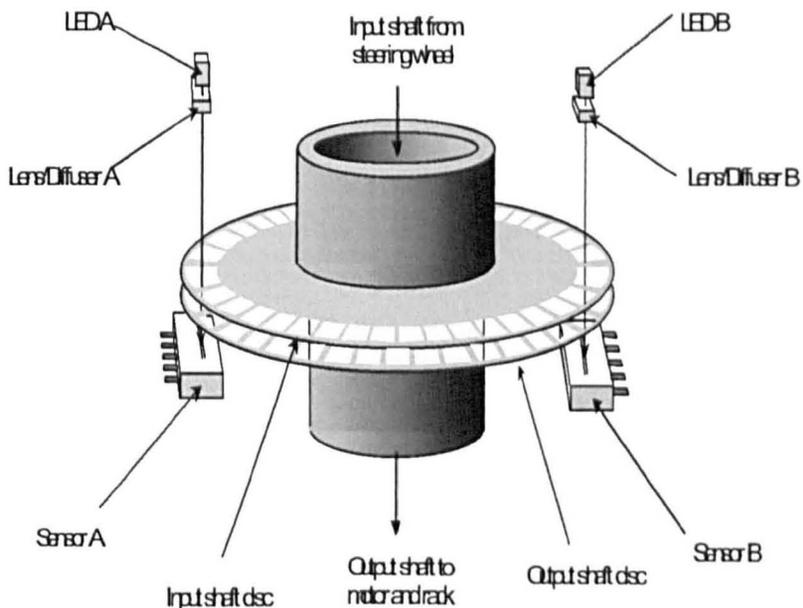
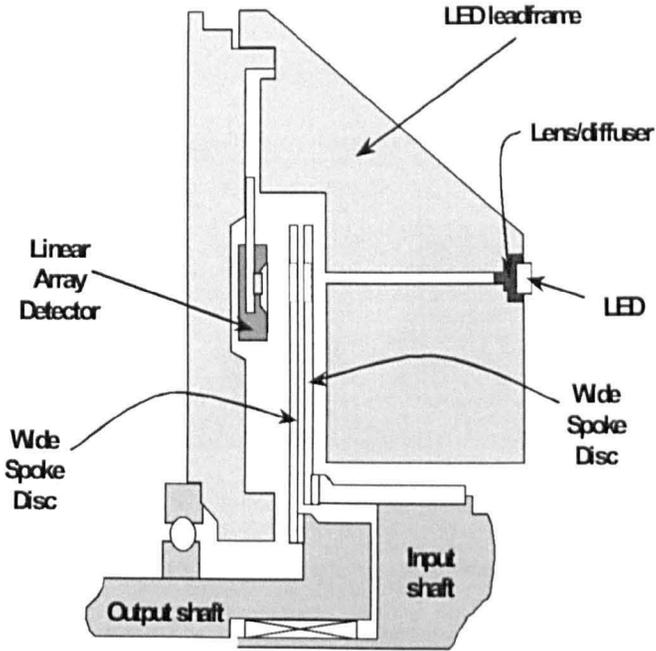


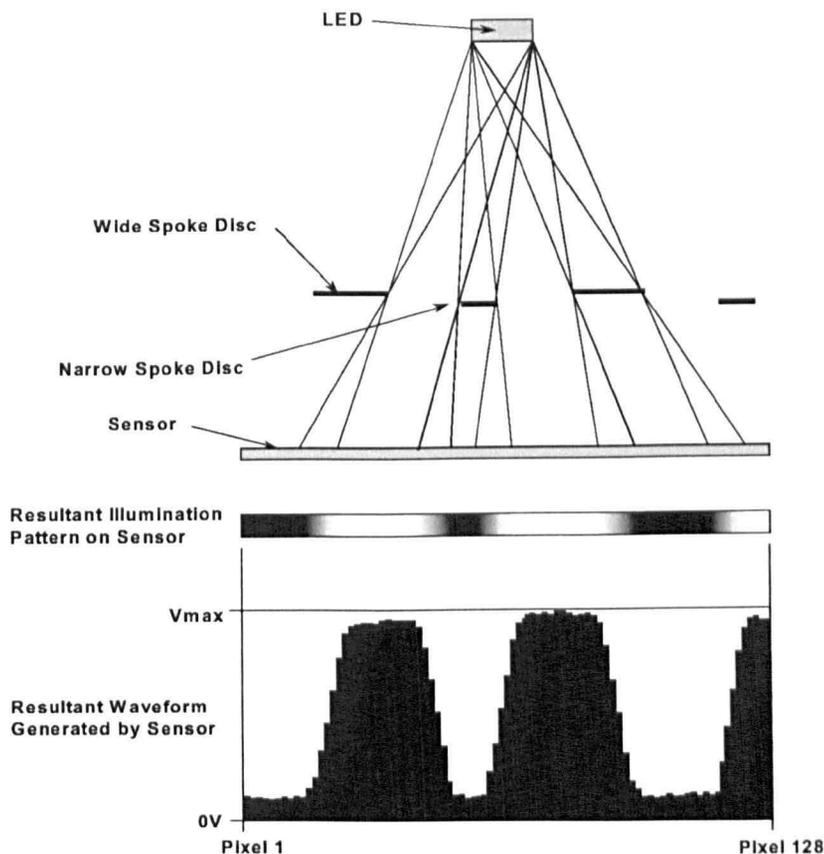
Figure 16-1 – EPS Gen. 1 Sensor Configuration

Light emitted by each source passes through the encoder discs and casts a shadow of the disc edges onto the corresponding sensors. Each sensor consists of a linear array of 128 light sensitive diodes whose output currents are integrated to give output voltages that are proportional to the incident light levels and the light integration period. A cross section through the optical components of one of the two sensor channels is shown in Figure 16-2.



**Figure 16-2 – Section Through Sensor Components**

The channels are read sequentially by an electronic control unit (ECU) which digitises the analogue signal, an example of the analogue signal is shown below in Figure 16-3 together with a ray trace of the light paths through the encoder discs.



**Figure 16-3 - Typical Sensor Illumination & Waveforms**

Once digitised the LAD waveforms are converted into two independent torque traces using custom ECU algorithms. Due to the diametrically opposed configuration of the sensing elements any errors arising from disc placement inaccuracy such as runout (non concentricity both with the shaft and each other) should be automatically corrected when the two independent signals are averaged to generate a column torque signal. Despite its desirable 'self correcting' features the sensor does require a number of software algorithms to correct some of the potential manufacturing defects before converting the channel torque signals into a column torque.